INDUSTRIAL STRENGTH...
Start Your Application From YOURITECH

Integration support
Obsolescence Management
Embedded Systems
PCAP
Human Machine Interface
Touch Solutions
Production
Custom designs
Installation
Software
Quality Management
Mechanical design
Open Frame Monitors
LCD Controller
Research & Development
Firmware
EMC tests
on-site service
In-house Manufacturing
Optical Bonding
Cover glass
System solutions
OEM Solutions

Erotech YOURITech AN EUROTECH COMPANY AOSHITE 奥靓特 Your Reliable Display Panel and Smart Touch Embedded Solution Partner

For more information about comprehensive display panels and touch embedded solutions, welcome contact us at:

https://www.youritech.com
info@youritech.com

SPECIFICATIONS No. 07TLM888	Issue: Aug. 30, 2007

Specifications for

TFT-LCD Monitor

Version 1.0

MODEL COM41T4129GLC

Customer's Approval
Signature:
Name:
Section:
Title:

CASIO

CASIO COMPUTER CO., LTD.
Device Division TFT Sales Headquarters
2951-5 Ishikawa-cho, Hachioji-city, Tokyo
192-8556,Japan
TEL 81-426-39-5121
FAX 81-426-39-5034

CASIO COMPUTER CO., LTD.
Device Division Product Quality Assurance
2951-5 Ishikawa-cho, Hachioji-city, Tokyo
192-8556,Japan
TEL 81-426-39-5138
FAX 81-426-39-5037

Approved by T. Tamura

Checked by M. Baba

Approved by H. Okimoto

Checked by E. Takabe

Prepared by M. Ueno

Revision History

Ver.	Date	Page	Description
1.0	Aug.30, '07		First issue

Contents

1. APPLICATION

This Specification is applicable to 10.32cm (4.1 inch) TFT-LCD back-light monitor for consumer use.

◎ CASIO makes no warranty or assume no liability that use of this Product and/or any information including drawings in this Specification by Purchaser is not infringing any patent or other intellectual property rights owned by third parties, and CASIO shall not grant to Purchaser any right to use any patent or other intellectual property rights owned by third parties. Since this Specification contains CASIO's confidential information and copy right, Purchaser shall use them with high degree of care to prevent any unauthorized use, disclosure, duplication, publication or dissemination of CASIO'S confidential information and copy right.

◎ If Purchaser intends to use this Products for an application which requires higher level of reliability and/or safety in functionality and/or accuracy such as transport equipment (aircraft, train automobile etc.), disaster-prevention/security equipment or various safety equipment, Purchaser shall consult CASIO on such use in advance.

◎ This Product shall not be used for application which requires extremely higher level of reliability and/or safety such as aerospace equipment, telecommunication equipment for trunk lines, control equipment for nuclear facilities or life-support medical equipment.

◎ CASIO assumes no liability for any damage resulting from misuse, abuse, and/or miss-operation of the Product deviating from the operating conditions and precautions described in the Specification.

◎ If any issue arises as to information provided in this Specification or any other information, CASIO and Purchaser shall discuss them in good faith and seek solution.

◎ CASIO assumes no liability for defects such as electrostatic discharge failure occurred during peeling off the protective film or Purchaser's assembly process.

◎ This Product is compatible for RoHS directive.

Object substance	Maximum content [ppm]
Cadmium and its compound	100
Hexavalent Chromium Compound	1000
Lead & Lead compound	1000
Mercury & Mercury compound	1000
Polybrominated biphenyl series（PBB series）	1000
Polybrominated biphenyl ether series（PBDE series）	1000

2. Outline Specifications

2.1 Features of the Product

・4.1 inch diagonal display, 960 (H) x 240 (V) dots
・8-bit / 16,777,216 colors
・3 volt single power source
・Timing generator (TG), Counter-electrode driving circuitry, Built-in power supply circuit
・Various display controls and functional selection by 3-wire serial communication method
・Standby (Power save) mode function
・Built-in rush current reduction circuit
・Schmitt trigger input method is applied for all logic input terminals
・Built-in panel residual charge reduction circuit
・High brightness LED back-light monitor

2.2 Display Method

Items	Specifications	Remarks
Display type	TN type 16,777,216 colors Transmissive type, Normally white	
Driving method	a-Si TFT active matrix Line-sequential scanning, Non-interlacing	
Dot arrangement	RGB stripe arrangement	Refer to fig. 1
Signal input method	8-bit RGB, parallel input	
Backlight type	High brightness write LED with sidelight method	
Viewing direction	From downside (6 o'clock)	Normal display orientatior

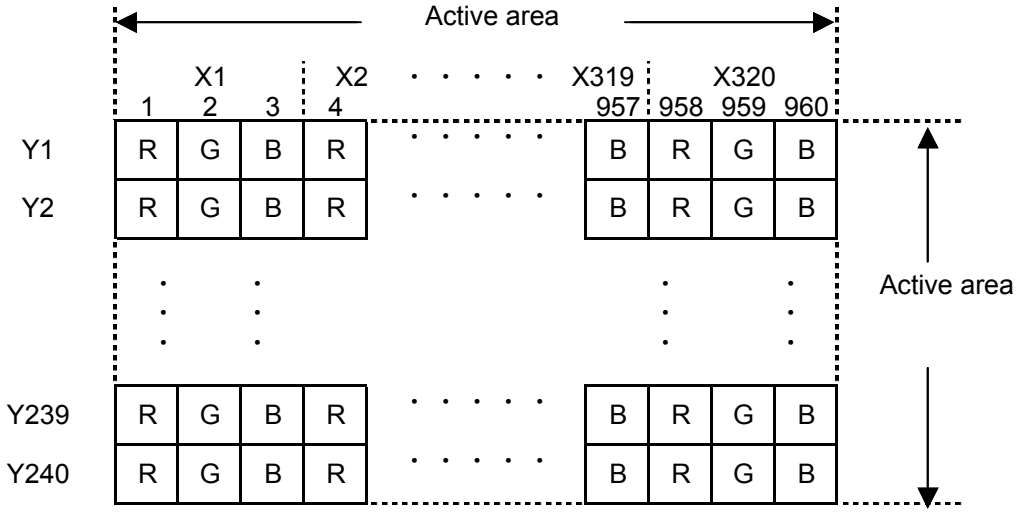


Fig 1 Dot arrangement
(FPC cable placed down)

3. DIMENSIONS AND SHAPE

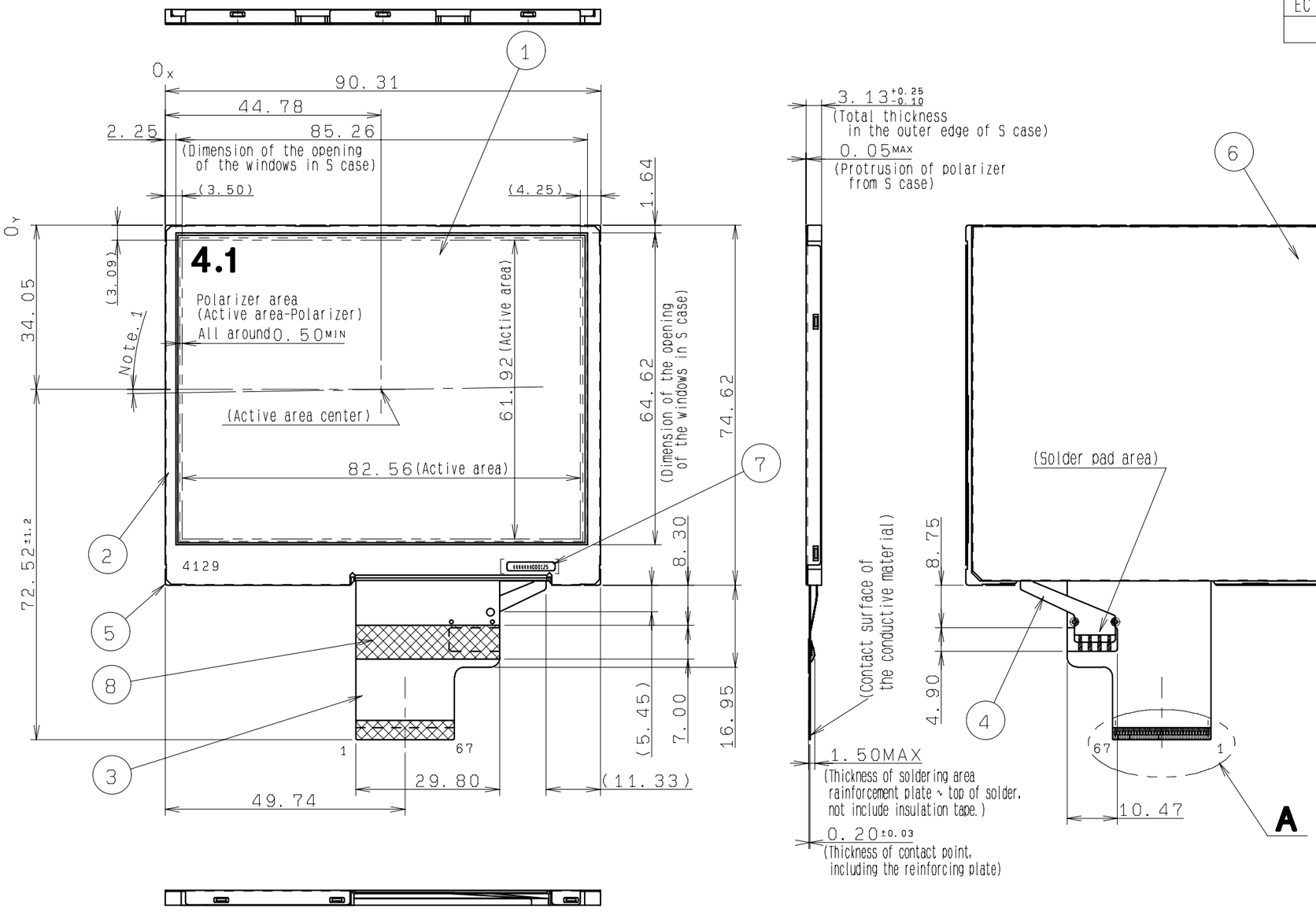
3.1 Dimensions

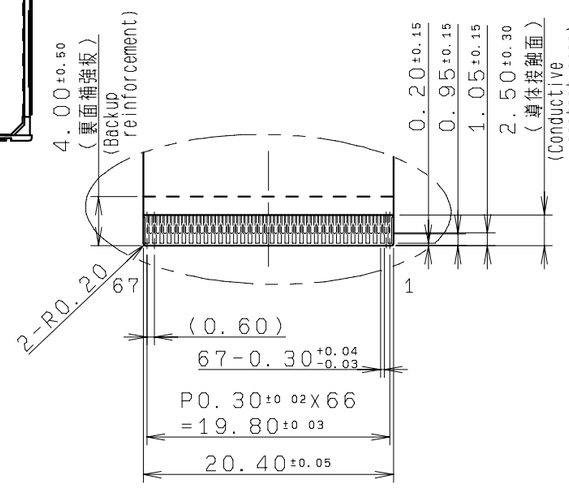
Items	Specifications	Unit	Remarks
Outline dimensions	90.31[H] × 74.62[V] × 3.13[D]	mm	Exclude FPC cable
Active area	82.56[H] × 61.92[V]	mm	10.32cm diagonal
Number of dots	960[H] × 240[V]	dot	
Dot pitch	86.00[H] × 258.00[V]	μm	
Surface hardness of the polarizer	3	H	Conforms to JIS K5400 Load: 2.0N
Weight	41.0	g	Include FPC cable

3. 2 Outward Form

EC No.	REV. No.	REVISE	DATE (Y:M:D)	APPROVED	CHECKED	PREPARED

(6/49)
07TLM888
ISSUE:Aug. 30, 2007





Ditail A (Observed from backside)
(S=2/1)

PART NAME	ITEM	PART CODE	MATERIAL GRADE	REMARK
RAINFORCEMENT PLATE	8		PI(0.125t)+Adhesive	
S LABEL	7			(10X1.85X0.075t)
S CASE C	6			
FRAME	5			
LED FPC	4			
LCD FPC	3			
S CASE A	2			
TFT-LCD PANEL	1		Glass substrate thickness=0.5t	

Note 1. Angular deviation of LCD cell from the TFT-LCD monitor's reference axis shall be less than [±40'].

Note 2. S label is affixed the area shown in the drawing.
The thickness of the S label will be added to that of S case's surface.

Note 3. Recommended FPC connectors
For LCD-FPC : Kyosera ELCO, part number: 04 6281 267 2X2 846+ (Lower contact)
For LCD-FPC : HIROSE ELECTRIC CO.,LTD., part number: FH26G-67S-0.3SHBW(05) (Lower contact)

Note 4. Protective film is affixed on front surface of the screen.
Location tolerance of the protective film shall be ±1.5 mm to the polarizing film.

APPROVED	GENERAL TOLERANCE ±0.5	SCALE 1/1(2/1)	UNIT mm	CASIO COMPUTER CO., LTD.
CHECKED	ISSUE (Y:M:D) 07:08:09	MODEL DX-4129		DO NOT DUPLICATE. CASIO CONFIDENTIAL AND PROPRIETARY
CHECKED	NAME			DRAWING NO. RJD513751D301 / REV. / SHEET / DIV.
DESIGN 荻野	OUTLINE-D4129			
DRAW 荻野				

PART

3.3 SERIAL LABEL (S-LABEL)

1) Display Items

S-label indicates the least significant digit of manufacture year (1digit), manufacture month with below alphabet (1letter), model code (4characters), serial number (6digits).

* Contents of Display

*	*	****	******
a	b	c	d

	Contents of display			
a	The least significant digit of manufacture year			
b	Manufacture month	Jan-A Feb-B Mar-C Apr-D	May-E Jun-F Jul-G Aug-H	Sep-I Oct-J Nov-K Dec-L
c	Model code	41KC (Made in Japan), 41LC (Made in China)		
d	Serial number			

* Example of indication of Serial label (S-label)

"COM41T4129GLC" (Made in Japan)

7K41KC000125

means "manufactured in Japan in November 2007, model 41K, C specifications, serial number 000125"

"COM41T4129GLC" (Made in China)

7K41LC000125

means "manufactured in China in November 2007, model 41L, C specifications, serial number 000125"

2) Location of Serial Label (S-label)

Refer to 3.2 "Outward Form".

4. PIN ASSIGNMENT

No.	Symbol	Function
1	VCOM	Common-electrode driving signal
2	D27	Display data input for (B) 00h for black display D20:LSB D27:MSB Driver IC carries out gamma conversion internally.
3	D26	
4	D25	
5	D24	
6	D23	
7	D22	
8	D21	
9	D20	
10	D17	Display data input for (G) 00h for black display D10:LSB D17:MSB Driver IC carries out gamma conversion internally.
11	D16	
12	D15	
13	D14	
14	D13	
15	D12	
16	D11	
17	D10	
18	D07	Display data input for (R) 00h for black display D00:LSB D07:MSB Driver IC carries out gamma conversion internally.
19	D06	
20	D05	
21	D04	
22	D03	
23	D02	
24	D01	
25	D00	
26	BLON	Logic signal output for external backlight circuitry
27	CS	Chip select input for serial communication (Lo: active)
28	DI	Data input for serial communication
29	SCK	Clock input for serial communication
30	VSYNC	Vertical sync signal input
31	HSYNC	Horizontal sync signal input
32	CLK	Clock input for display
33	VSS	GND
34	VSS	GND
35	POCB	Power on clear (Lo: active)
36	NC	OPEN
37	RVDD	Internal power supply
38	COMDC	Common-electrode drive DC output
39	NC	OPEN
40	VSREF	Built-in DAC reference supply
41	C1P	Contacting terminal of capacitor for charge pump
42	C1M	Contacting terminal of capacitor for charge pump
43	C2M	Contacting terminal of capacitor for charge pump
44	C2P	Contacting terminal of capacitor for charge pump
45	VDD	Power supply input

No.	Symbol	Function
46	COMOUT	Square wave output for common-electrode
47	VDD2	Internal power supply
48	VSS	GND
49	VSS	GND
50	VSS	GND
51	C3M	Contacting terminal of capacitor for charge pump
52	C3P	Contacting terminal of capacitor for charge pump
53	C4M	Contacting terminal of capacitor for charge pump
54	C4P	Contacting terminal of capacitor for charge pump
55	VVCOM	Voltage output for COMOUT
56	NC	OPEN
57	NC	OPEN
58	VGH	Positive supply for gate driver
59	C5P	Contacting terminal of capacitor for charge pump
60	C5M	Contacting terminal of capacitor for charge pump
61	VGL	Negative supply for gate driver
62	BLL2	LED drive power source 2 (Cathode side)
63	BLH2	LED drive power source 2 (Anode side)
64	NC	OPEN
65	NC	OPEN
66	BLH1	LED drive power source 1 (Anode side)
67	BLL1	LED drive power source 1 (Cathode side)

* Recommended connector: KYOCERA ELCO 6281 series（04 6281 267 2X2 846+）
HIROSE ELECTRIC FH26 series (FH26G-67S-0.3SHBW(05))
* Since FPC cable has gold plated terminals, gilt finish contact shoe connector is recommended.

Please refer to the section 3.2 "Outward Form" for pin assignment.

5. ABSOLUTE MAXIMUM RATING

VSS=0V

Item	Symbol	Condition	Rating		Unit	Applicable terminal
			MIN	MAX		
Supply voltage	VDD	Ta=25°C	-0.3	6.0	V	VDD
Input voltage for logic 1	VI1		-0.3	VDD+0.3	V	POCB,CLK,VSYNC,HSYNC D[27:00]
Input voltage for logic 2	VI2		-0.3	6.0	V	CS,DI,SCK
LED forward current	IL	Ta = 25°C	—	35	mA	BLH1 - BLL1
		Ta = 70°C	—	15		BLH2 - BLL2
Storage temperature range	Tstg		-30	80	°C	
Storage humidity range	Hstg		Non condensing in an environmental moisture at or less than 40°C90%RH		%	

Note: Please set "Power-on" and "Power-off" sequences in accordance with the "standby sequence" described later.

6. RECOMMENDED OPERATING CONDITIONS

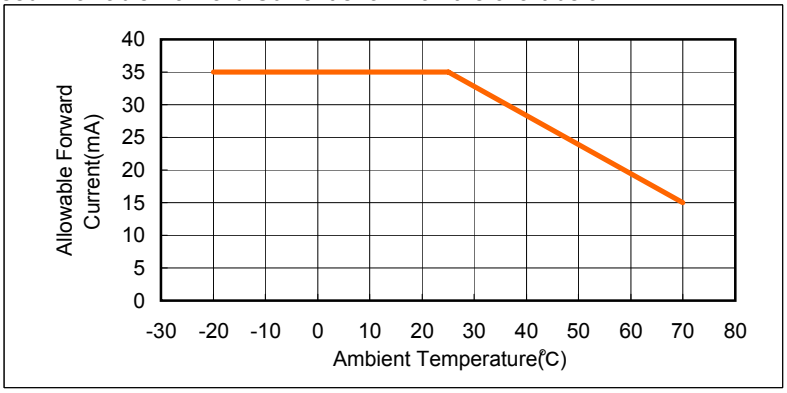
VSS=0V

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Supply voltage	VDD		2.7	3.0	3.6	V	VDD
Input voltage for logic 1	VI1	VDD=2.7～3.6V	0	—	VDD	V	POCB,CLK,VSYNC HSYNC,D[27:00]
Input voltage for logic 2	VI2		0	—	5.5	V	CS,DI,SCK
Common-electrode center voltage Note 1	VCOMDC	VCOMDC[5:0] =12h～3Ch	1.40	1.90	2.24	V	COMDC
Operating temperature range Note 3	Top	Note 2	-20	+25	+70	°C	Panel surface temperature
Operating humidity range	Hop	Ta ≦ 30°C	20	—	80	%	
		Ta ＞ 30°C	Non condensing in an environmental moisture at or less than 30°C80%RH.				

Note 1: Common-electrode center voltage indicates that optimum VCOMDC value lies within the bound of these voltages, but it does not mean that the whole range of voltages are the optimum VCOMDC value. This product must to be used with optimized VCOMDC value.

Note 2: This monitor is operatable in this temperature range. With regard to optical characteristics, refer to Item 10."CHARACTERISTICS".

Note 3: Acceptable Forward Current to LED is up to 15mA, when Ta=+70°C. Do not exceed Allowable Forward Current shown on the chart below.



7. CHARACTERISTICS

7.1 DC characteristics

7.1.1 Display Module

(Unless otherwise noted, Ta=25°C,VDD=3.0V,VSS=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Schmitt Threshold voltage	VP	VDD=2.7～3.6V	0.47×VDD	0.60×VDD	0.73×VDD	V	POCB,CS,DI,SCK
	VN		0.30×VDD	0.43×VDD	0.56×VDD	V	VSYNC,HSYNC
	VH		0.08×VDD	0.17×VDD	0.27×VDD	V	D[27:00],CLK
Pull up resistance	Rpu		45	91	182	kΩ	POCB
Output Voltage	VOH	Io = -1.0mA	VDD - 0.5	—	VDD	V	BLON
	VOL	Io = 1.0mA	0	—	0.5	V	
Operating Current	IDD	VDD=3.0V,BRIGHT[5:0]=13h CONTRAST[3:0]=7h Color bar display,fCLK=6.75MHz	—	9.0	16.0	mA	VDD
Standby current	IDDs	VDD=3.0V Other input with constant voltage	—	11.0	30.0	μA	VDD

(Unless otherwise noted, Ta=25°C,VDD=3.0V,VSS=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
VcomDC Adjusted value	VCOMDC	VCOMDC[5:0]=00h	0.94	1.04	1.14	V	COMDC
		VCOMDC[5:0]=1Fh	1.56	1.66	1.76		
		VCOMDC[5:0]=3Ch	2.14	2.24	2.34		

(Unless otherwise noted, Ta=25°C,VDD=3.0V,VSS=0V)

Item	Symbol	Condition		Rating			Unit
				MIN	TYP	MAX	
BRIGHT Adjusted value	VLCD	BRIGHT[5:0]=00h	D[×7:×0]=00h	4.10	4.25	4.40	V
		CONTRAST[3:0]=Eh	D[×7:×0]=FFh	0.92	1.07	1.22	
		BRIGHT[5:0]=13h	D[×7:×0]=00h	3.72	3.87	4.02	
		CONTRAST[3:0]=Eh	D[×7:×0]=FFh	0.54	0.69	0.84	
		BRIGHT[5:0]=2Eh	D[×7:×0]=00h	3.18	3.33	3.48	
		CONTRAST[3:0]=Eh	D[×7:×0]=FFh	0.00	0.15	0.30	
CONTRAST Adjusted value	VLCD	CONTRAST[3:0]=0h VLCD(D[×7:×0]=00h)-VLCD(D[×7:×0]=FFh)		1.35	1.50	1.65	V
		CONTRAST[3:0]=7h VLCD(D[×7:×0]=00h)-VLCD(D[×7:×0]=FFh)		2.19	2.34	2.49	
		CONTRAST[3:0]=Fh VLCD(D[×7:×0]=00h)-VLCD(D[×7:×0]=FFh)		3.15	3.30	3.45	

7.1.2 Backlight

Item	Symbol	Condition	Rating			Unit	Applicable terminals
			MIN	TYP	MAX		
Forward current	IL25	Ta=25°C	—	20.0	35.0	mA	BLH1 — BLL1
	IL70	Ta=70°C	—	—	15.0	mA	BLH2 — BLL2
Forward voltage	VL	Ta=25°C, IL=20.0mA	—	16.0	17.5	V	
Estimated Life of LED	LL	Ta=25°C, IL=20.0mA Note 1	—	10,000	—	hr	

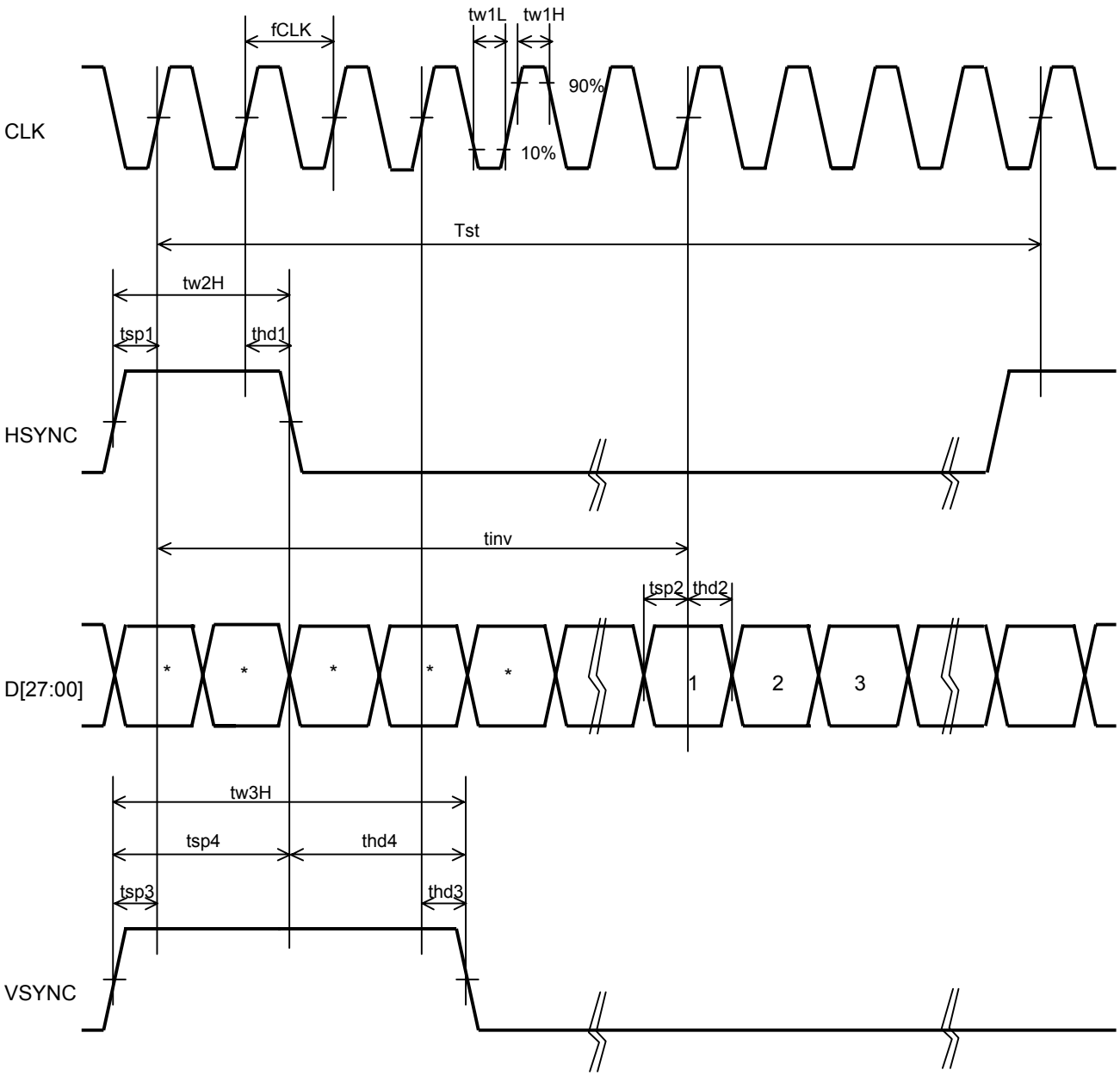
Note 1: Life is defined as the brightness decrease to half of its initial brightness.
This number is for reference, and not a guaranteed spec.
This presumption value shows the estimated life expectancy in LED side light single purpose operation.
It is different from presumption with the monitoring because the environment is different.
Life is depend on environmental temperature. Especially using high temperature decrease life.

7. 2. AC CHARACTERISTICS
7.2.1 Display Module

(Unless otherwise noted, Ta=25°C,VDD=3.0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminals
			MIN	TYP	MAX		
CLK Low period	tw1L	0.1×VDD or less	20	—	—	ns	CLK
CLK High period	tw1H	0.9×VDD or more	20	—	—	ns	CLK
HSYNC setup time	tsp1		10	—	—	ns	HSYNC,CLK
HSYNC hold time	thd1		10	—	—	ns	HSYNC,CLK
Data setup time	tsp2		10	—	—	ns	D[27:00],CLK
Data hold time	thd2		10	—	—	ns	
VSYNC setup time 1	tsp3		10	—	—	ns	VSYNC,CLK
VSYNC hold time 1	thd3		10	—	—	ns	VSYNC,CLK
HSYNC pulse width	tw2H		2CLK	—	20µs		HSYNC
VSYNC pulse width	tw3H		4	-	—	CLK	VSYNC
VSYNC setup time 2	tsp4		2	—	—	CLK	VSYNC,HSYNC
VSYNC hold time 2	thd4		2	—	—	CLK	VSYNC,HSYNC
VSYNC frequency	fVSYNC		50.0	54.7	60.0	Hz	VSYNC
HSYNC frequency	fHSYNC		—	13.2	—	KHz	HSYNC
CLK frequency	fCLK		—	6.75	—	MHz	CLK
HSYNC signal cycle time	Tst		—	512	—	CLK	HSYNC
Data invalid period	tinv		5	11	58	CLK	D[27:00],HSYNC

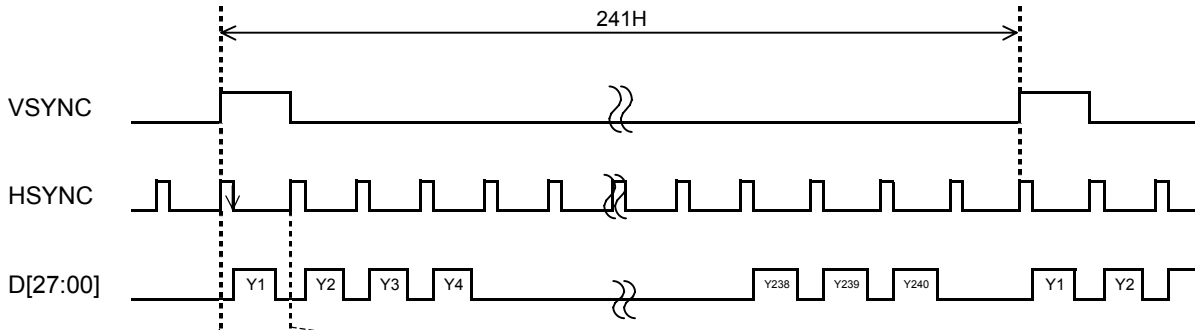
Switching Waveform Characteristics



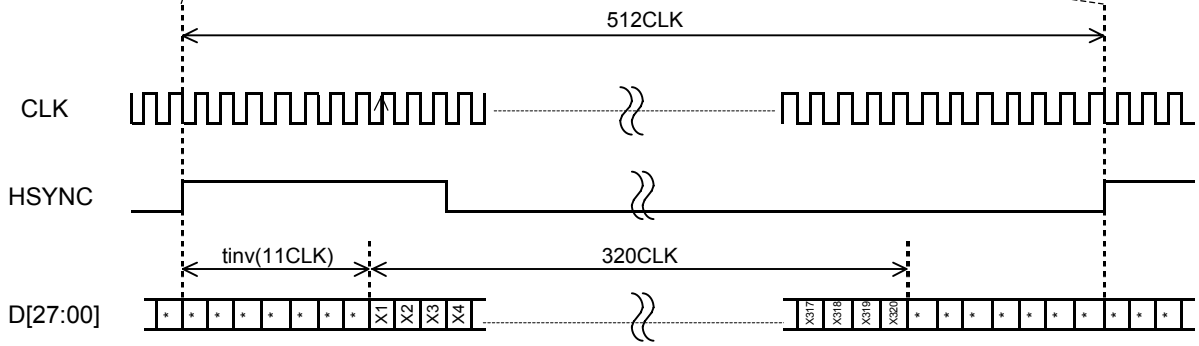
Note: Unless otherwise noted, each item is defined between each 50 % point of signal amplitude.

Example of Driving Timing Chart (Normal display direction: fCLK=6.75MHz)

Vertical Timing



Horizontal Timing

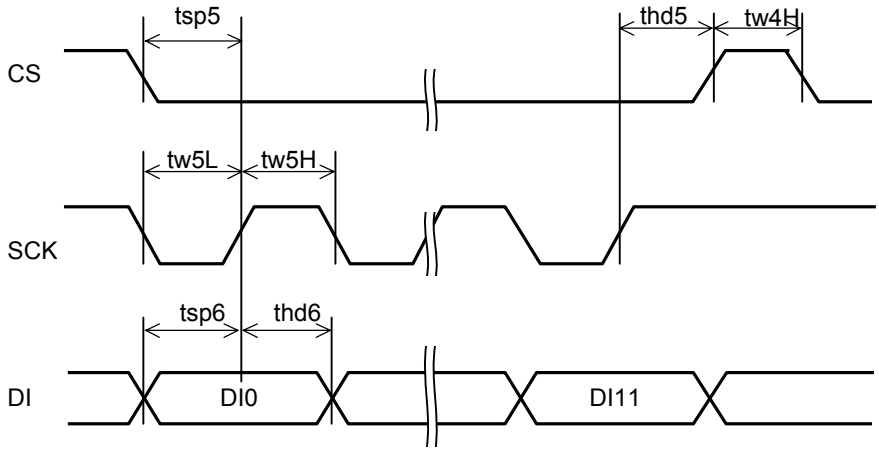


11CLK = HDISP + 3
HDISP=8

7.2.2 Serial Communication Block

(Unless otherwise noted, Ta=25°C,VDD=3.0V)

Item	Symbol	Condition	Rating			Unit	Applicable Terminals
			MIN	TYP	MAX		
CS setup time	tsp5		20	–	–	ns	CS
CS hold time	thd5		20	–	–	ns	CS
DI setup time	tsp6		20	–	–	ns	DI
DI hold time	thd6		20	–	–	ns	DI
CS pulse High period	tw4H		20	–	–	ns	CS
SCK pulse Low period	tw5L		20	–	–	ns	SCK
SCK pulse High period	tw5H		20	–	–	ns	SCK

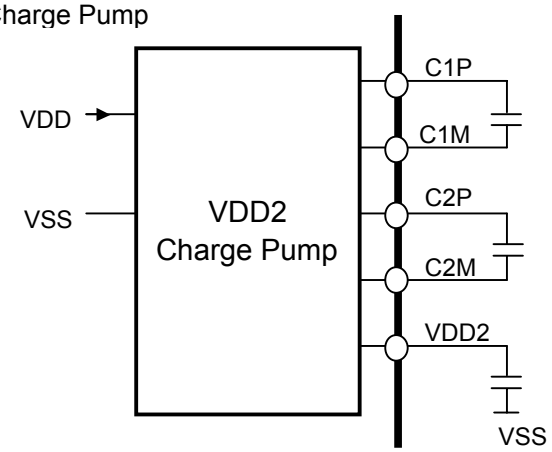


Note: Unless otherwise noted, each item is defined between each 50 % point of signal amplitude.

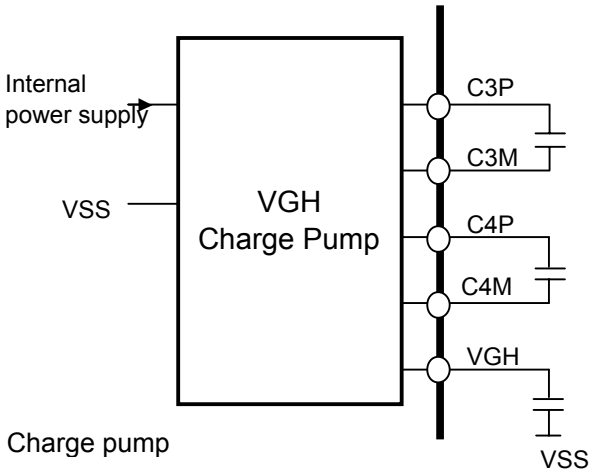
8. DESCRIPTION OF OPERATION

8.1 Power Supply

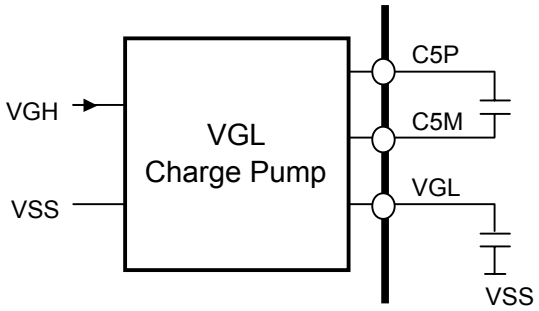
8.1.1 VDD2 Charge Pump



8.1.2 VGH Charge Pump



8.1.3 VGL Charge pump



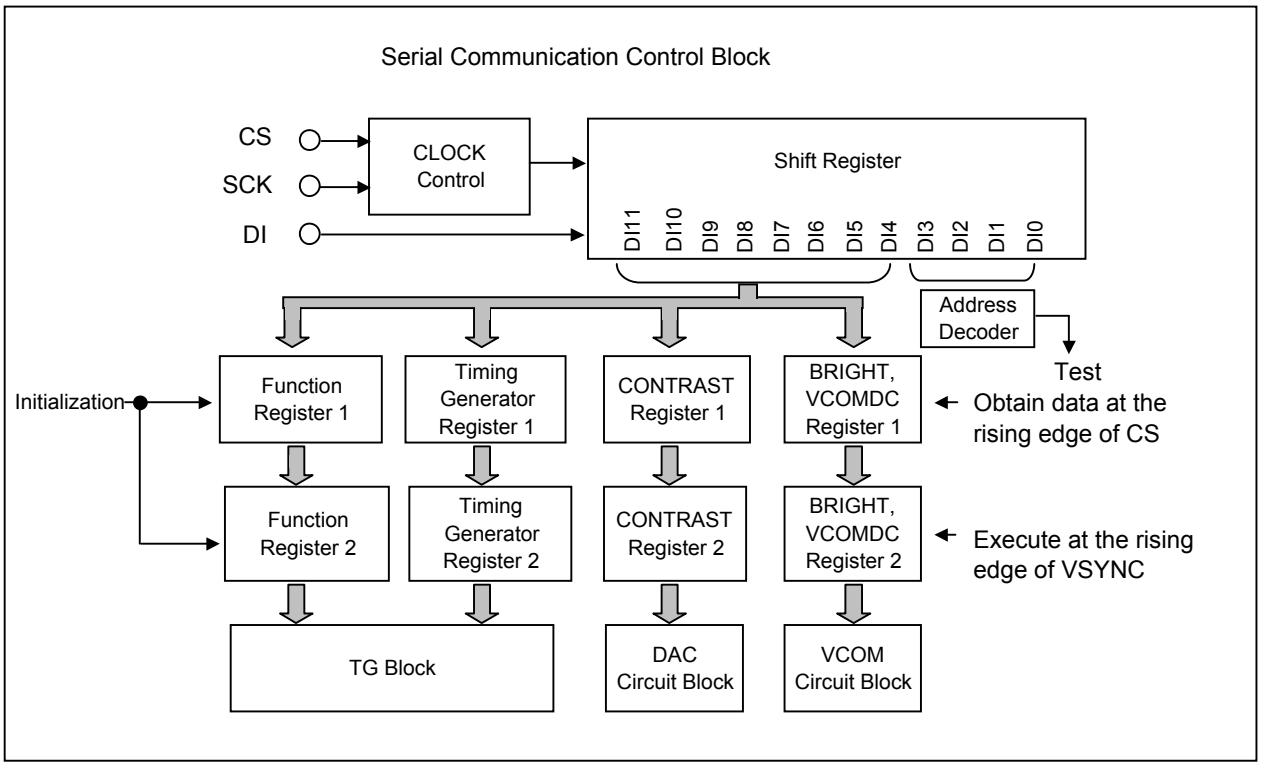
Please use ceramic capacitors with B property for external capacitors

8. 2 Serial Communication

Serial communication control block in the LCD monitor is described below.

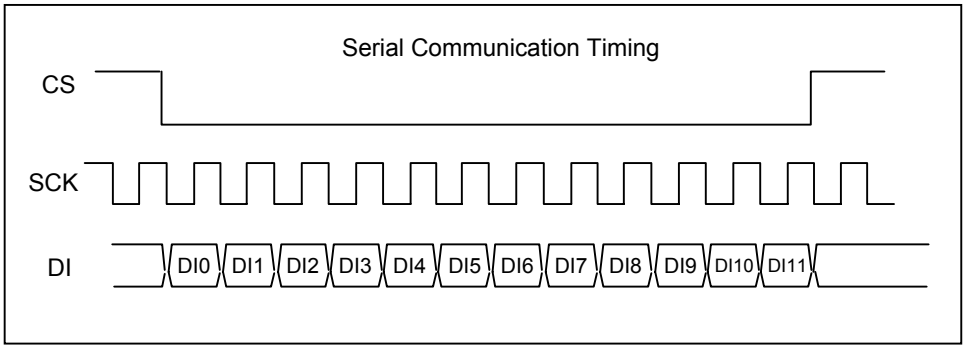
8. 2. 1 Feature Description

Serial communication control block is consist of registers that store data entered from CS, SCK, DI terminals and DAC that outputs control voltages to each part according to the data loaded from these registers .
All registers are set to initial values at power-on.
Electrostatics or noises may re-set the registers to improper values. It is advisable to set up serial communication as frequently as possible as liquid crystal could degrade if such state is left untreated for a long time.



8.2.2 Serial Communication Timing

After input signal of CS drops from Hi to Lo, the Shift Resister loads 12 bits of serial data from DI at the rising edge of the input signal of SCK.
Mode register and DAC register load the stored data at the rising edge of the input signal of CS.
When loaded DI data during the low period of CS is less than 12 bits, all loaded data are discarded .
When loaded DI data during the low period of CS is 12 bits or more, the last read of 12 bits is used .
Each command is executed by VSYNC immediately after the rising the edge of CS.
Serial Communication Control Block is configurable at any time during display and standby mode as it is completely independent from other circuitry run by CLK in the monitor.



8.2.3 Serial Communication Data

Configuration of serial data for DI terminal

First LSB — Last MSB

DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
Register address				Data							

Note: D12=D13=1 for Test mode

Register	Address				Number of bits for data	Effect of increase of value	Preset value (LSB → MSB)								User setting value (LSB → MSB)							
	DI0	DI1	DI2	DI3			DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11	DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
BRIGHT	0	0	0	0	6 (DI6-DI11)	→Brighter	-	-	1	1	0	0	1	0	-	-	User setting					
VCOMDC	1	0	0	0	6 (DI6-DI11)	→higher DC voltage	-	-	0	1	0	0	0	1	-	-	Optimum setting for each monitor					
CONTRAST	0	1	0	0	4 (DI4-DI7)	→higher contrast	0	1	1	1	-	-	-	-	User setting				-	-	-	-
PANEL1					3 (DI9-DI11)	-	-	-	-	-	-	0	0	1	-	-	-	-	-	0	0	1
VDISP	1	1	0	0	5 (DI4-DI8)	→longer vertical flyback time	0	0	0	0	0	-	-	-	User setting					-	-	-
PANEL2					2 (DI10-DI11)	-	-	-	-	-	-	-	0	0	-	-	-	-	-	-	0	0
HDISP	0	0	1	0	8 (DI4-DI11)	→longer horizontal flyback time	0	0	0	1	0	0	0	0	User setting							
PANEL3	1	0	1	0	8 (DI4-DI11)	-	0	1	0	0	0	0	0	1	Optimum setting by CLK							
FUNC1	0	1	1	0	8 (DI4-DI11)	-	0	0	0	0	0	0	0	0	0	User setting				0	0	0
FUNC2	1	1	1	0	8 (DI4-DI11)	-	0	0	0	0	0	0	1	1	User setting			1	0	0	-	-
FUNC3	0	0	0	1	8 (DI4-DI11)	-	0	0	0	0	0	0	0	0	0	0	User setting					
FUNC4	1	0	0	1	8 (DI4-DI11)	-	0	0	0	0	0	0	0	0	1	User setting						
PANEL4	0	1	0	1	8 (DI4-DI11)	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PANEL5	1	1	0	1	8 (DI4-DI11)	-	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
TESTMODE	*	*	1	1	8 (DI4-DI11)	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Configuration o f FUNC1 register

bit	Function	Description
DI4	TEST 0	Fix it to 0.
DI5	Vertical flip display	Flip image vertically (from top to bottom) 0: Normal, 1: Vertical flip
DI6	Horizontal flip display	Flip image horizontally (from side to side) 0: Normal, 1: Horizontally flip
DI7	Backlight control	Set BLON signal that controls external backlight circuitry. 0: Low 1: High
DI8	Standby control	Switch between standby and operation. 0: standby, 1: operation
DI9	TEST 1	Fix it to 0.
DI10	TEST 2	
DI11	TEST 3	

Configuration of FUNC2 register

bit	Function	Description
DI4	HSYNC polarity	Change polarity of HSYNC. 0: Positive polarity, 1: Negative polarity
DI5	VSYNC polarity	Change polarity of VSYNC 0: Positive polarity, 1: Negative polarity
DI6	CLK polarity	Change polarity of CLK. 0: Noninversion 1: Inversion
DI7	TEST 4	Fix it to 1.
DI8	TEST 5	Fix it to 0.
DI9	TEST 6	
DI10	NC	-
DI11	NC	

FUNC3 Register Configuration

bit	Function	Description
DI4	Test7	Please fix it to "0".
DI5	Test8	
DI6	GM1[0]	Register for gamma potential correction when input data D [×7:×0] is 192(=C0h).
DI7	GM1[1]	
DI8	GM1[2]	
DI9	GM2[0]	Register for gamma potential correction when input data D[×7:×0] is 148(=94h).
DI10	GM2[1]	
DI11	GM2[2]	

FUNC4 Register Configuration

bit	Function	Description
DI4	Test9	Please fix to "1".
DI5	Select gamma correction curve	Select gamma correction curve 0: built-in gamma correction curve 1: user-established gamma correction curve
DI6	GM3[0]	Register for gamma potential correction when input data D [×7:×0] is 108(=6Ch).
DI7	GM3[1]	
DI8	GM3[2]	
DI9	GM4[0]	Register for gamma potential correction when input data D[×7:×0] is 64(=40h).
DI10	GM4[1]	
DI11	GM4[2]	

TEST0 to TEST9

Please fix DI4, DI9 through DI11 of the FUNC1 registers to "0".
Please fix DI7 of FUNC2 to "1", DI8 and DI19 of FUNC2 to "0". DI10 and DI11 are no connection.
Please fix DI4 and DI5 of FUNC3 to "0".
Please fix DI4 of FUNC4 to"1".

User Setting Values

Please use "User setting values" to set up PANEL1, PANEL2, PANEL3, DI9 through DI11 of FUNC1, DI7 through DI11 of FUNC2, PANEL4 and PANEL 4. Use of unspecified values may cause malfunction.

8.2.4 Detailed Description of Function

(1) BRIGHT CONTROL (BRIGHT)

Bright setting values is controlled by 6 bit (DI6 through DI1) of BRIGHT registers.
The display lightens in proportion to data value while VLCD changes inversely with the data value.

Initial value of BLACK[00h] is 3.87V and WHITE[FFh] is 0.69V when the CONTRAST register is Eh.

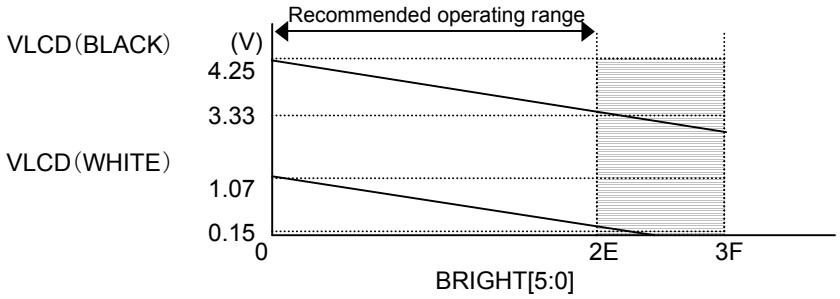
The amount of change in VLCD is 0.02V per LSB.

Recommended Operating Range
The register shall be set in 00h to 2Eh range.

(Typ.)

BRIGHT[5:0]	VLCD（BLACK）	VLCD（WHITE）
00h	4.25V	1.07V
01h	4.23V	1.05V
～	～	～
13h	3.87V	0.69V
～	～	～
2Dh	3.35V	0.17V
2Eh	3.33V	0.15V

Recommended operating range



(2) COMMON ELECTRODE CENTER VOLTAGE (VCOMDC)

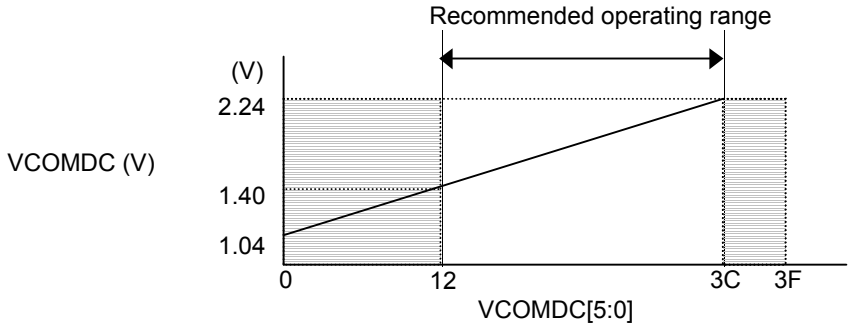
Common-electrode center voltage is controlled by 6-bit (DI6 through DI11).
The voltage is proportional to data values. Each TFT monitor has to be optimized to its own optimum value separately. This optimization is mandatory. If not implemented, liquid crystal of TFT monitor will be degraded by long operation.
Initial value of VCOMDC is1.72V.
Amount of change in VCOMDC is 0.02V per LSB.

Recommended Operating Range
Since VCOMDC has its optimum value somewhere between 1.40 and 2.24V, the register should be set in 12h to 3Ch range

(Typ)

VCOMDC[5:0]	VCOMDC (V)
00h	1.04V
～	～
11h	1.38V
12h	1.40V
～	～
3Ch	2.24V

Recommended operating range



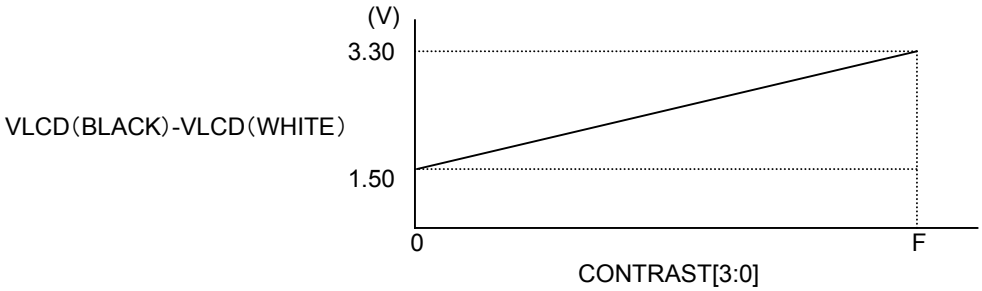
(3) Contrast Control (CONTRAST)

Contrast is controlled in 16 levels by 4-bit (DI4 through DI7) CONTRAST register.
Contrast is proportional to data values. Contrast does not affect aforementioned bright control.

Initial value of Contrast is 3.18V.
Amount of change in contrast is 0.12V per LSB.

(Typ)

CONTRAST[3:0]	VLCD（BLACK）-VLCD（WHITE）
0h	1.50V
～	～
Eh	3.18V
Fh	3.30V



(4) PANEL SETTING 1 (PANEL 1)

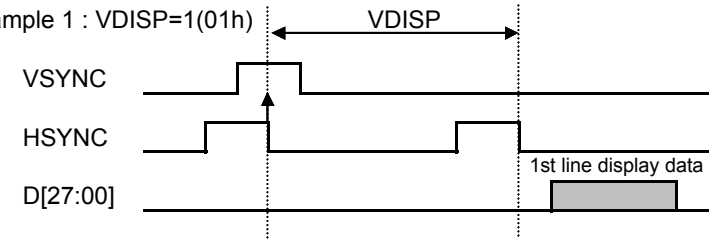
PANEL register 3-bit (DI9 thru DI11) can select operating condition from 8 choices.
Please set this register to these values.

DI9	DI10	DI11
0	0	1

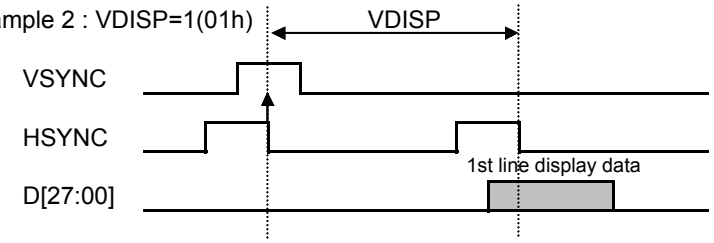
(5) VERTICAL FLYBACK TIME SET (VDISP)

The length of vertical fly back period can be set from 0 to 31H by 5-bit of DI4 through DI8 of VDISP register.
When VSYNC and HSYNC are positive polarity, "Hi" period of VSYNC is detected at the falling edge of HSYNC.
The setting value of VDISP is determined by the number of horizontal periods from the first detection of VSYNC=Hi to the first line's display data input.Please set VDISP=1 as shown in "Example 1" even if the display data of the first line is input
When the pulse width of VSYNC extends over two or more H as shown in "Example 3", the setting value is determined by the number of horizontal periods from the first detection of VSYNC=Hi to the first line's display data input.
When the initial value is "0", the first line's display data needs to be inputted immediately after VSYNC as shown in "Example 4".
When VDISP=0, please use odd number for the setting of the total number of lines that compose one field.
This function can also be used for vertical display range setup (Vertical position setup).

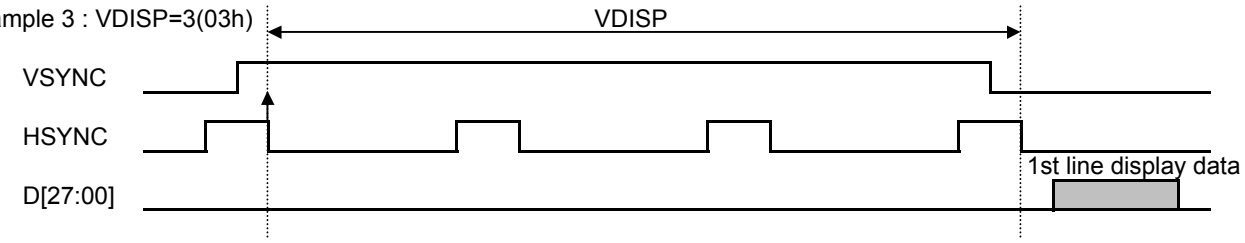
Example 1 : VDISP=1(01h)



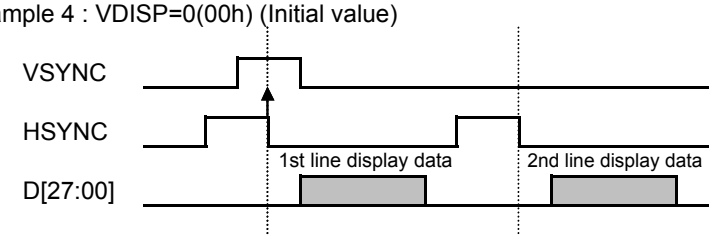
Example 2 : VDISP=1(01h)



Example 3 : VDISP=3(03h)



Example 4 : VDISP=0(00h) (Initial value)



(6) PANEL Setting 2 (PANEL2)

PANEL 2 register 2-bit (DI10 and DI11) can select operating conditions from 4 choices.
Please set this register to these values.

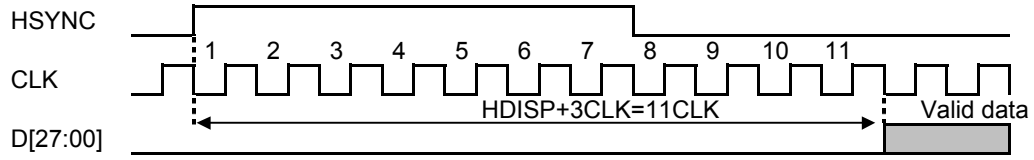
DI10	DI11
0	0

(7) Horizontal Flyback Period Setting (HDISP)

Horizontal flyback time can be set from 5 to 258CLK by HDISP register with 8-bit of DI14 thru DI11.
However, set value of 0 or 1 is prohibited. Actual flyback time is "setting value plus 3CLK".
When initial value is 8, a data after a lapse of 8 + 3CLK=11CLK from the rising edge of HSYNC is displayed as shown in the following chart.
Horizontal flyback time must be set between 5 and 58 CLK due to the restriction of Data Invalid Period.

This function can also be used for horizontal display range setup (Horizontal position setup).

Example : HDISP=8(08h)



(8) PANEL Setting 3 (PANEL3)

PANEL3 register is used for optimizing operating condition of the signals internally generated by driver IC.
Optimum setting value varies according to number of CLK in 1H period and CLK frequency.
Setting of non-optimum value may cause malfunction.
Please be sure to optimize this setting before driving.

Optimum setting value (decimal) = (number of CLK in 1H period - 1.0μ ×CLK frequency) ÷ 7.75

Round off calculated result after decimal point.

Example : When fCLK=6.75MHz, Number of CLK in 1H=512CLK
Optimum setting value(decimal) = (512 - 1.0μ × 6.75M) ÷ 7.75 = 65(decimal) = 01000001(binary)
Therefore, the optimum setting of PANEL 3 is;

DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
1	0	0	0	0	0	1	0

(9) FUNCTION SET 1 (FUNC1)

FUNC1 register sets and controls the following functions by its each bit of DI4 thru DI6.

Vertical Flip Display (Up/Down)

DI5=0 for normal display, DI5=1 for vertical flip display
After completing the setup by serial communication, the selected display mode is carried out by VSYNC.
(Normal display is defined when FPC of the monitor is place downside.)

Horizontal Flip Display (Right/Left)

DI6=0 for normal display, DI6=1 for horizontal flip display
The selected display mode is executed at VSYNC after setup by serial communication.

(Please refer to the section 8.3 for display data input sequence)

Backlight Control

DI7 switches the backlight driver IC. BLON terminal outputs set value of DI7.
Since its output level is VDD or VSS, this function can also be used for other controls than the backlight.
After completing the setup by serial communication, the selected display mode is carried out by VSYNC.

Standby Mode

DI8=0 for standby mode, DI8=1 for normal operation
Since default value of DI8 after power on is "0", it automatically goes to standby mode. Power consumption is significantly reduced in standby mode by disabling the timing generator and the LCD driving circuitry, and disconnecting current lines.
No image is displayed (white raster display) during standby mode unless DI8 is set to 1 for normal operation by serial communication. Serial data can be received by serial communication block even in standby mode.
Please refer to the section 8.4 "Standby (Power save) Sequence" for standby mode and power on/off sequence.
When normal operation is switched to standby mode, afterimage treatment is carried out before switching to standby mode.

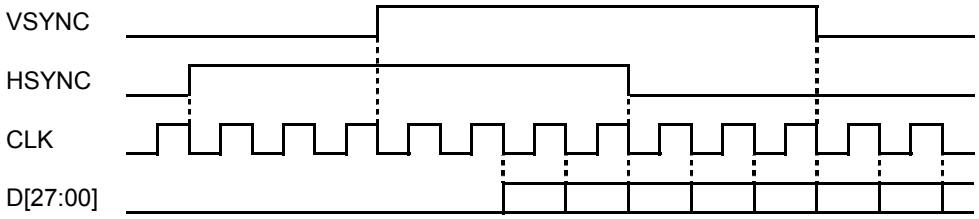
(10) FUNCTION SET 2 (FUNC2)

FUNC2 register sets and controls the following functions by its each bit of DI4 thru DI6.

HSYNC,VSYNC,CLK Polarity Switching

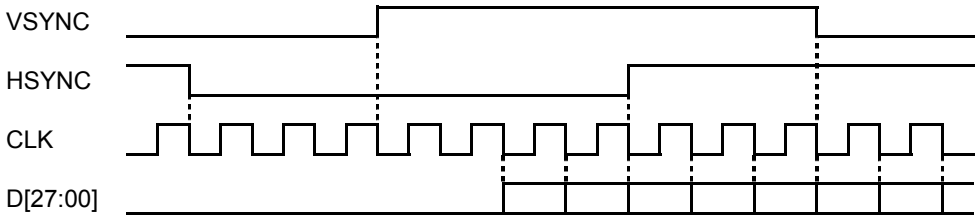
Polarity of HSYNG is switched by DI4. DI4=0 for positive polarity input, DI4=1 for negative polarity input.
Polarity of VSYNC is switched by DI5. DI5=0 for positive polarity input, DI5=1 for negative polarity input.
Polarity of CLK is switched by DI6. DI6=0 for non-inversion, DI6=1 for inversion.

Initial value of DI4, DI5 and DI6 are "0". The following chart shows polarity of each signal at the initial value.
Please set change of VSYNC,HSYNC and display data at the falling edge of CLK.

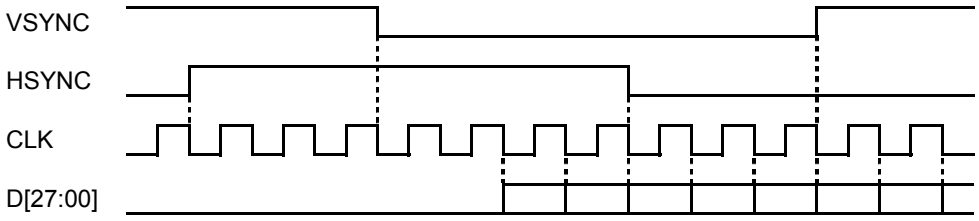


Polarity of each signal can be changed independently by logic of DI4, DI5 and DI6.

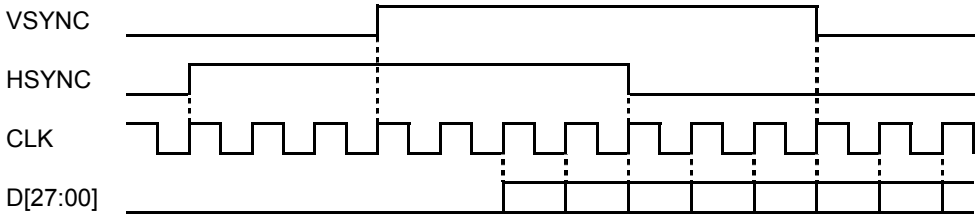
Example 1 : DI4=1,DI5=DI6=0 (HSYNC has negative polarity and low active)



Example 2 : DI4=0,DI5=1,DI6=0 (VSYNC has negative polarity and low active)



Example 3 : DI4=DI5=0,DI6=1 (CLK is reversed, data is read at the falling edge of CLK.)



(11) FUNCTION SET 3, 4 (FUNC 3, 4)

Gamma Curve Correction Select

DI5=0 of FUNC 4 Register: Deactivate user configurable gamma correction circuitry. Use built-in gamma curve.

DI5=1 of FUNC 4 Register: Activate user configurable gamma correction circuitry. Use user configurable gamma correction curve.

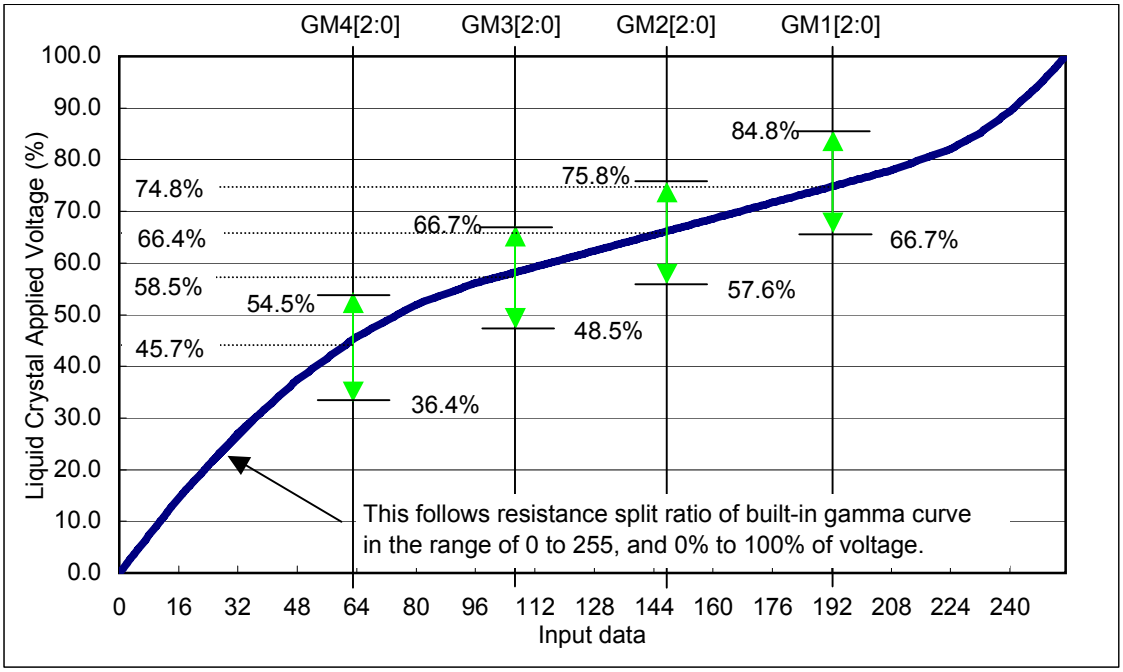
Setting Method of User Configurable Gamma Correction Curve

Gamma curve can be corrected by using GM1[2:0] thru GM4[2:0] registers of FUNC 3 and FUNC 4. GM1 thru GM4 corrects each following gamma potential respectively.

GM1[2:0] → Input data D[×7:×0] = Register for gamma potential correction at 192(=C0h)
GM2[2:0] → Input data D[×7:×0] = Register for gamma potential correction at 148(=94h)
GM3[2:0] → Input data D[×7:×0] = Register for gamma potential correction at 108(=6Ch)
GM4[2:0] → Input data D[×7:×0] = Register for gamma potential correction at 64(=40h)

Below chart shows characteristic curve of gray scale input data - liquid crystal applied voltage. Input value of "0" is assumed to be 0% of applied voltage to liquid crystal, and input value of "225" is assumed to be 100% of applied voltage to liquid crystal. Adjustable range of GM1 thru GM4 registers are described below.

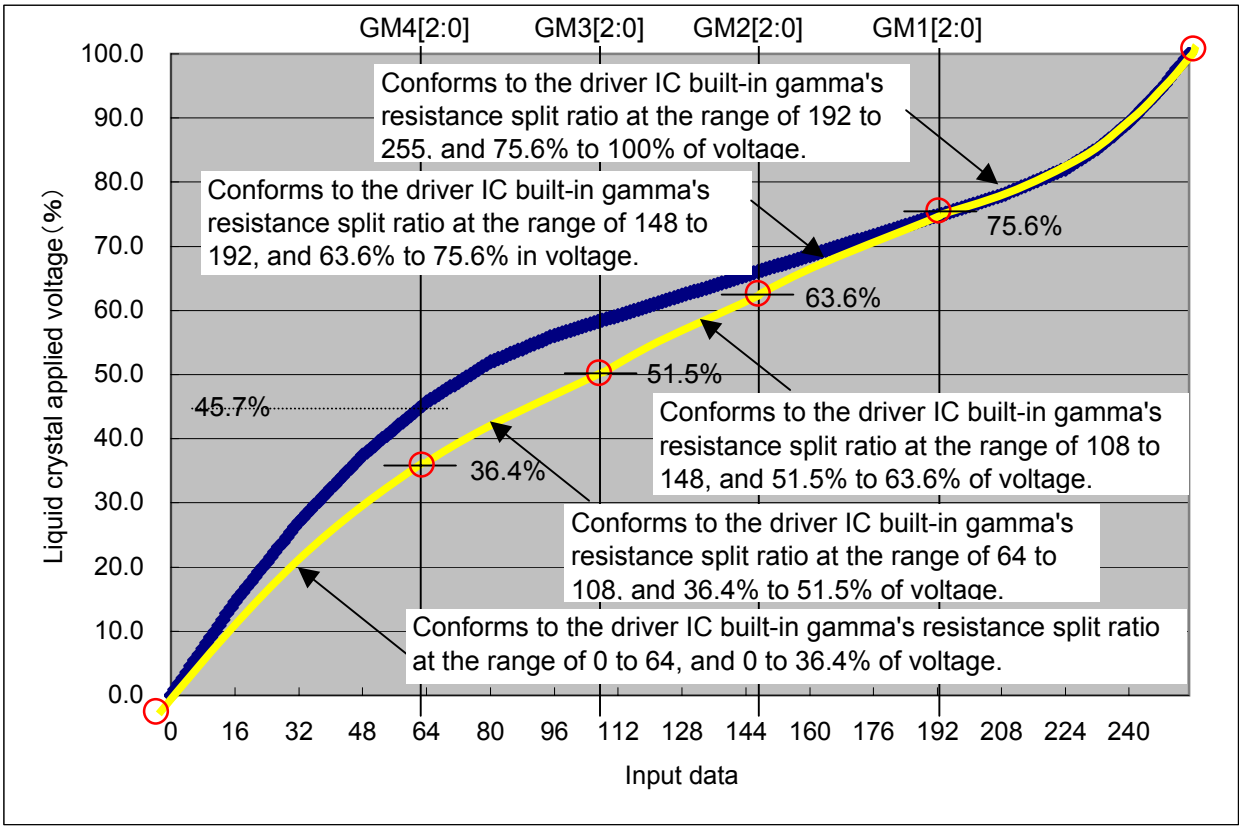
	GM4[2:0]	GM3[2:0]	GM2[2:0]	GM1[2:0]
00h	No correction	No correction	No correction	No correction
01h	54.5%	66.7%	75.8%	84.8%
02h	51.5%	63.6%	72.7%	81.8%
03h	48.5%	60.6%	69.7%	78.8%
04h	45.5%	57.6%	66.7%	75.6%
05h	42.4%	54.5%	63.6%	72.7%
06h	39.4%	51.5%	60.6%	69.7%
07h	36.4%	48.5%	57.6%	66.7%



When no correction is made to gamma potential of GM1 to GM4;
The voltages at "0" and "255" are fixed in accordance with the contrast and brightness settings,
and voltages at 1 to 254 are determined by resister split ratio produced by the driver IC built-in gamma curve resister.
(Refer to the chart in previous page)
Liquid crystal applied voltage takes the values of 45.7%, 58.5%, 66.4% and 74,8% when input date is
64, 108, 148 and 192 respectively.

When correction is made to any of GM1 to GM4 by user;
The voltage is corrected in accordance with a correction point and its set value configured by user.
The voltages at 1 to 254 are determined by resister split ratio between voltage at 0 and 225 and input data.

Example:
Darken gray scale in black side.
→ Change liquid crystal applied voltage at the 64 point to darken side.
→ Set GM4[2:0] to 7h, GM3[2:0] to 6h, GM2[2:0] to 5h and GM1[2:0] to 4h.



(12) PANEL SELECT 4 (PANEL 4)

Select operating condition of the signal generated by driver IC in accordance with 8-bit of DI4 to DI11 of PANEL 4 register.Please set this register to this value.

DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
0	0	0	0	0	0	0	0

(13) PANEL SELECT 5 (PANEL 5)

Select operating condition of the signal generated by driver IC in accordance with 8-bit of DI4 to DI11 of PANEL 5 register.Please set this register to this value.

DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
0	1	0	0	0	0	0	0

(14) TEST MODE (TEST MODE)

Select operating condition of test mode in driver IC in accordance with 8-bit of DI4 to DI11 of TEST MODE register. Please set this register to this value.

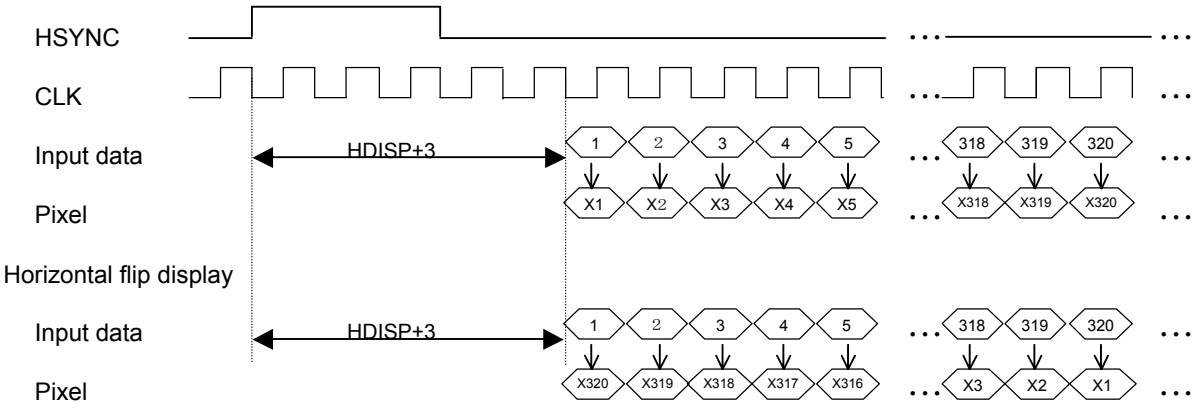
DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
0	0	0	0	0	0	0	0

8.3 Display Data 1

Input display data to D[27:00] D×0 : LSB, D×7 : MSB

Horizontal Timing and Order of Input Data

Display data shall be input in synchronization with CLK.
Polarity of CLK can be selected by DI16 of FUNCTION SET 2 (FUNC2).
Normal display: Normal display is defined as the orientation that the FPC cable on the TFT monitor is placed on the downside.

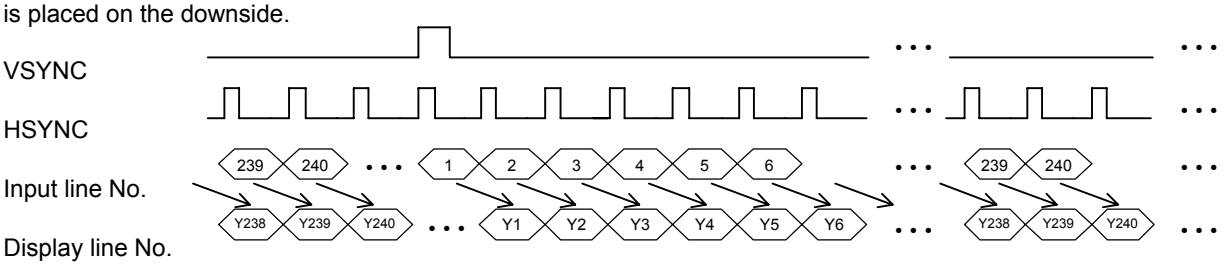


* Above timing chart shows correlation between input data and pixels in visual way and it is not actual timing chart.

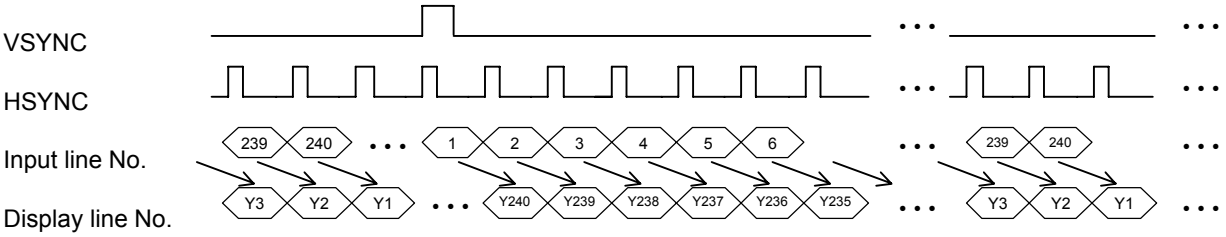
Vertical Timing and Order of Input Data

Transfer of display data that consist of 240 lines in 1 field is explained below.
The correlations between input line and display line at normal display and vertical flip display are described below.

Normal display: Normal display is defined as the orientation that the FPC cable on the TFT monitor is placed on the downside.



Vertical flip display



8.4 Standby (Power Save) Sequence

Serial communication signals of CS, DI and SCK shall be input after VDD stabilizes at 2.7 V or more V for 20 msec or more after power on. All initial values of serial data shall be set during this standby mode.
Other logic input signals of HSYNC, VSYNC, D[27:00] and CLK shall be input simultaneously with VDD or after power on (specified period marked ① in next page). All input signals shall be set to a fixed DC to reduce power consumption during standby mode.
Since the signals or voltage marked with * in next page are generated inside the LCD monitor, their sequences can be disregarded. Please follow the recommended power on/off sequence described below.

① Right after power on, serial communication registers are initialized by a power-on-clear signal generated by POCB capacitor and internal pull-up resistance. Therefore, standby control bit takes the value of "0".
By this procedure the LCD goes into standby mode which significantly reduces power consumption of the LCD. No image is displayed (white raster display) on the screen and internal power circuit is deactivated during standby mode.
Sync signal and display data (HSYNC, VSYNC, D[27:00], CLK) start to input before standby mode is released by serial communication.

② When the standby control bit is set to "1" by serial communication, the standby mode is released by following VSYNC and VGH, VDD2, VVCOM, VGL will be generated from VDD.
No image is displayed (white raster display) on the screen for 5 fields from the following VSYNC after the release of standby mode.

③ LCD goes into normal display (display under normal operation) at the timing of VSYNC after completion of the procedure described in ②. Backlight shall be lit up 1 or more field after going to normal display.
When BLON terminal is used for backlight control, backlight control bit shall be set to "1" to light up backlight by serial communication after going to normal display.

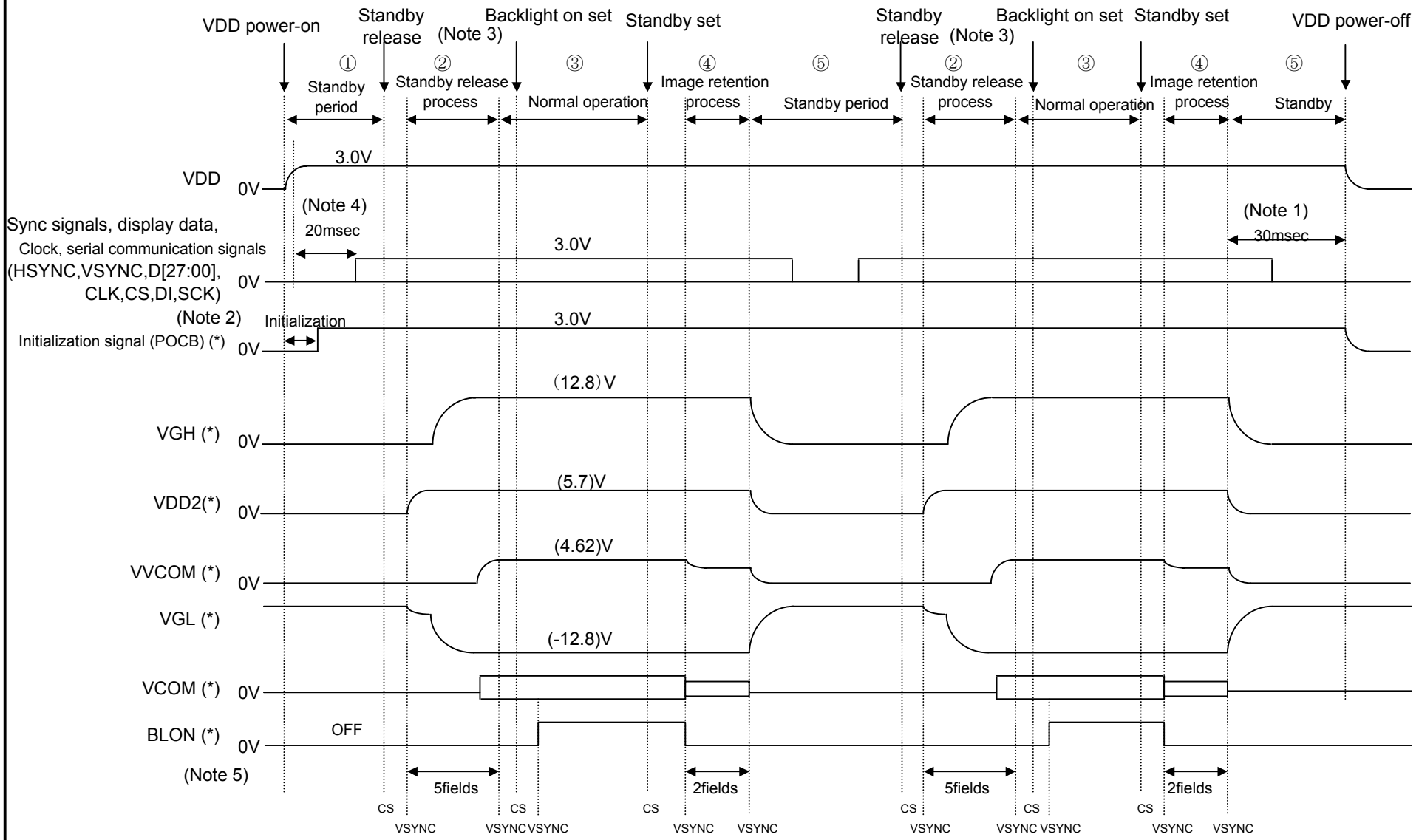
④ Standby mode can be established by setting standby control bit to "0" by serial communication.
Display data is changed to FFh at VSYNC that comes right after this serial communication, and afterimage treatment is performed for 2 fields of VSYNC. Displayed image under normal display is immediately changed to white raster display by this treatment.
Continue to input sync signal (HSYNC,VSYNC,CLK) during this period.
Backlight shall be turned off before standby control is set to "0" by serial communication.

⑤ LCD goes into standby mode, which is same as ① above, at the timing of VSYNC after completion of the procedure described in ④. Serial communication data is retained during standby mode.
Serial communication signal and input signal can be deactivated

② to ④ repeats same procedures as described above.

Below procedure must be followed for power-off.

① Implement standby setting.
② After standby setting, continue to input sync signals (HSYNC, VSYNC, CLK) during the image treatment period (until VSYNC after 2 fields subsequent to standby setting).
③ After ②, power off VDD after 30msec or more
④ Stop the sync signals (HSYNC, VSYNC, CLK) subsequent to afterimage treatment period and no later than VDD off.



(Note 1) Power off VDD more than 30 msec after VSYNC that arrives 2 fields from standby set.

(Note 2) Input CLK during the period of inputting sync signals (HSYNC, VSYNC) and display data D[27:00].

(Note 3) Due consideration needs to be given to power supply capacity as bigger current (inrush current) flows at standby release.

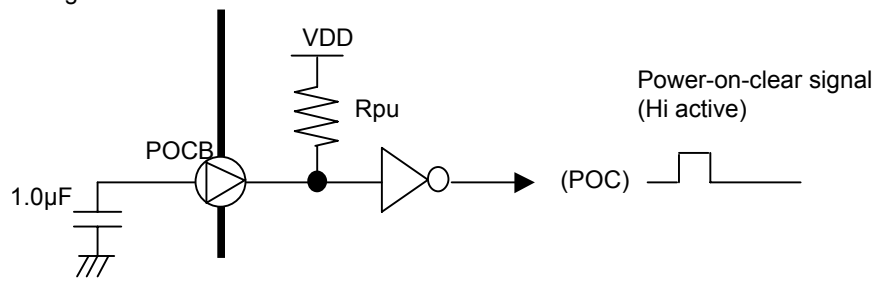
(Note 4) Serial communication signals should be input after VDD stabilizes at 2.7 V for more than 20 msec.
And initial values of all serial data should be set during this period before standby release.

(Note 5) Backlight should be turned on after 1 field from starting display. Backlight should be turned off before standby control is set to "0" by serial communication. Voltage values shown in this chart are typical values, not fixed values.

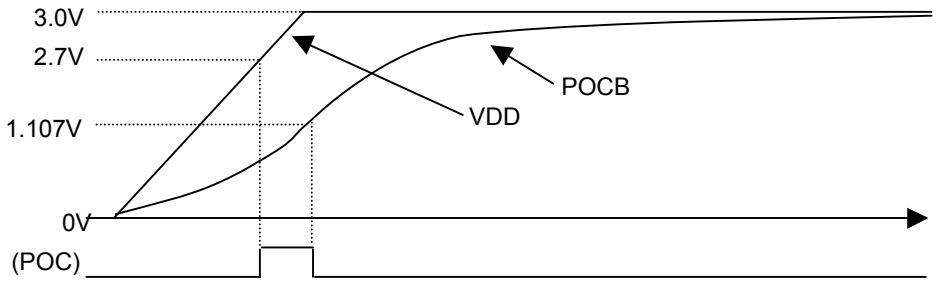
8.5 Power On Clear (POC)

The following restrictions apply to power on period and serial communication setting.

Power-on-clear circuit diagram

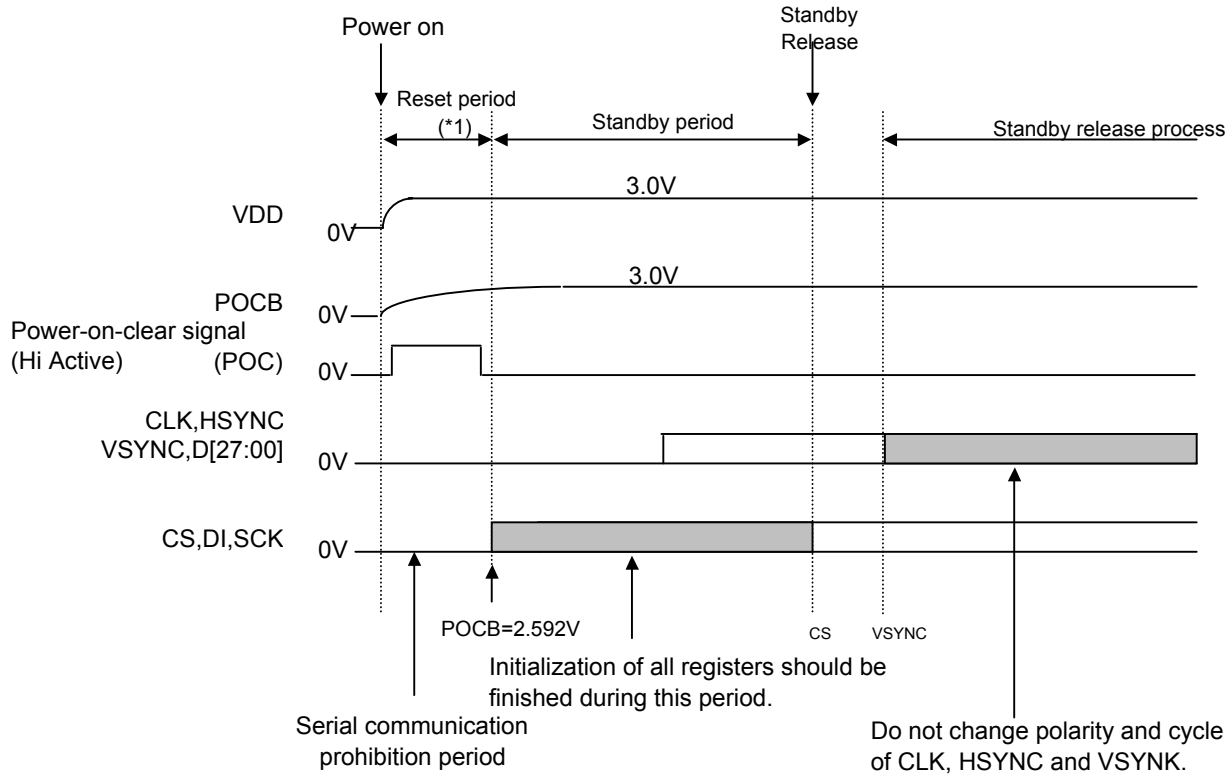


POCB terminal is connected to VDD through the pull-up resistor (Rpu).
When rising of VDD takes long time, POCB will have unstable and unpredictable waveform.
Please determine value of external capacitor by which POCB takes 1.107 V or less at VDD is 2.7V.



Power On Sequence

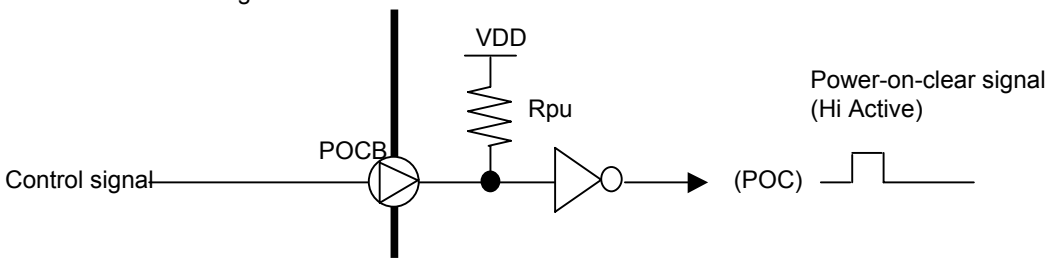
Serial Communication Prohibition Period



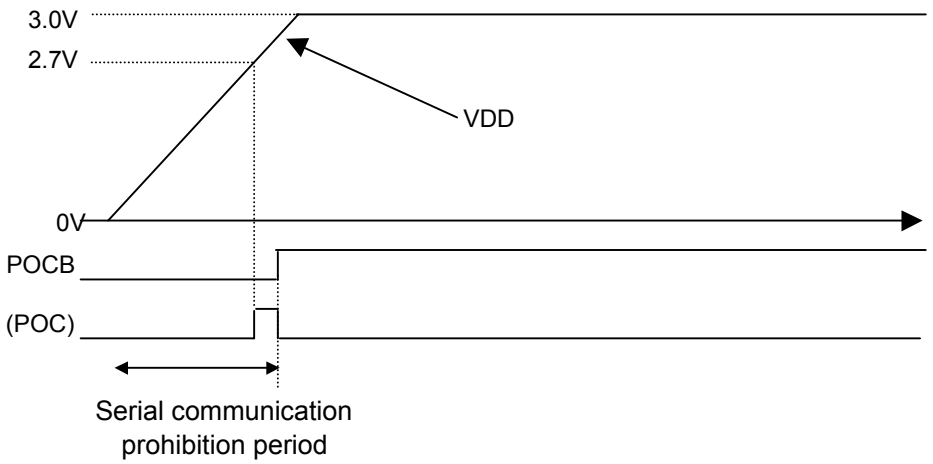
Note1: All logic input signals are ignored during input period (POC is Hi).
POC changes and remains "Lo" when POCB is between 1.107V and 2.592V.

In case of rapid startup after power-on, directly control POCB terminal.

Power-on-clear circuit diagram



In case of directly controlling POCB terminal, POCB terminal should be set to "Lo" at Power-on
POCB should be changed to "Hi" after VDD is exceeding 2.7V.
Serial communication is prohibited while POCB is "Lo".



8.6 Other Functions

Free-run Function

When HSYNC or VSYNC is not supplied for a certain period of time, white luster display (FFh) is automatically displayed on the screen to prevent "burn-in" by internally producing signals equivalent to HSYNC and VSYNC.
Free-run function is activated on the following condition.

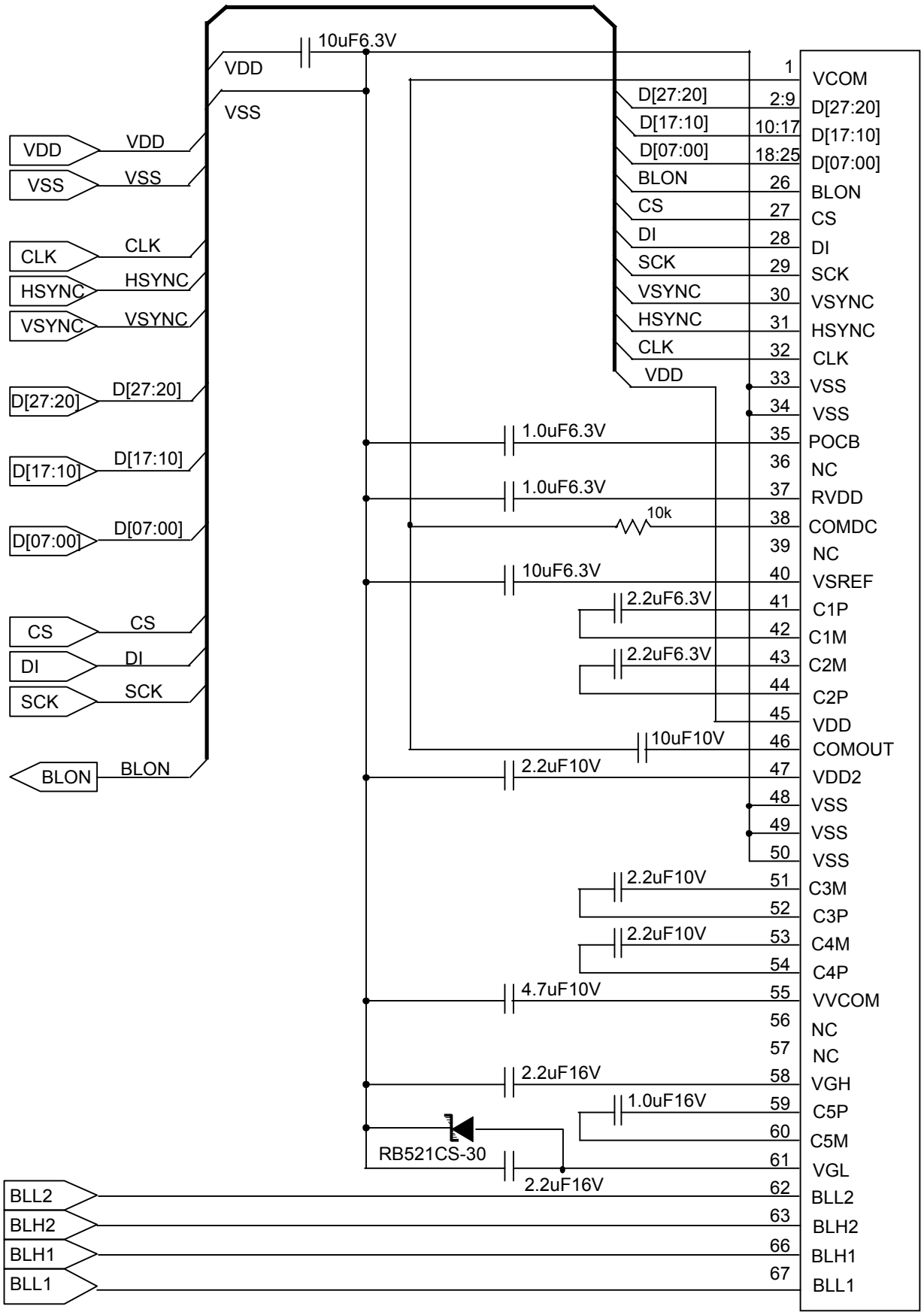
- No HSYNC input for 4096CLK period.
- No VSYNC input for 512H period.

Normal display resumes from free-run by a supply of HSYNC and VSYNC pulses.

- Built-in Panel Residual Charge Reduction Circuit

When the power turns off in accordance with the mandatory procedure described in the section "8.4 Standby (Power save) Sequence", afterimage treatment is carried out after standby mode is set.
This circuit automatically reduces panel's residual charge and prevents afterimage for a long time even if standby mode setting fails to be made before power-off.

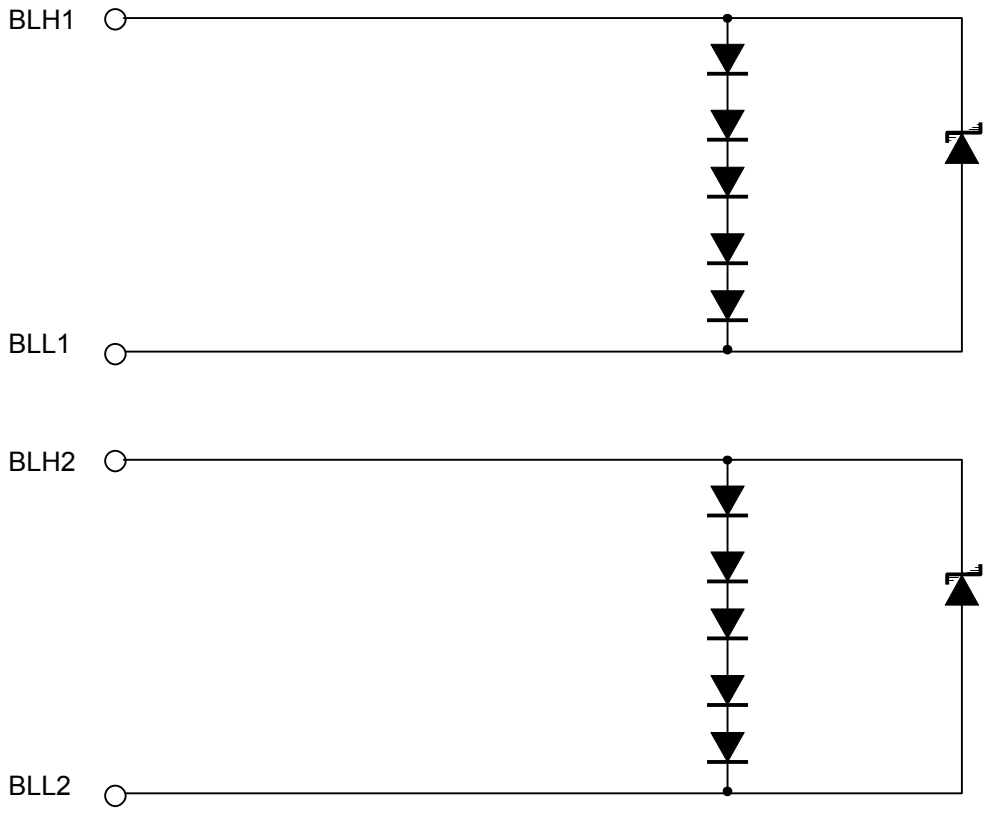
9. CIRCUIT
9.1 Reference Circuit Design



TFT LCD MODULE REFERENCE CIRCUIT

This circuit is solely for reference purpose and optimum circuit and components values may be different. User's due consideration and evaluation must be given to this circuit design and component values prior to their intended use.

9.2 LED Circuit



10. CHARACTERISTICS

10.1 Optical Characteristics

< Measurement Condition >
Measuring instruments: CS1000(KONICA MINOLTA), LCD7000(OTSUKA ELECTRONICS)
Driving condition: VDD = 3.0V, VSS = 0V
Optimized Vcom/c
VLCD=(Vsigpp±Vcompp)/2
Backlight: IL=20.0mA
Measured temperature: Ta ＝ 25°C

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Note No.	Remark
Response time	Rise time	TON	VLCD= 0.69V→3.87V	—	—	40	ms	1	*
	Fall time	TOFF	VLCD= 3.87V→0.69V	—	—	60	ms		
Contrast ratio		CR	VLCD= 0.69V/3.87V	60	—	—		2	
Viewing angle	Left	θL	VLCD= 0.69V/3.87V CR≧10	40	—	—	deg	3	*
	Right	θR		40	—	—	deg		
	Up	φU		20	—	—	deg		
	Down	φD		70	—	—	deg		
V-T threshold voltage		V90		1.0	1.3	1.6	V	4	*
		V50		1.5	1.8	2.1	V		
		V10		2.0	2.3	2.6	V		
White V-T Curve				Refer to Fig. 3: White V-T Curve					Reference
White Chromaticity		x	VLCD=0.69V	Fig. 4: White chromaticity range				5	
		y							
Max. Contrast angle		CRφ		2	9	16	deg	6	Downward *
Burn-in				No noticeable burn-in image should be observed after 2 hours				7	At optimized VCOMDC
Brightness at the screen center			VLCD=0.69V	300	450	—	cd/m^2	8	
Brightness distribution			VLCD=0.69V	70	—	—	%	9	

* Note number 1 to 9: Refer to the APPENDIX of "Reference Method for Measuring Optical Characteristics".
* Measured in the form of LCD module.

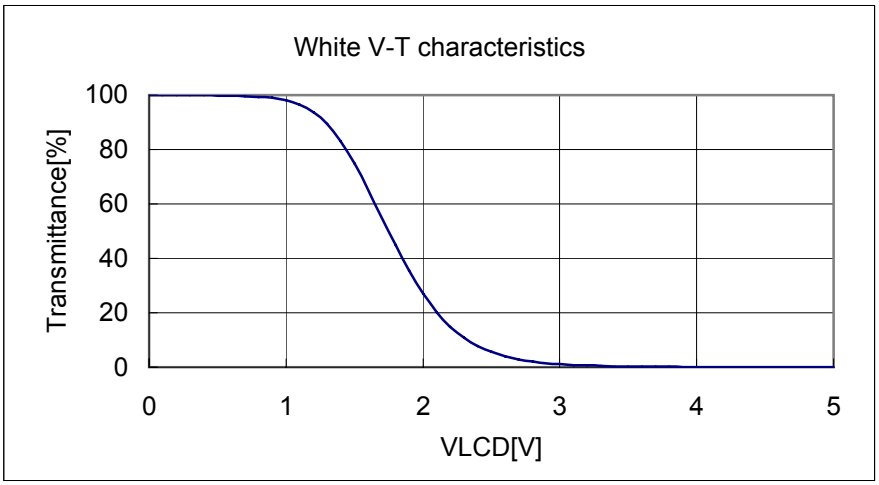
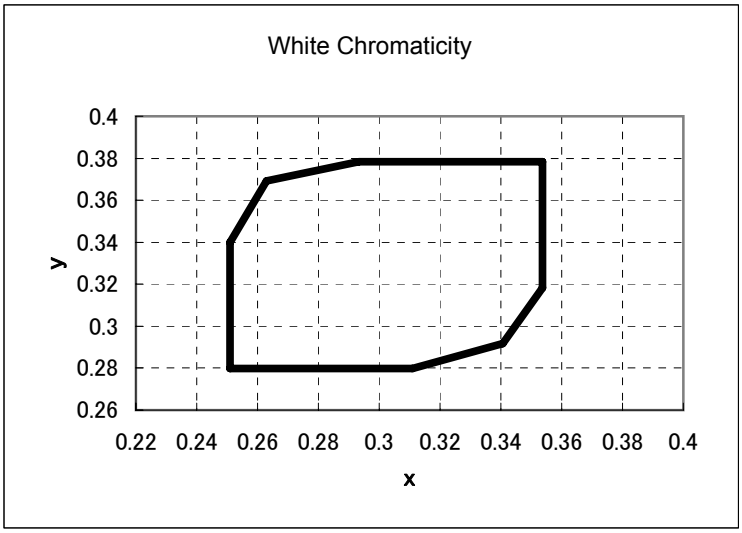


Fig. 3: White V-T Curve



【White Chromaticity Range】

x	y
0.251	0.280
0.251	0.340
0.263	0.369
0.293	0.378
0.354	0.378
0.354	0.318
0.341	0.292
0.311	0.280

Fig. 4: White Chromaticity Range

10.2 Temperature Characteristics

< Measurement Condition >
Measuring instruments: CS1000（KONICA MINOLTA）, LCD7000(OTSUKA ELECTRONICS)
Driving condition: VDD = 3.0V, VSS = 0V
Optimized Vcom/c
VLCD=（Vsigpp±Vcompp）/2
Backlight: IL=20.0mA

Item			Specification		Remark
			Ta＝－10°C	Ta＝70°C	
Contrast ratio		CR	40 or more	40 or more	
Response time	Rise time	TON	200 msec or less	30 msec or less	
	Fall time	TOFF	200 msec or less	50 msec or less	
Display Quality			No noticeable display defect or ununiformity should be observed.		Use the criteria for judgment specified in the

11. CRITERIA OF JUDGMENT

11.1 Defective Display and Screen Quality

Test Condition: Observed TFT-LCD monitor from front during operation with the following conditions

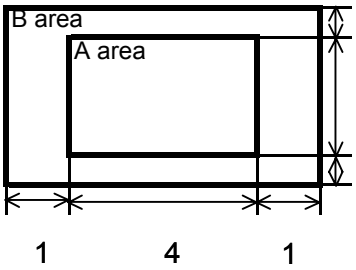
Driving Signal	Raster Patter (RGB in monochrome, white, black)
Signal condition	VLCD:0.69V,1.75V,3.87V(3steps)
Observation distance	30 cm
Illuminance	200 to 350 lx
Backlight	IL = 20.0 mA

Defect item		Defect content			Criteria
Display Quality	Line defect	Black, white or color line, 3 or more neighboring defective dots			Not exists
	Dot defect	Uneven brightness on dot-by-dot base due to defective TFT or CF, or dust is counted as dot defect (brighter dot, darker dot) High bright dot: Visible through 2% ND filter at VLCD=3.87V Low bright dot: Visible through 5% ND filter at VLCD=3.87V Dark dot: Appear dark through white display at VLCD=1.75V			Refer to table 1
Screen Quality	Dirt	Point-like uneven brightness (white stain, black stain etc)			Invisible through 1% ND filter
	Foreign particle	Dust in the gap between the LCD panel and the backlight	Point-like	0.25mm<φ	N=0
				0.20<φ≦0.25mm	N≦2
				0.15<ϕ≦0.20mm	N≦3
				φ≦0.15mm	Ignored
			Liner	3.0mm<length, 0.08mm<width	N=0
				length≦3.0mm, width≦0.08mm	Ignored
	Others				Use boundary sample for judgment when necessary

φ(mm): Average diameter = (major axis + minor axis)/2
Permissible number: N

Table 1

Model	Area	High bright	Low bright	Dark dot	Total	Criteria
COM41T4129GLC	A	0	2	2	3	Permissible distance between same color bright dots (includes neighboring dots): 3 mm or more Permissible distance between same color high bright dots (includes neighboring dots): 5 mm or more
	B	2	4	4	6	
	Total	2	4	4	7	



Division of A and B areas
B area: Active area
Dimensional ratio between A and B areas: 1: 4: 1 (Refer to the left figure)

11.2 Screen & Other Appearance

Testing conditions

Illuminance	1200～2000 lx
Observation distance	30cm

Item		Criteria	Remark
Polarizer	Flaw Stain Bubble Dust Dent	Ignore invisible defect when the backlight is on.	Applicable area: Active area only (Refer to the section 3.2 "Outward form")
S-case		No functional defect occurs	
FPC cable		No functional defect occurs	

12. RELIABILITY TEST

Test item		Test condition	number of failures /number of examinations
Durability test	High temperature storage	Ta=80°C 240H	0／3
	Low temperature storage	Ta=-30°C 240H	0／3
	High temperature & high humidity test	Ta=60°C, RH=90% 240H non condensing ※	0／3
	High temperature operation	Tp=70°C 240H	0／3
	Low temperature operation	Tp=-20°C 240H	0／3
	High temp & humid operation	Tp=40°C, RH=90% 240H non condensing ※	0／3
	Thermal shock storage	-30←→80°C(30min/30min) 100 cycles	0／3
Mechanical environmental test	Electrostatic discharge test (Non operation)	Confirms to EIAJ ED-4701 C-111 C=200pF,R=0Ω,V=±200V Each 3 times of discharge on and power supply and other terminals.	0／3
	Surface discharge test (Non operation)	C=250pF, R=100Ω, V=±12kV Each 5 times of discharge in both polarities on the center of screen with the case grounded.	0／3
	Vibration test	Total amplitude 1.5mm, f=10 ～55Hz, X,Y,Z directions for each 2 hours	0／3
	FPC tensile test	Pull the FPC with the force of 3N for 10 sec. in the direction +/- 90-degree to its original direction.	0／3
	FPC bend test	Pull the FPC with the force of 3N for 10 sec. in the direction +/-180-degree to its original direction. Repeat it 3 times.	0／3
	Impact test	Use CASIO original jig (see next page)and make an impact with peak acceleration of 1000m/s^2 for 6 msec with half sine-curve at 3 times to each X, Y, Z directions in conformance with JIS 60068-2-27-1995.	0／3
Packing test	Packing vibration-proof test	Acceleration of 19.6m/s^2 with frequency of 10→55→10Hz, X,Y, Zdirection for each 30 minutes	0／1 Packing
	Packing drop test	Drop from 75cm high. 1 time to each 6 surfaces, 3 edges, 1 corner	0／1 Packing

Note:Ta=ambient temperature Tp=Panel temperature

※ The profile of high temperature/humidity storage and High Temperature/humidity operation (Pure water of over 10MΩ·cm shall be used.)

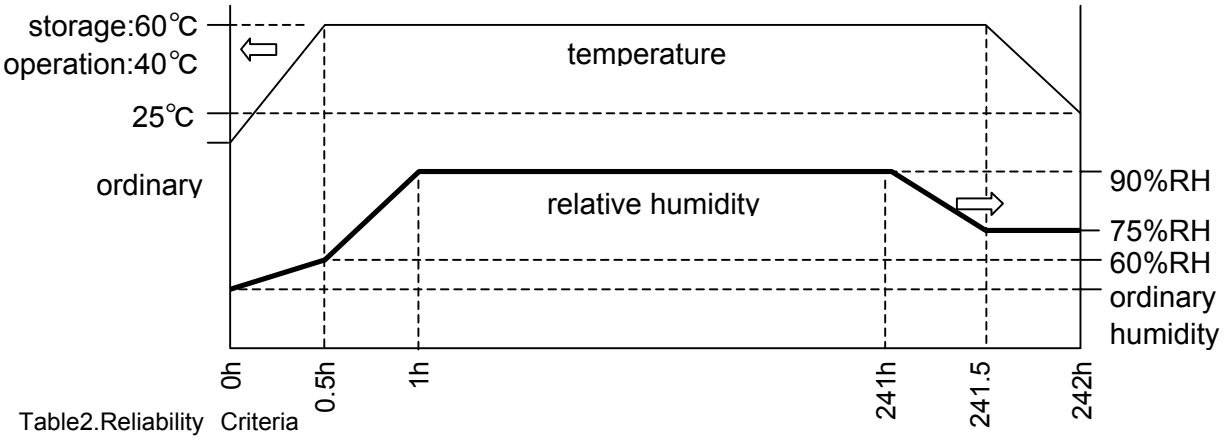
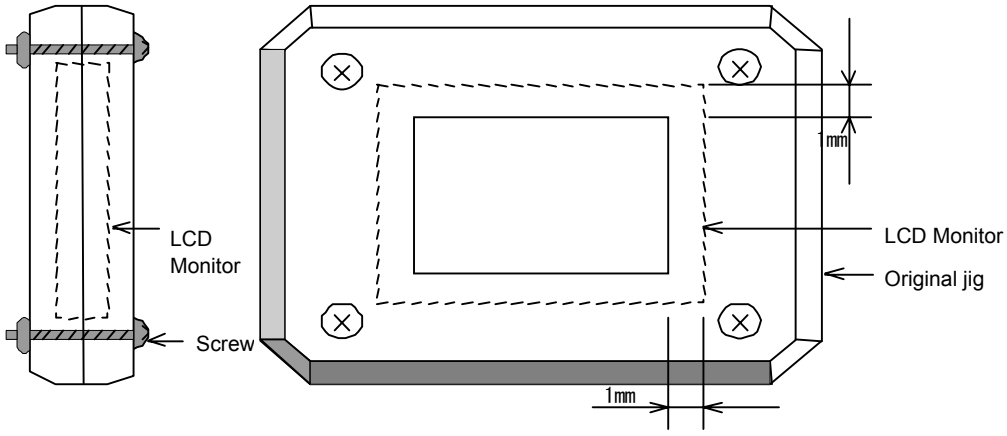


Table2.Reliability Criteria

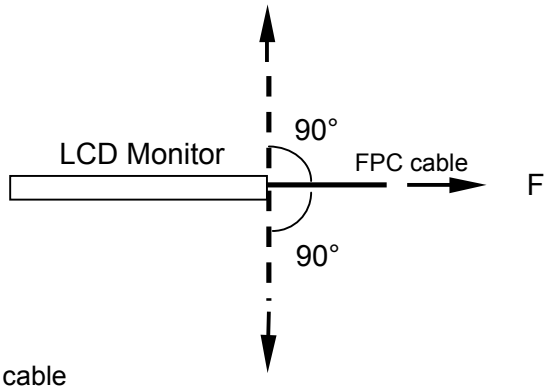
Measure the parameters after leaving the monitor at the ordinary temperature for 2 hours or more after the test completion.

item	Standard	Remarks
Display quality	No visible abnormality shall be seen.	As criteria of 11"CRITERIA OF JUDGMENT".
Contrast ratio	40 or more	

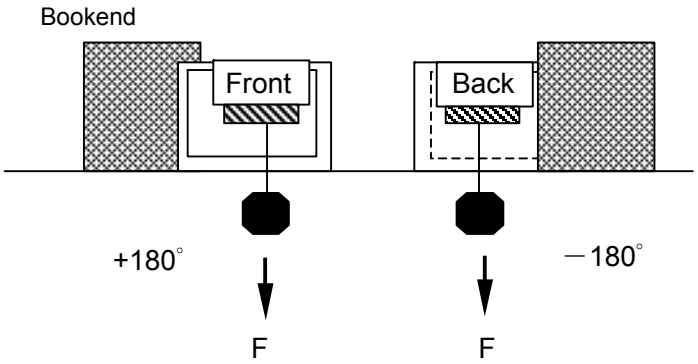
CASIO Original Jig



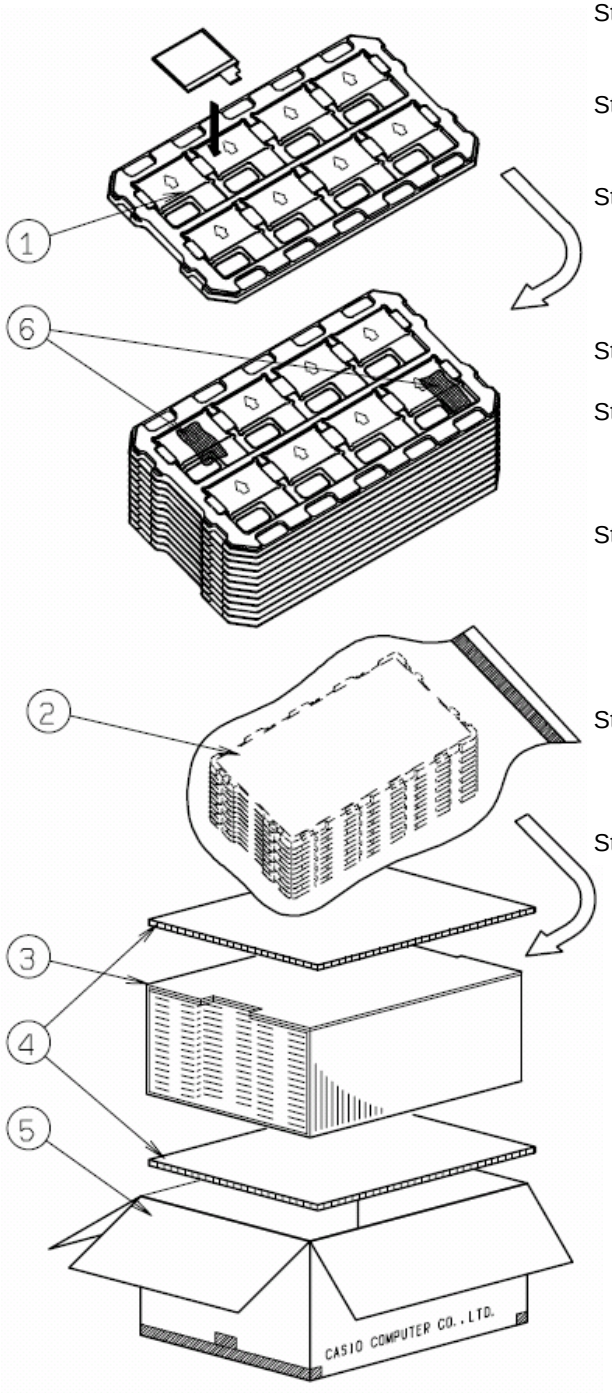
Tension Test Method for FPC cable



Bend Test Method for FPC cable



13. PACKING SPECIFICATIONS



Step 1. Each product is to be placed in one of the cut-outs of the tray with the display surface facing upward.
(8 products per tray)

Step 2. Each tray needs to be same orientation respect to the tray below or above it and the trays be in a stack of 10.
One empty tray is to be put on the top of stack of 10 trays.

Step 3. 2 packs of moisture absobers are to be placed on the top tray as shown in the drawing.
Put piled trays into a sealing bag.
Vacuum and seal the sealing bag with the vacuum sealing machine.

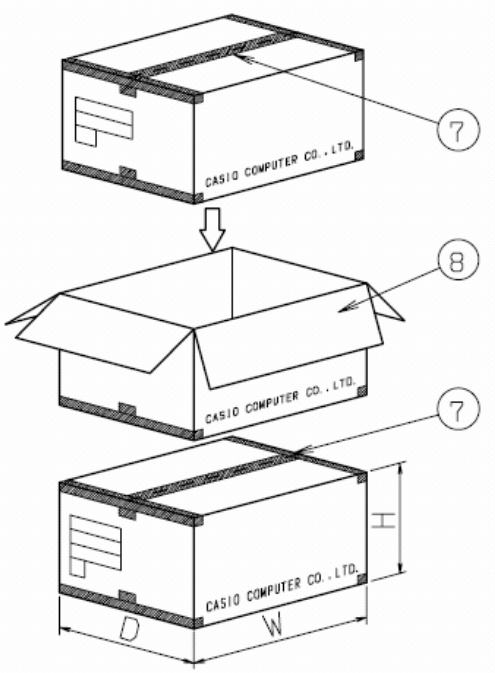
Step 4. The stack of trays in the plastic back is to be inserted into a inner carton.

Step 5. A corrugated board is to be placed on the top and on the bottom of the inner carton.
The two corrugated boards and the inner carton is to be inserted into an outer carton.

Step 6. The outer carton needs to sealed with packing tape as shown in the drawing.
The model number, quantity of products, and shipping date are to be printed on the outer carton.
If necessary, shipping labels or impression markings are to be put on the outer carton.

Step 7. The outer carton is to be inserted into a extra outer carton with same direction.
The extra outer carton needs to sealed with packing tape as shown in the drawing.

Step 8. The model number, quantity of products, and shipping date



Remark: The return of packing materials is not required.

Packing item name		Specs., Material
①	Tray	PP
②	Sealing bag	
③	Inner carton	Corrugated cardboard
④	Inner board	Corrugated cardboard
⑤	Outer carton	Corrugated cardboard
⑥	Drier	Moisture absorber
⑦	Packing tape	
⑧	Extra outer carton	Corrugated cardboard

Dimension of extra outer carton
D : Approx. (338mm)
W : Approx. (549mm)
H : Approx. (198mm)
Quantity of products packed in one carton 80
Gross weight : Approx. 6.6Kg

14. HANDLING INSTRUCTION

14.1 Cautions for Handling LCD panels

Caution

(1) Do not make an impact on the LCD panel glass because it may break and you may get injured from it.

(2) If the glass breaks, do not touch it with bare hands.
(Fragment of broken glass may stick you or you cut yourself on it.

(3) If you get injured, receive adequate first aid and consult a medial doctor.

(4) Do not let liquid crystal get into your mouth.
(If the LCD panel glass breaks, try not let liquid crystal get into your mouth even toxic property of liquid crystal has not been confirmed.

(5) If liquid crystal adheres, rinse it out thoroughly.
(If liquid crystal adheres to your cloth or skin, wipe it off with rubbing alcohol or wash it thoroughly with soap. If liquid crystal gets into eyes, rinse it with clean water for at least 15 minutes and consult an eye doctor.

(6) If you scrape this products, follow a disposal standard of industrial waste that is legally valid in the community, country or territory where you reside.

(7) Do not connect or disconnect this product while its application products is powered on.

(8) Do not attempt to disassemble or modify this product as it is precision component.

(9) A part of soldering part has been exposed, and avoid contact (short-circuit) with a metallic part of the case etc. about FPC of this model, please.
Please insulate it with the insulating tape etc. if necessary.
The defective operation is caused, and there is a possibility to generation of heat and the ignition.

Caution **This mark is used to indicate a precaution or an instruction which, if not correctly observed, may result in bodily injury, or material damages alone.**

14.2 Precautions for Handling

1) Wear finger tips at incoming inspection and for handling the TFT monitors to keep display quality and keep the working area clean.
Do not touch the surface of the polarizer as it is easily scratched.

2) Wear grounded wrist-straps and use electrostatic neutralization blowers to prevent static charge and discharge when handling the TFT monitors as the LED in this TFT monitors is damageable to electrostatic discharge,
Properly set up equipment, jigs and machines, and keep working area clean and tidy for handling the TFT monitors.

3) Avoid strong mechanical shock including knocking, hitting or dropping to the TFT monitors for protecting their glass parts. Do not use the TFT monitors that have been experienced dropping or strong mechanical shock.

4) Do not use or storage the TFT monitors at high temperature and high humidity environment.
Particularly, never use or storage the TFT monitors at a location where condensation builds up.

5) Avoid using and storing TFT monitors at a location where they are exposed to direct sunlight or ultraviolet rays to prevent the LCD panels from deterioration by ultraviolet rays.

6) Do not stain or damage the contacts of the FPC cable .
Otherwise, it may cause poor contact or deteriorate reliability of the FPC cable.

7) Do not bend or pull the FPC cable or carry the TFT monitor by holding the FPC cable.

8) Peel off the protective film on the TFT monitors during mounting process.
Refer to the section 14.5 on how to peel off the protective film.
We are not responsible for electrostatic discharge failures or other defects occur when peeling off the protective film.

14.3 Precautions for Operation

1) Since this TFT monitors are not equipped with light shielding for the driver IC,
do not expose the driver IC to strong lights during operation as it may cause functional failures.

2) When driving the monitor,refer to "8.4 Standby (Power Save) Sequence".
When turning off the power,turn off the input signal before or at the same timing of switching off the power.

3) Optimize Vcom/C within recommended operating conditions.
* When Vcom/c is not an optimal value, flicker and image sticking will be occuerd.

4) Do not plug in or out the FPC cable while power supply is switch on.
Plug the FPC cable in and out while power supply is switched off.

5) Do not operate the TFT monitors in the strong magnetic field. It may break the TFT monitors.

6) Do not display a fixed image on the screen for a long time.
Use a screen-saver or other measures to avoid a fixed image displayed on the screen for a long time. Otherwise, it may cause burn-in image on the screen due the characteristics of liquid crystal.

14.4 Storage Condition for Shipping Cartons

Storage environment

- Temperature: 0 to 40˚C
- Humidity: 60%RH or less
  No-condensing occurs under low temperature with high humidity condition.
- Atmosphere: No poisonous gas that can erode electronic components and/or wiring materials should be detected.
- Time period: 3 months
- Unpacking: To protect the TFT monitors from static damage during unpacking, keep room humidity more than 50%RH and implement effective countermeasures against static electricity such as establishing a ground (an earth) before unpacking.
- Maximum piling up: 7 cartons

14.5 Precautions for Peeling off the Protective film

The followings work environment and work method are recommended to prevent the TFT monitors from static damage or adhesion of dust when peeling off the protective films.

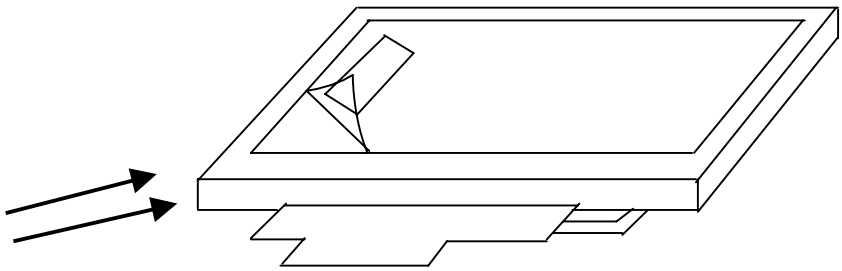
A) Work Environment

a) Humidity: 50 to 70 %RH, Temperature15˚C to 27˚C
b) Operators should wear conductive shoes, conductive clothes, conductive finger tips and grounded wrist-straps. Anti-static treatment should be implemented to work area's floor.
c) Use a room shielded against outside dust with sticky floor mat laid at the entrance to eliminate dirt.

B) Work Method

The following procedures should taken to prevent the driver ICs from charging and discharging.

a) Use an electrostatic neutralization blower to blow air on the TFT monitors to its lower left when the FPC cable is facing to the downside.
Optimize direction of the blowing air and the distance between the TFT monitors and the electrostatic neutralization blower.
b) Put an adhesive tape (Scotch tape, etc) at the lower left corner area of the protective film to prevent scratch on the touch panel.
c) Peel off the adhesive tape slowly (spending more than 2 secs to complete) by pulling it to opposite direction.



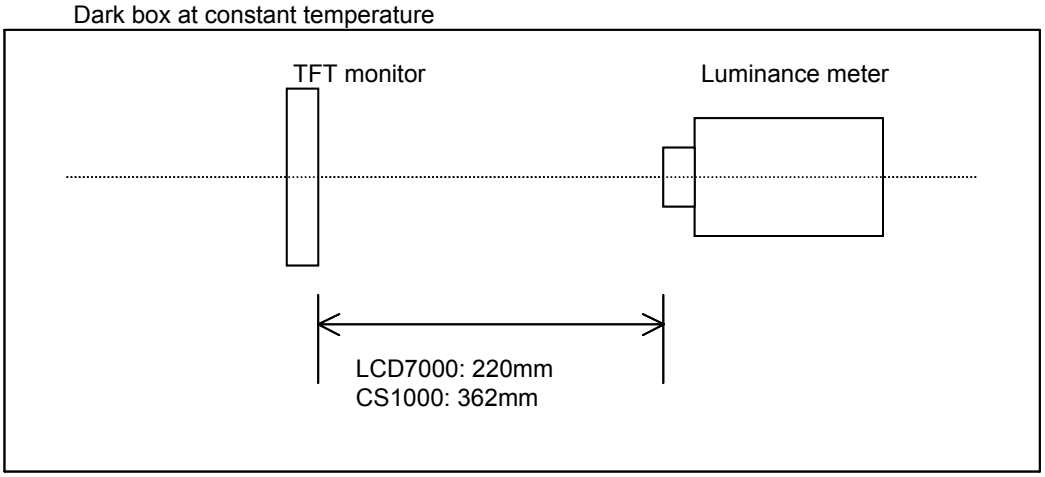
Direction of blowing air
(Optimize air direction and the distance)

APPENDIX

Reference Method for Measuring Optical Characteristics and Performance

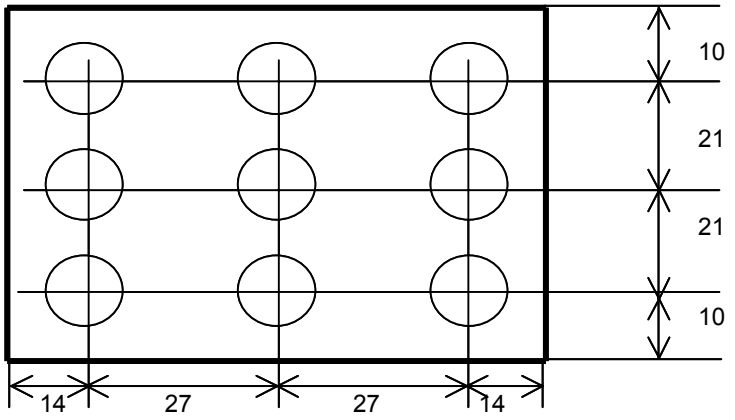
1. Measurement Condition

Measuring instruments:	CS1000（KONICA MINOLTA）, LCD7000(OTSUKA ELECTRONICS)
Driving condition:	Refer to the section 10.1 "Optical Characteristics"
Measured temperature:	25˚C unless specified
Measurement system:	See the chart below. The luminance meter is placed on the normal line of measurement system.
Measurement point:	At the center of the screen unless otherwise specified



Measurement is made after 30 minutes of lighting of the backlight.

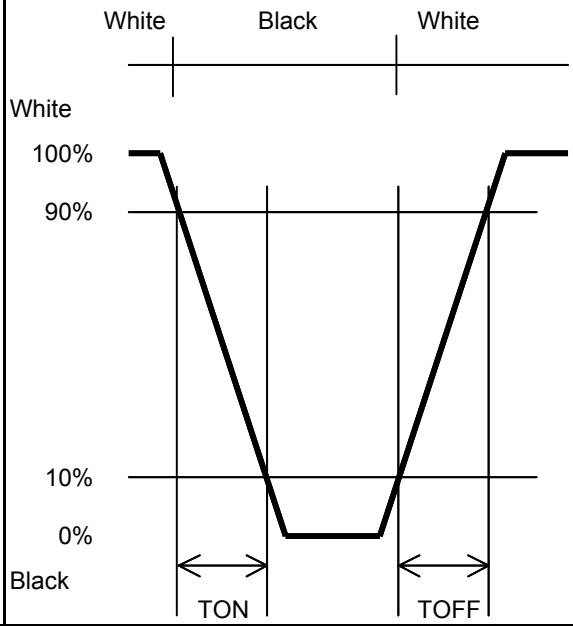
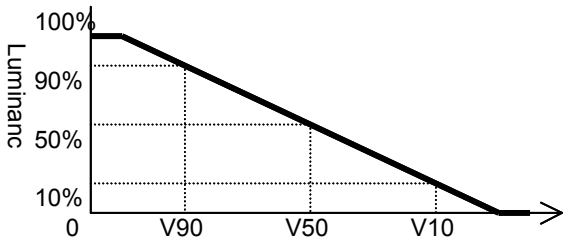
Measurement point: At the center point of the screen
Brightness distribution: 9 points shown in the following drawing.



Unit: mm

Backlight IL = 20.0mA

2. Test Method

Notice	Item	Test method	Measuring instrument	Remark
1	Response time	Measure output signal waveform by the luminance meter when raster of window pattern is changed from white to black and from black to white. 	LCD7000	Black display VLCD=3.87V White display VLCD=0.69V TON Rise time TOFF Fall time
2	Contrast ratio	Measure maximum luminance Y1(VLCD=0.69V) and minimum luminance Y2(VLCD=3.87V) at the center of the screen by displaying raster or window pattern. Then calculate the ratio between these two values. Contrast ratio = Y1/Y2 Diameter of measuring point: 8mmφ	CS1000	
3	Viewing angle Horizontalθ Verticalφ	Move the luminance meter from right to left and up and down and determine the angles where contrast ratio is 10.	LCD7000	
4	V-T threshold value	Change VLCD by 0.1V step and plot the points where the luminance is 90% as V90, 50% as V50 and 10% as V10 of maximum luminance. 	LCD7000	
5	White chromotica	Measure chromaticity coordinates x and y of CIE1931colorimetric system at VLCD = 0.69V Color matching faction: 2°view	CS1000	

Notice	Item	Test method	Measuring instrument	Remark
6	Maximum contrast angle	Move the luminance meter vertically to the display from its normal line and measure the angles where contrast ratio reaches its highest value.	LCD7000	
7	Burn-in	Visually check burn-in image on the screen after 2 hours of "window display" (VLCD=0.69V/3.87V).		At optimized Vcom/C
8	Center brightness	Measure the brightness at the center of the screen.	CS1000	
9	Brightness distribution	(Brightness distribution) = 100 x B/A % A : max. brightness of the 9 points B : min. brightness of the 9 points	CS1000	