Doc. Number:

■ Tentative Specification
☐ Preliminary Specification
☐ Approval Specification

MODEL NO.: WJ014ZE-02A

Customer:

APPROVED BY **SIGNATURE**

Name / Title _____ _____
Note

_____
Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By

- CONTENTS -

REVISION HISTORY

Version	Date	Page	Description
Ver 0.0	May.26 ,2017	All	Spec Ver.0.0 was first issued..

1. PURPOSE

WJ014ZE-02A is a color active matrix of Organic Light-Emitting Diode (OLED), which uses Low Temperature Poly-silicon (LTPS) as switching devices. This panel has a 1.39 inches diagonally measured active display area with 400 x 400 resolutions. This product is composed of a LTPS-AMOLED panel, Polarizer, driver IC(COF) and FPCa. The following describes the features of this product.

2. FEATURES

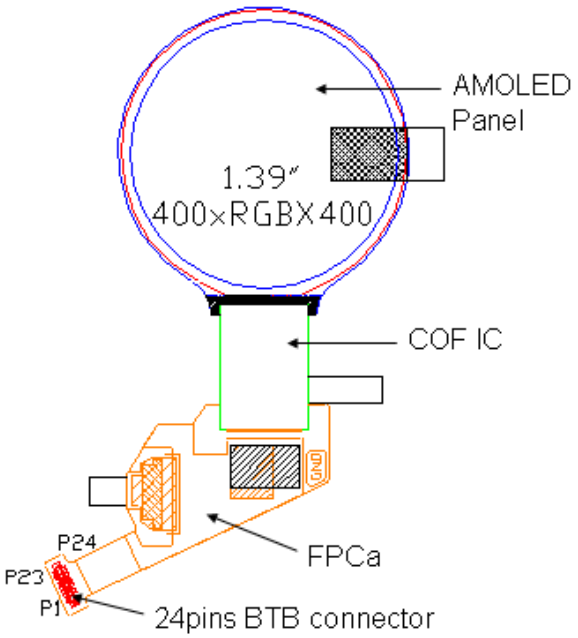
- 1.39” (diagonal) inch configuration
- 400xRGBX400 resolution
- 287 PPI

3. GENERAL RULES OF SINGLE PANEL

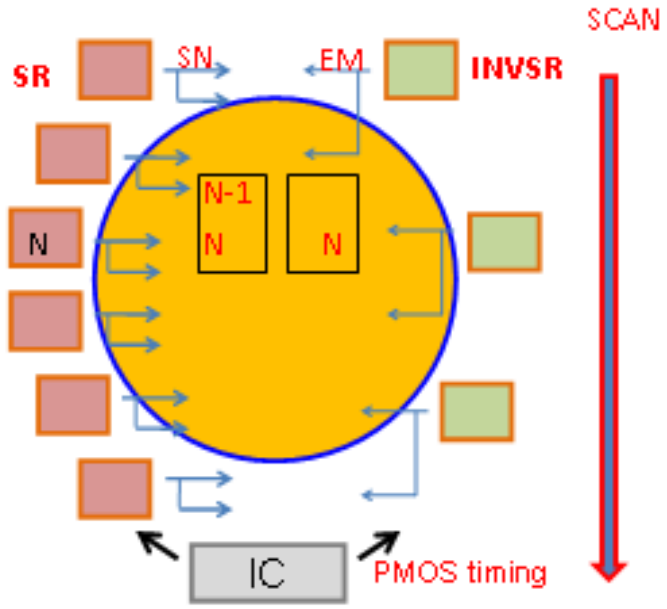
3-1 Physical Specification

No.	Item	Specification	Unit
1	Screen Size	1.39 (Diameter)	inch
2	Display Resolution	400 x 400	pixel
3	Pixel Pitch	0.0885 (H) x 0.0885 (V)	mm
4	Active Area	35.4mm (Diameter)	mm
5	Outline Dimension	38.6 (H) × 40.5(V) × 0.71(T) w/o FPCa	mm
6	Pixel Configuration	RGB-SBS	--
7	Color Depth	8/8/8	colors
8	Display Type	Color OLED	--
9	Interface Type	MIPI	--
10	Surface Treatment	NA	--
12	Weight	1.5	g

3-2 Module Appearance



3-3 Panel Scan Direction



4. ABSOLUTE MAXIMUM RATING

(Ta = 25 ± 2℃)

Item	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VCI	-0.3	5.5	V	Power for digital circuit
Interface supply voltage	VDDIO	-0.3	5.5	V	Power for Interface circuit
ELVDD power supply	PVDD	-	5.0	V	Power for OLED
ELVSS power supply	PVEE	-5.0	-	V	Power for OLED
Storage temperature	Tstg	-30	+70	℃	
Operating Temperature	Topr	-20	+60	℃	

Note:

(1) All of the voltages listed above are with respective to GND= 0V

(2) Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

5. ELECTRICAL CHARICTERISTICS

5-1. Operating Conditions:

(Ta = 25 ± 2℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Driver driving voltage	VCI	2.7	2.8	3.6	V	(1)
	VDDIO	1.65	1.8	3.3	V	(1)
OLED driving voltage	PVDD	4.55	4.60	4.65	V	(1)(2)
	PVEE	-2.35	-2.40	-2.45	V	(1)

Note:

(1) The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

(2)RT4723 Positive output voltage = 4.6V ± 0.8% at $-40℃ \leqq Ta \leqq +85℃$

5-2. Power Consumption:

(Ta = 25 ± 2℃, VDDIO=1.8,VCI=2.8V)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Normal Mode	P_{Normal}				mW	(1)
Standby Mode	$P_{Standby}$				mW	-

Note: (1) White pattern.

6. DC CHARACTERISTICS

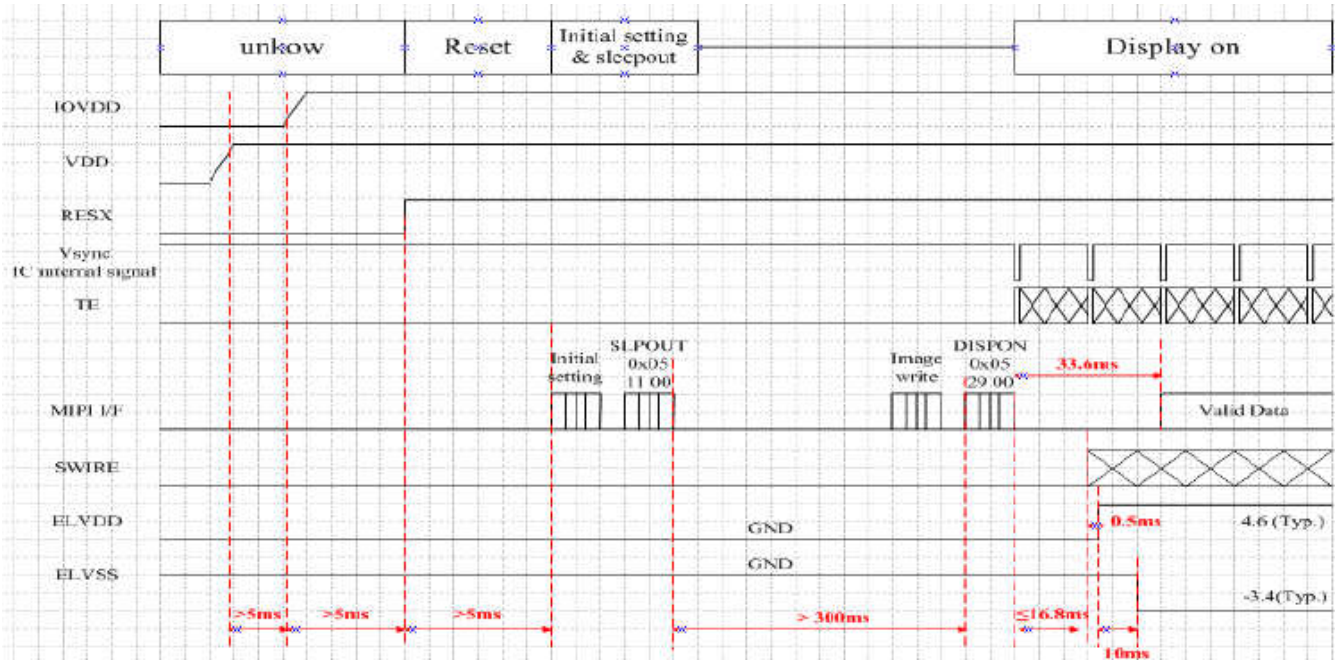
6.1 Parameter

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
High Level Input Voltage	VIH	VDDIO=1.65~3.3V	0.8xVDDIO		VDDIO	V	
Low Level Input Voltage	VIL	VDDIO=1.65~3.3V	0		0.2xVDDIO	V	
Input Leakage Current	IL1	Vi= 0 ~ VDDIO	-1		+1	uA	
VGH output voltage	VGH		7	7	18	V	
VGL output voltage	VGL		-8	-8	-18	V	

(Ta = 25 ± 2℃)

6.2 Power Sequence

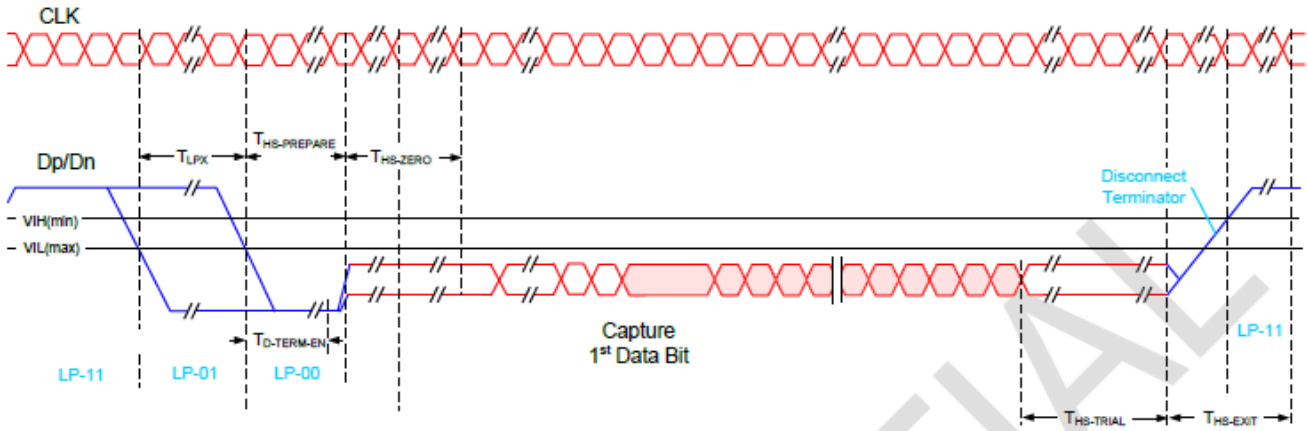
Power on sequence



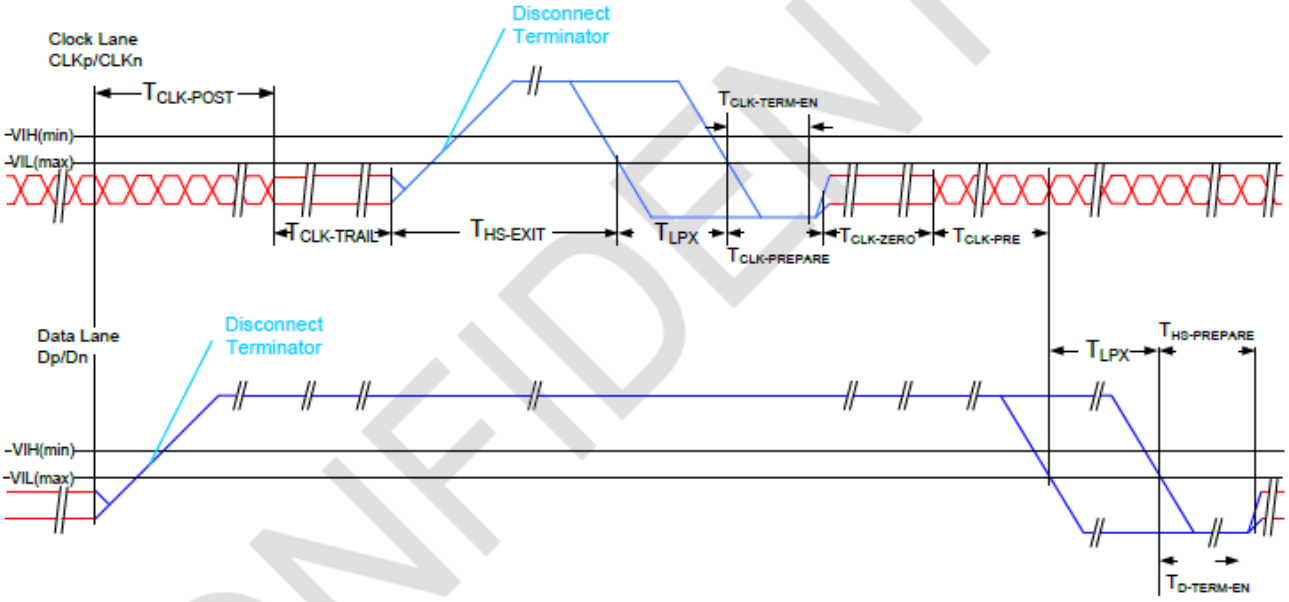
7. AC CHARCTERISTICS

7.1. MIPI Interface Characteristics

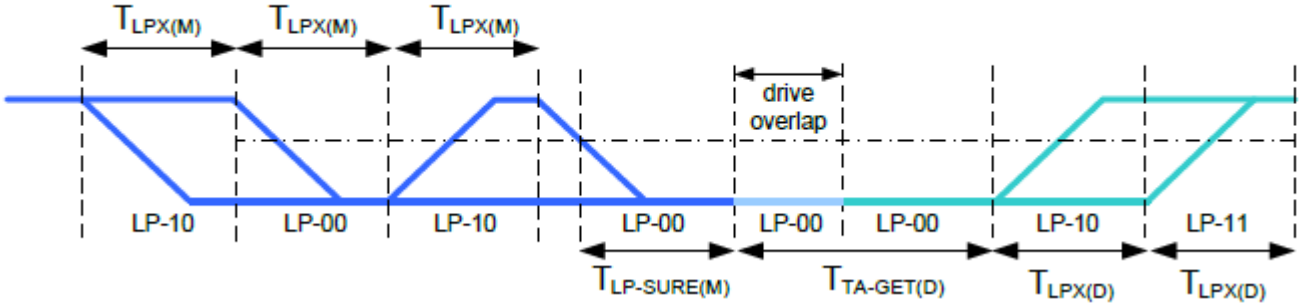
HS Data Transmission Burst



➢ HS clock transmission



Turnaround Procedure

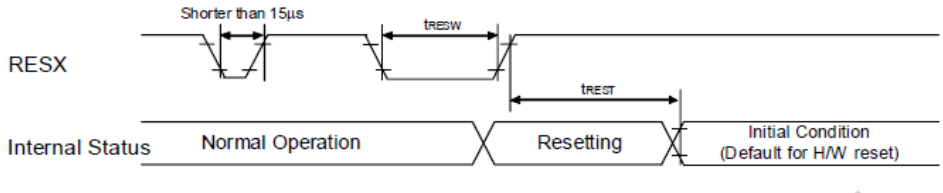


Timing Parameters: Parameter	Description	Min	Typ	Max	Unit
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL .	60ns + 52*UI			ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	300			ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX .	Time for Dn to reach VTERM-EN		38	ns
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX .	Time for Dn to reach VTERM-EN		35 ns +4*UI	
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		60 ns + 6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns

THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns+4*UI			ns
TLPX(M)	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns
TTA-SURE(M)	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX(M)		2*TLPX(M)	ns
TLPX(D)	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns
TTA-GET(D)	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	5*TLPX(D)			ns
TTA-GO(D)	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	4*TLPX(D)			ns
TTA-SURE(D)	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX(D)		2*TLPX(D)	ns

7.2. Display RESET Timing Characteristics

Reset input timing



IOVDD=1.65 to 1.95V, VDD=2.8 to 3.1V, AGND=DGND=0V, Ta=-40 to 85° C

Timing Parameters

Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
tRESW	*1) Reset low pulse width	RESX	10	-	-	-	us
tREST	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-			120	When reset applied during Sleep out mode	ms

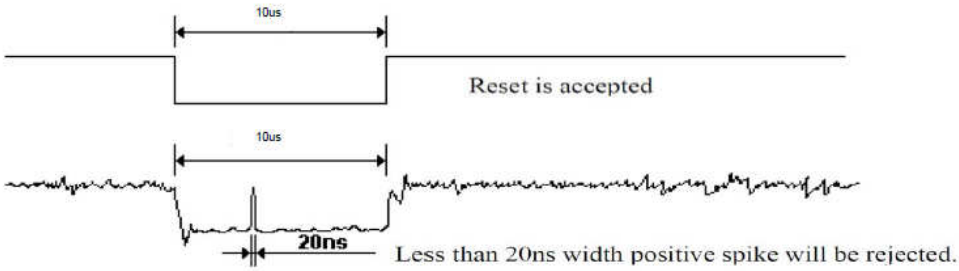
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 s	Reset Rejected
Longer than 10 s	Reset
Between 5 s and 15 s	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. OPTICAL CHARCTERISTICS

(Ta = 25 ± 2℃,)

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Transmittance	T%							
Viewing Angle CR>1600	Top		-	80	-	-	Degree	Note 8-3
	Bottom			80	-	-		
	Left			80	-	-		
	Right			80	-	-		
Response Time	Tr+Tf		Θ=0°	-	<4	-	ms	Note 8-8
Contrast Ratio	CR		Θ=0°	10,000	-	-	-	Note 8-3
Luminance	L		Θ=0°	285	300	-	cd/m^2	Note 8-5
NTSC	-		-	85	100	-	%	Note 8-7
Uniformity	-		-	-	-	-	%	Note 8-6
Chromaticity	White	x	Θ=0°	0.27	0.30	0.33	-	Chromaticity
		y		0.28	0.31	0.34		
	Red	x		0.64	0.67	0.70		
		y		0.30	0.33	0.36		
	Green	x		0.19	0.24	0.29		
		y		0.67	0.72	0.77		
	Blue	x		0.09	0.13	0.17		
		y		0.025	0.065	0.105		
Gamma	-		-		2.2	2.4		

Above measuring is panel only.

Note 8

8.1 Definition of viewing angle range

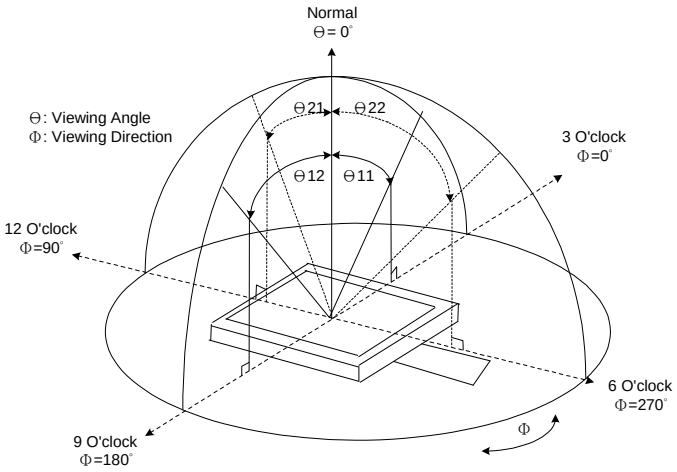


Fig. 8-1 Definition of viewing angle

8.2 Measuring setup:

The module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting for 20 minutes in a windless room.

8.2.1 Driving voltage

ELVDD= 4.6V, ELVSS=-2.4V

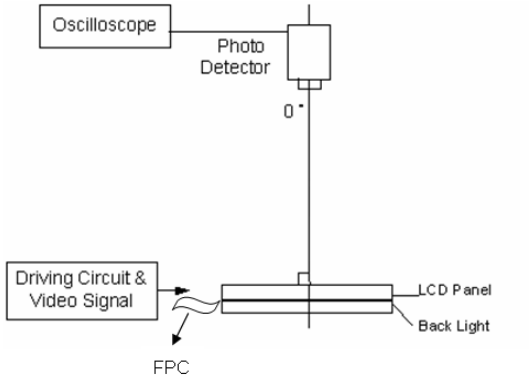
8.2.2 Ambient temperature: Ta=25℃

8.2.3 Testing point: measure in the display center point and the test angle Θ=0°

8.2.4 Testing Facility

Environmental illumination: ≤ 1 Lux

A. System A (DMS 900 series)



B. System B (SR3)

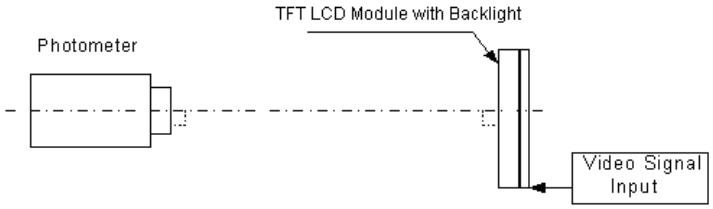


Fig. 8-2 Optical measurement system setup

8-3: Contrast ratio

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

8-4: Chromaticity and NTSC

Test Point: Display Center

8-5: Luminance

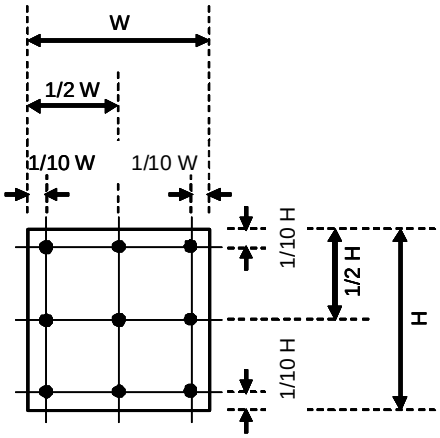
The measurement shall be done at the center of the display with a full white image.

8-6: Uniformity

The luminance of 9 points as the black dot in the figure shown below is measured and the uniformity is defined as the formula:

*

$$\text{Uniformity} = \frac{\text{The minimum luminance among 9 points}}{\text{The maximum luminance among 9 points}}$$

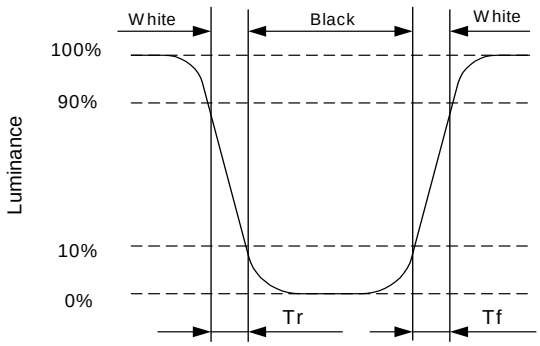


Active Area (W x H)

8-7: Chromaticity and NTSC

Test Point: Display Center

8-8: Definition of response time: (Measure System A_Photometer)



9. INTERFACE PIN CONNECTION

Main FPC Pin assignment — AMOLED Panel Input/Output Signal Interface

Recommended connector: 504248-2410 (Molex)

FPC	Symbol	I/O	Function	Remark
1	GND	P	GND	
2	RESX	I	Device reset signal (0 : Enable ; 1: Disable)	
3	HSSI_D0_N	I/O	MIPI data negative signal	
4	SWIRE	O	SWIRE signal for PWR IC control	
5	HSSI_D0_P	I/O	MIPI data positive signal	
6	MTP_PWR	P	MTP(need to indicate to connect GND or NC)	
7	GND	P	GND	
8	TE	O	Vsync(vertical sync)signal output from panel to avoid tearing effect	
9	HSSI_CLK_N	I	MIPI negative clock signal	
10	GND	P	GND	
11	HSSI_CLK_P	I	MIPI positive clock signal	
12	GND	P	GND	
13	GND	P	GND	
14	GND	P	GND	
15	VDDIO	P	Power supply for Interface system	
16	VCI	P	Power supply for analog	
17	GND	P	GND	
18	GND	P	GND	
19	ELVSS	P	AMOLED power Negative	
20	ELVDD	P	AMOLED power positive	
21	ELVSS	P	AMOLED power Negative	
22	ELVDD	P	AMOLED power positive	
23	ELVSS	P	AMOLED power Negative	
24	ELVDD	P	AMOLED power positive	

External Components

No.	Signal name	Values	Max ability
1	VDDA, VDDR, VDDB	Cap , 2.2uF	6.3V
2	VDDI, VCC	Cap , 2.2uF	6.3V
3	VREF	Cap , 22nF	6.3V
4	DVDD	Cap , 1.0uF	6.3V
5	VREFN5/VREFP5	Cap , 1.0uF	6.3V
6	VGHR	Cap , 1.0uF	16V
7	VGLR	Cap , 1.0uF	16V
8	BVP3D	Cap , 2.2uF	10V
9	BVN3D	Cap , 2.2uF	10V
10	C11P/C11N	Cap , 1.0uF	6.3V
11	C12P/C12N	Cap , 1.0uF	6.3V
12	AVDD	Cap , 2.2uF	10V
13	C31P/C31N	Cap , 1.0uF	6.3V
14	C32P/C32N	Cap , 1.0uF	6.3V
15	VCL	Cap , 2.2uF	6.3V
16	C41P/C41N	Cap , 1.0uF	16V
17	VGH	Cap , 2.2uF	25V
18	C51P/C51N	Cap , 1.0uF	16V
19	VGL	Cap , 2.2uF	25V
20	VGL (VGL-GND)	Schottky Diode	

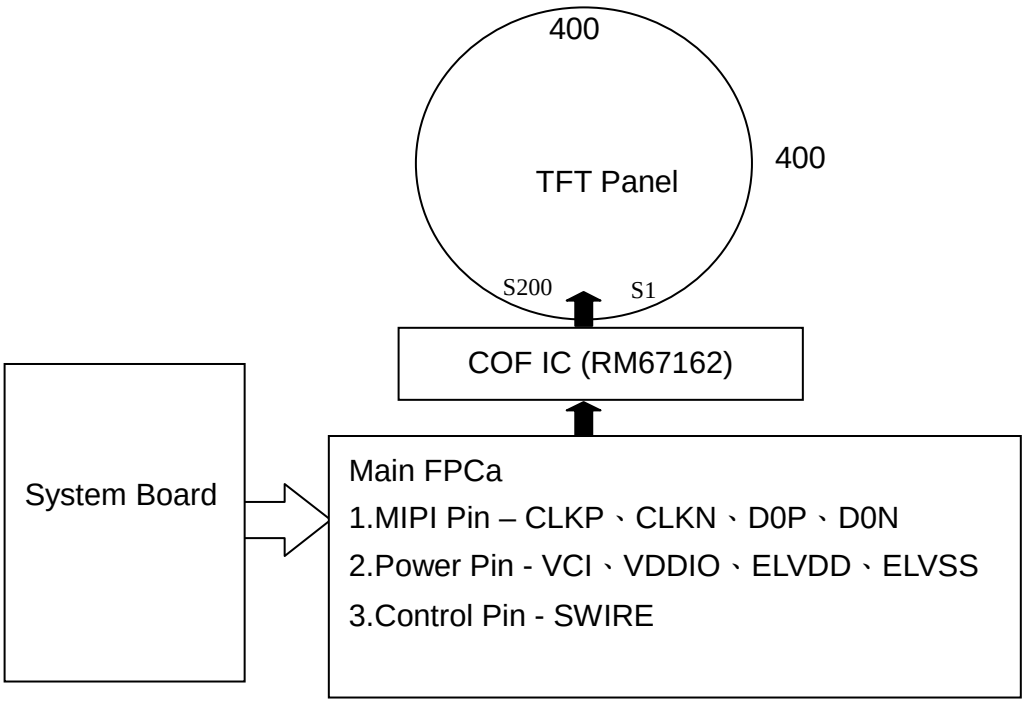
Display Initial code

MIPI data type	Address			Description
	MIPI	Others	Value	
0X39	FE	FE00	01	
0X39	25	2540	03	
0X39	26	2640	6F	
0X39	FE	FE00	04	
0X39	5E	5E70	45	
0X39	5F	5F70	00	
0X39	60	6070	20	
0X39	61	6170	A1	
0X39	62	6270	30	
0X39	5D	5D70	10	
0X39	5A	5A70	FF	
0X39	00	0070	8C	
0X39	01	0170	00	
0X39	02	0270	02	
0X39	03	0370	00	
0X39	04	0470	00	
0X39	05	0570	01	
0X39	06	0670	01	
0X39	07	0770	00	
0X39	08	0870	00	
0X39	09	0970	C0	
0X39	0A	0A70	00	
0X39	0B	0B70	02	
0X39	0C	0C70	00	
0X39	0D	0D70	70	
0X39	0E	0E70	05	
0X39	0F	0F70	50	
0X39	10	1070	2D	
0X39	11	1170	08	
0X39	12	1270	CC	
0X39	13	1370	00	
0X39	14	1470	02	
0X39	15	1570	00	
0X39	16	1670	70	
0X39	17	1770	04	
0X39	18	1870	50	
0X39	19	1970	2D	
0X39	1A	1A70	08	
0X39	1B	1B70	82	

0X39	1C	1C70	00	
0X39	1D	1D70	02	
0X39	1E	1E70	05	
0X39	1F	1F70	60	
0X39	20	2070	04	
0X39	21	2170	01	
0X39	22	2270	6F	
0X39	23	2370	00	
0X39	24	2470	CC	
0X39	25	2570	00	
0X39	26	2670	04	
0X39	27	2770	02	
0X39	28	2870	00	
0X39	29	2970	10	
0X39	2A	2A70	2B	
0X39	2B	2B70	15	
0X39	2D	2D70	26	
0X39	2F	2F70	C0	
0X39	30	3070	00	
0X39	31	3170	04	
0X39	32	3270	02	
0X39	33	3370	00	
0X39	34	3470	12	
0X39	35	3570	2B	
0X39	36	3670	15	
0X39	37	3770	26	
0X39	FE	FE00	01	
0X39	05	0540	12	
0X39	06	0640	64	
0X39	27	2740	12	
0X39	28	2840	12	
0X39	0E	0E40	80	
0X39	10	1040	51	
0X39	13	1340	82	
0X39	15	1540	81	
0X39	18	1840	CC	
0X39	19	1940	33	
0X39	1A	1A40	10	
0X39	1B	1B40	11	
0X39	1C	1C40	55	
0X39	36	3640	44	
0X39	3A	3A40	00	

0X39	3B	3B40	00	
0X39	3D	3D40	17	
0X39	3F	3F40	41	
0X39	40	4040	15	
0X39	41	4140	0D	
0X39	37	3740	10	
0X39	42	4240	33	
0X39	43	4340	22	
0X39	44	4440	11	
0X39	45	4540	66	
0X39	46	4640	55	
0X39	47	4740	44	
0X39	4C	4C40	33	
0X39	4D	4D40	22	
0X39	4E	4E40	11	
0X39	4F	4F40	66	
0X39	50	5040	55	
0X39	51	5140	44	
0X39	70	7040	05	
0X39	74	7440	0C	
0X39	FE	FE00	02	
0X39	9B	9B40	40	
0X39	9C	9C40	58	
0X39	9D	9D40	30	
0X39	FE	FE00	05	
0X39	05	0540	1D	
0X39	FE	FE00	00	
0x15	35	3500	01	
0x05	11	1100	00	
Delay 300ms				
0x05	29	2900	00	

10. BLOCK DIAGRAM



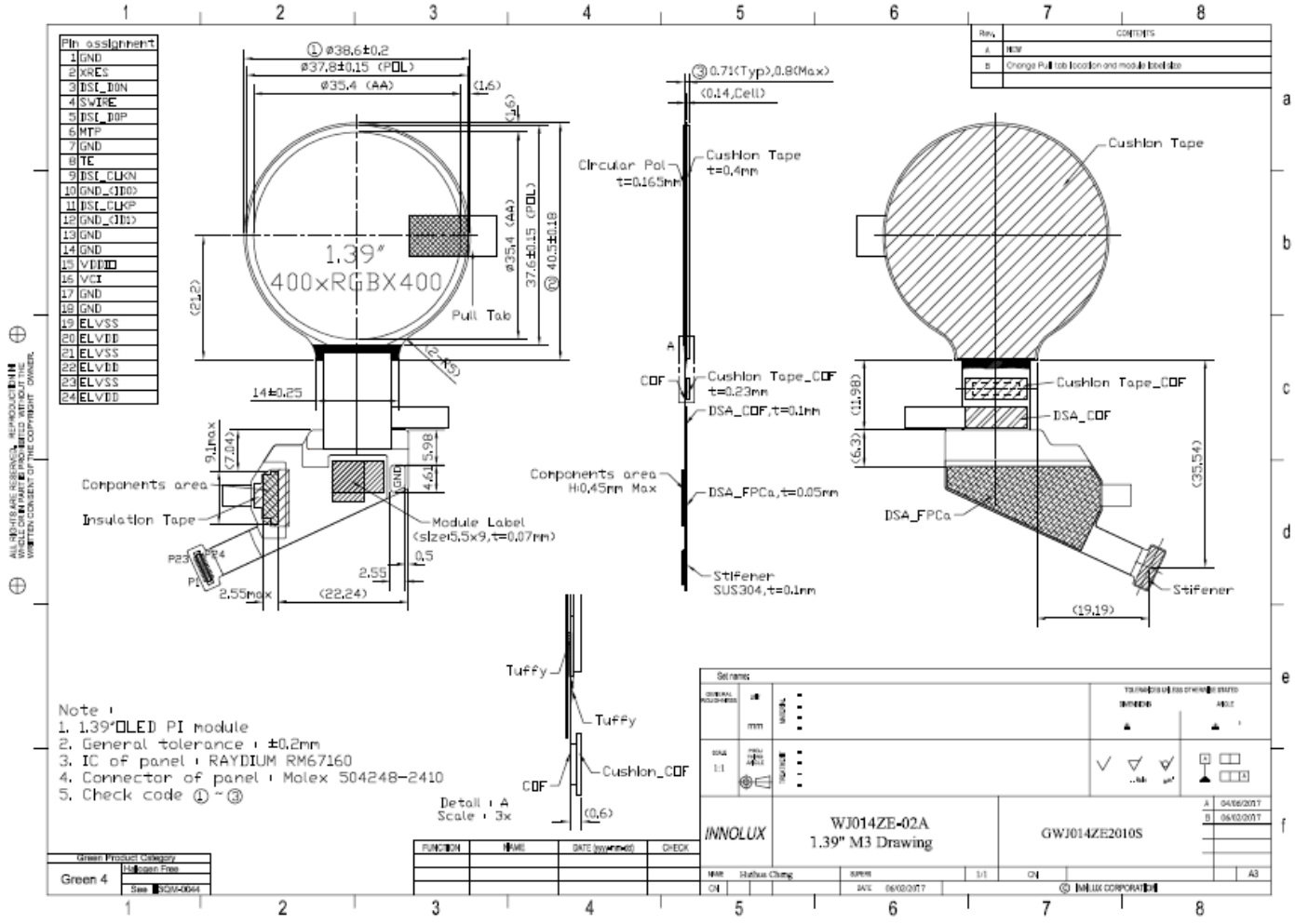
11.QUALITY ASSURANCE

No	Test Item	Condition	Remark
1	High Temperature Operation	Ta=60℃, 240Hrs	Note1, Note2
2	High Temperature Storage	Ta=70℃, 240Hrs	Note1, Note2
3	Low Temperature Operation	Ta=-20℃, 240Hrs	Note1, Note2
4	Low Temperature Storage	Ta=-30℃, 240Hrs	Note1, Note2
5	High Temperature & High Humidity Operation	Ta=60℃, RH=90%, 240Hrs	Note1, Note2
7	Thermal Shock	-30℃(30min)←→70℃(30min), 100Cycles	Note1, Note2
8	Vibration Test - Non Operation	1.5G / 10-500Hz, 30mins/cycle, 1cycle for each X, Y, Z	Note2

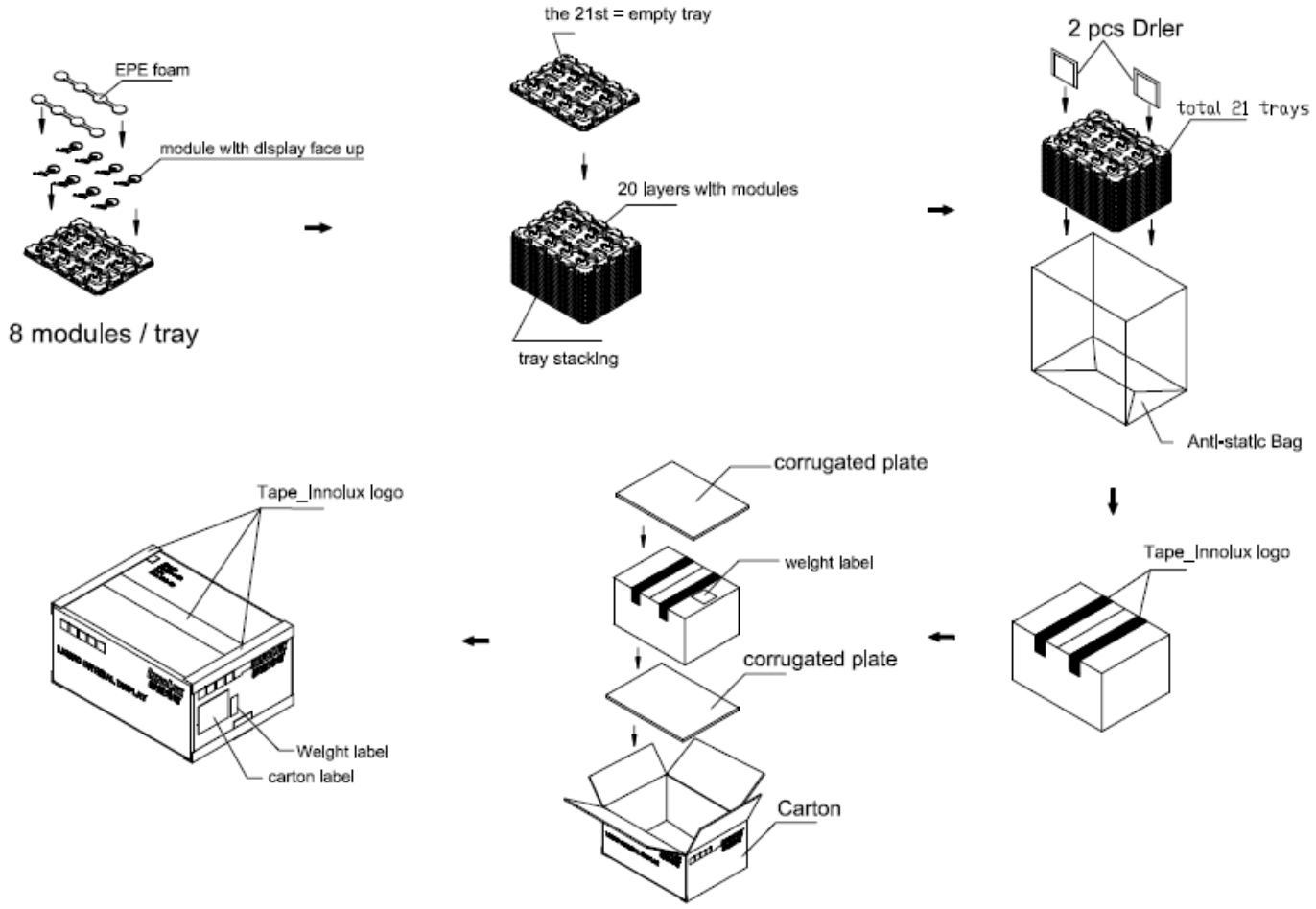
Note1: The test samples have recovery time for 2 hours at room temperature before the function check. In the standard conditions, there is no display function NG issue occurred.

Note2: After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

12. OUTLINE DRAWING



13. PACKAGE FORM



1.39" Module (WJ014ZE-02A) delivery packing method

(1). Module packed into tray cavity (with Module display face up) and covered byEPE.

(2). Tray stacking with 20 layers and with 1 empty tray above the stacking tray unit.
2pcs desiccant put above the empty tray

(3). Stacking tray unit put into the LDPE bag and fix by adhesive tape.

(4). Put 1pc cardboard inside the carton bottom, and then pack the package unit into the carton. Put 1pc cardboard above the package unit.

(5). Carton tapping with adhesive tape.

14. PRECAUTIONS

Please pay attention to the following when you use this AMOLED module.

14.1 Mounting Precautions

(1) You must mount a module using arranged in four corners or four sides.

(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.

(3) Please attach a transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.

(4) You should adopt radiation structure to satisfy the temperature specification.

(5) Acetic acid type and chlorine type materials for the cover case are not describe because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.

(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are determined to the polarizer)

(7) When the surface becomes dusty, please wipe gently with adsorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.

(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.

(9) Do not open the case because inside circuits do not have sufficient strength.

14.2 Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage : V=±200mV(Over and under shoot voltage)

(2) Response time depends on the temperature. (In lower temperature, it becomes longer.)

(3) Brightness depends on the temperature. (In lower temperature, it becomes lower)
And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.

(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.

(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.

(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be

done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

14.3 Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wristband etc. And don't touch interface pin directly.

14.4 Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

14.5 Storage

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.

(2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

14.6 Handling Precautions for Protection Film

(1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.

(2) The protection film is attached to the polarizer with a small amount of glue. It is apt to remain on the polarizer. Please carefully peel off the protection film without rubbing it against the polarizer.

(3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.

(4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

