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CUSTOMER APPROVAL SHEET

Company Name	
MODEL	A030VVN01.0
CUSTOMER APPROVED	Title : Name :

☐ APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 0.4)

☐ APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver. 0.4)

☐ APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver. 0.4)

☐ CUSTOMER REMARK :

P/N : 97.03A38.000
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Doc. version :	0.4
Total pages :	42
Date :	2012/03/07

Product Specification
3.0" COLOR TFT-LCD MODULE

Model Name： **A030VVN01.0**

Planned Lifetime:	From 2011/Nov To 2013/ Nov
Phase-out Control:	From 2013/Dec To 2014/ May
EOL Schedule:	2014/May

< ◆ >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2011/6/24	-	First Draft
0.1	2011/8/22	7	Update Cell Power
		15	Update R0[7] description
		36-37	Power On Recommend Command
		32	Update Outline dimension
0.2	2011/9/6	27	Update Note
0.3	2011/11/23	34-35	Update Gamma setting
		26	Add R,G,B chromaticity spec
0.4	2012/03/07	26, 28	Add brightness and uniformity specification after reliability test.

Contents

A. General Information

NO.	Item	Specification	Remark
1	Display resolution（dot）	480 (W) x 640(RGB) (H)	
2	Active area（mm）	60 x 45	
3	Screen size（inch）	2.95 (Diagonal)	
4	Dot pitch（um）	93.75 x 93.75	
5	Color configuration	R, G, B strip	
6	Overall dimension（mm）	71.4 x 51.0 x 2.2	Note 1
7	Weight（g）	20	
8	Panel surface treatment	AR <= 1.45%	

Note 1: Refer to F. Outline Dimension

B. Electrical Specifications

Connector: Hirose : FH26-45S-0.3SHW

Pin no	Symbol	I/O	Description	Remark
1	GND	P	Ground	
2	DR7	I	Data signal (MSB)	Note1
3	DR6	I	Data signal	Note1
4	DR5	I	Data signal	Note1
5	DR4	I	Data signal	Note1
6	DR3	I	Data signal	Note1
7	DR2	I	Data signal	Note1
8	DR1	I	Data signal	Note1
9	DR0	I	Data signal (LSB)	Note1
10	GND	P	Ground	
11	DG7	I	Data signal (MSB)	Note2
12	DG6	I	Data signal	Note2
13	DG5	I	Data signal	Note2
14	DG4	I	Data signal	Note2
15	DG3	I	Data signal	Note2
16	DG2	I	Data signal	Note2
17	DG1	I	Data signal	Note2
18	DG0	I	Data signal (LSB)	Note2
19	GND	P	Ground	
20	DB7	I	Data signal (MSB)	Note3
21	DB6	I	Data signal	Note3
22	DB5	I	Data signal	Note3
23	DB4	I	Data signal	Note3
24	DB3	I	Data signal	Note3
25	DB2	I	Data signal	Note3
26	DB1	I	Data signal	Note3
27	DB0	I	Data signal (LSB)	Note3
28	GND	P	Ground	
29	SDA	I	Data input pin of SPI mode	
30	CS	I	Chip select pin of SPI interface	
31	SCL	I	Clock input pin of SPI mode	
32	DCLK	I	Data-clock and oscillator source	
33	Dummy1	Dummy	Not connected	
34	HSYNC	I	Horizontal synchronizing signal	

35	VSYNC	I	Vertical synchronizing signal	
36	RESET	I	System reset pin	
37	VDDIO	P	Voltage input pin for logic I/O	
38	VDD	P	Voltage input pin for digital power	
39	VCI	P	Voltage input pin for analog power	
40	VCI	P	Voltage input pin for analog power	
41	Dummy2	Dummy	Not connected	
42	Dummy3	Dummy	Not connected	
43	Dummy4	Dummy	Not connected	
44	VLED-	P	LED backlight cathode	
45	VLED+	P	LED backlight anode	

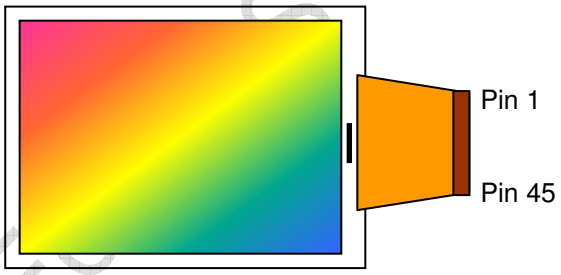
I：Input, O：Output, C：Capacitor, P：Power, D：Dummy

Note1:DR[7:0] : When input timing is ‘Parallel RGB’, it is as Red digital data input.
When input timing is ‘YUV’, it is as Y-data input.

Note2:DG[7:0]: When input timing is ‘Parallel RGB’, it is as Green digital data input.
When input timing is ‘YUV’, it is as C-data input.

Note3:DB[7:0] :When input timing is ‘Parallel RGB’, it is as Blue digital data input.

Note4:Definition of scanning direction, Refer to figure as below：



2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Supply Voltage	VCI	GND=0V	-0.3	5.0	V	
Supply Voltage	VDD	GND=0V	-0.3	5.0	V	
Supply Voltage	VDDIO	GND=0V	-0.3	5.0	V	

Note 1: Functional operation should be restricted under ambient temperature (25°C).

Note 2: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

3. Electrical characteristics

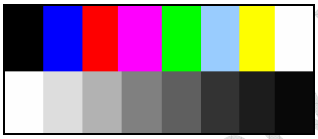
3.1 Recommended operating conditions (GND=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VCI	3.0	3.3	3.6	V	
		VDD	3.0	3.3	3.6	V	
		VDDIO	3.0	3.3	3.6	V	
Input Signal voltage	H Level	V_{IH}	0.7* VDDIO	-	VDDIO	V	
	L Level	V_{IL}	GND	-	0.3* VDDIO	V	

3.2 Electrical characteristics (GND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Current for V_{VCI}	I_{VCI}	V_{VCI}=3.3V	-	20	30	mA	Note 1
	$I_{VCI(STANDBY)}$		-	0.1	0.2		
Input Current for V_{VDD}	I_{VDD}	V_{VDD}=3.3V	-	5	8	mA	Note 1
	$I_{VDD(STANDBY)}$		-	0.1	0.2		
Input Current for V_{VDDIO}	I_{VDDIO}	V_{VDDIO}=3.3V	-	1	3	mA	Note 1
	$I_{VDDIO(STANDBY)}$		-	0.1	0.2		

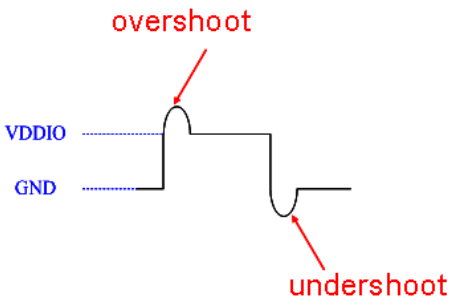
Note 1: Test Condition: 8colorbar+Grayscale pattern, Frame rate: 60Hz, other registers are default setting.



3.3 Digital input signal overshoot and undershoot limitation

The digital input signal overshoot and undershoot voltage should keep under VDDIO+0.2V and over GND-0.2V.

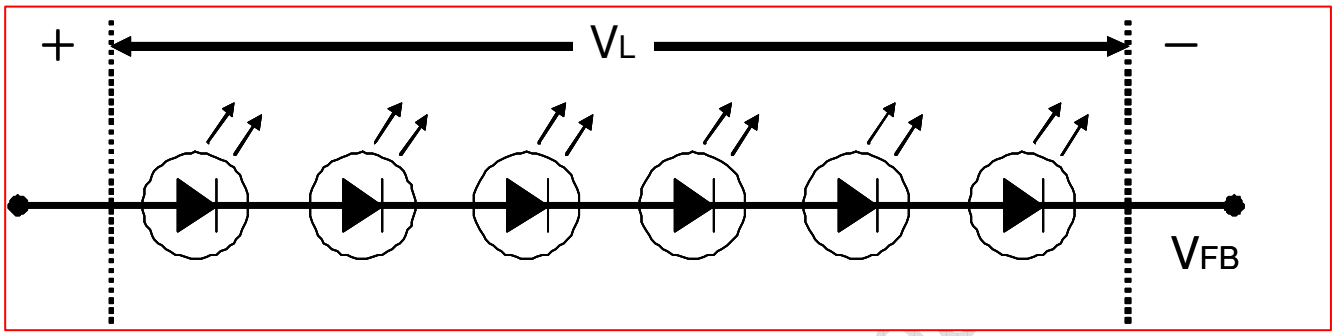
Symbol	Overshoot	Undershoot
DB[7:0]	< VDDIO+0.2V	> GND-0.2V
DG[7:0]		
DR[7:0]		
DCLK		
HSYNC/VSYNC		
SCL/ SDA/ CS		



3.4 Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.[Note1]	Unit	Remark
Backlight Current			25	27.5	mA	**Note2**
Backlight voltage	V_L	17.28	19.2	21.12	V	6 LED's

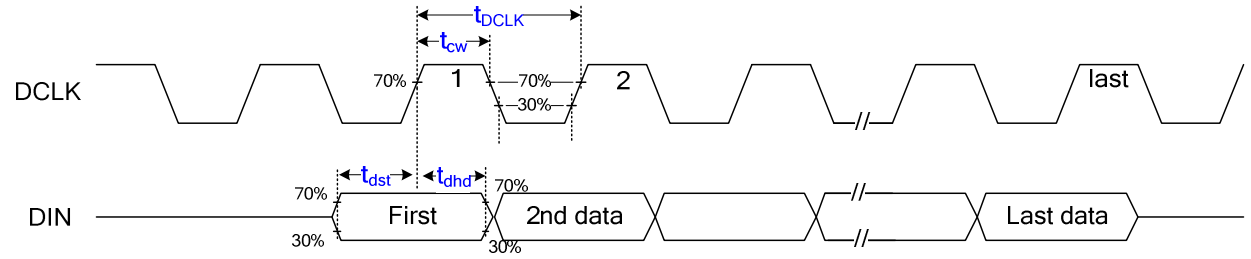
Note1: To consider LED driver and feedback resistor tolerance.
Note2: If using LCD internal LED driver controller the maximum setting should be typical value. Ta=25℃

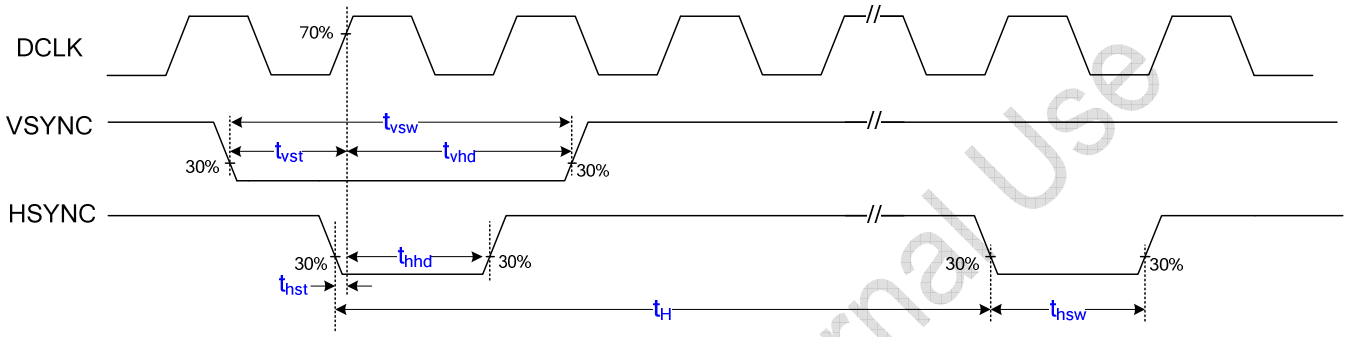


4. Input timing AC characteristic

(VCI=3.0 ~3.6V, AGND=GND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK duty cycle	Tcw	40	50	60	%	
VSYNC setup time	Tvst	10	-	-	ns	
VSYNC hold time	Tvhd	10	-	-	ns	
HSYNC setup time	Thst	10	-	-	ns	
HSYNC hold time	Thhd	10	-	-	ns	
Data setup time	Tdst	10	-	-	ns	
Data hold time	Tdhd	10	-	-	ns	





t_H means: HSYNC period

5. Input timing format

5.1 Parallel RGB timing (Refer to Fig.1 Fig.2)

Parameter		Symbo	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency		$1/t_{DCLK}$	19.75	24	28.22	MHz	
HSYNC	Period	t_H	680	762	840	t_{DCLK}	
	Display period	t_{hd}		640		t_{DCLK}	
	Blanking	t_{hb}	20	81	150	t_{DCLK}	Note 1
	Front porch	t_{hfp}	20	41	50	t_{DCLK}	
	Pulse width	t_{hsw}	1	40	50	t_{DCLK}	
VSYNC	Period	t_V	484	525	560	t_H	
	Display period	t_{vd}		480		t_H	
	Blanking	t_{vb}	3	27	50	t_H	Note 2
	Front porch	t_{vfp}	1	18	30	t_H	
	Pulse width	t_{vsw}	1	9	18	t_H	

Note 1: The t_{hb} time is adjustable by setting register HBLANKING; requirement of minimum blanking time and minimum front porch time must be satisfied.

Note 2: The t_{vb} time is adjustable by setting register VBLANKING.

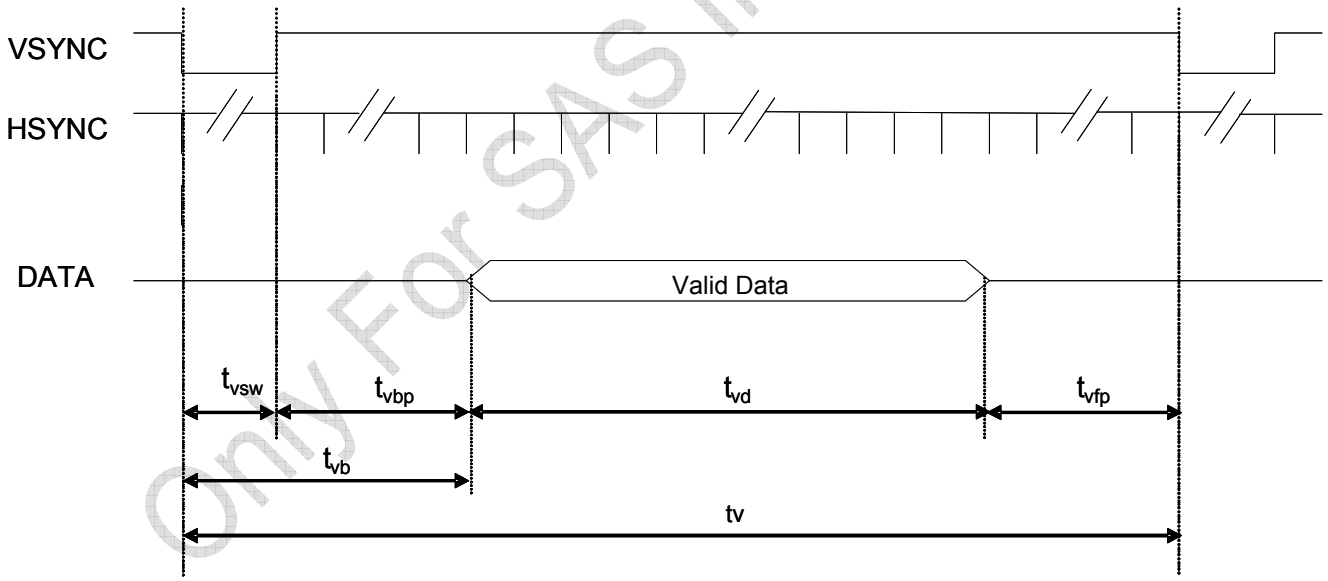


Fig.1 Parallel RGB Input Vertical Timing Chart

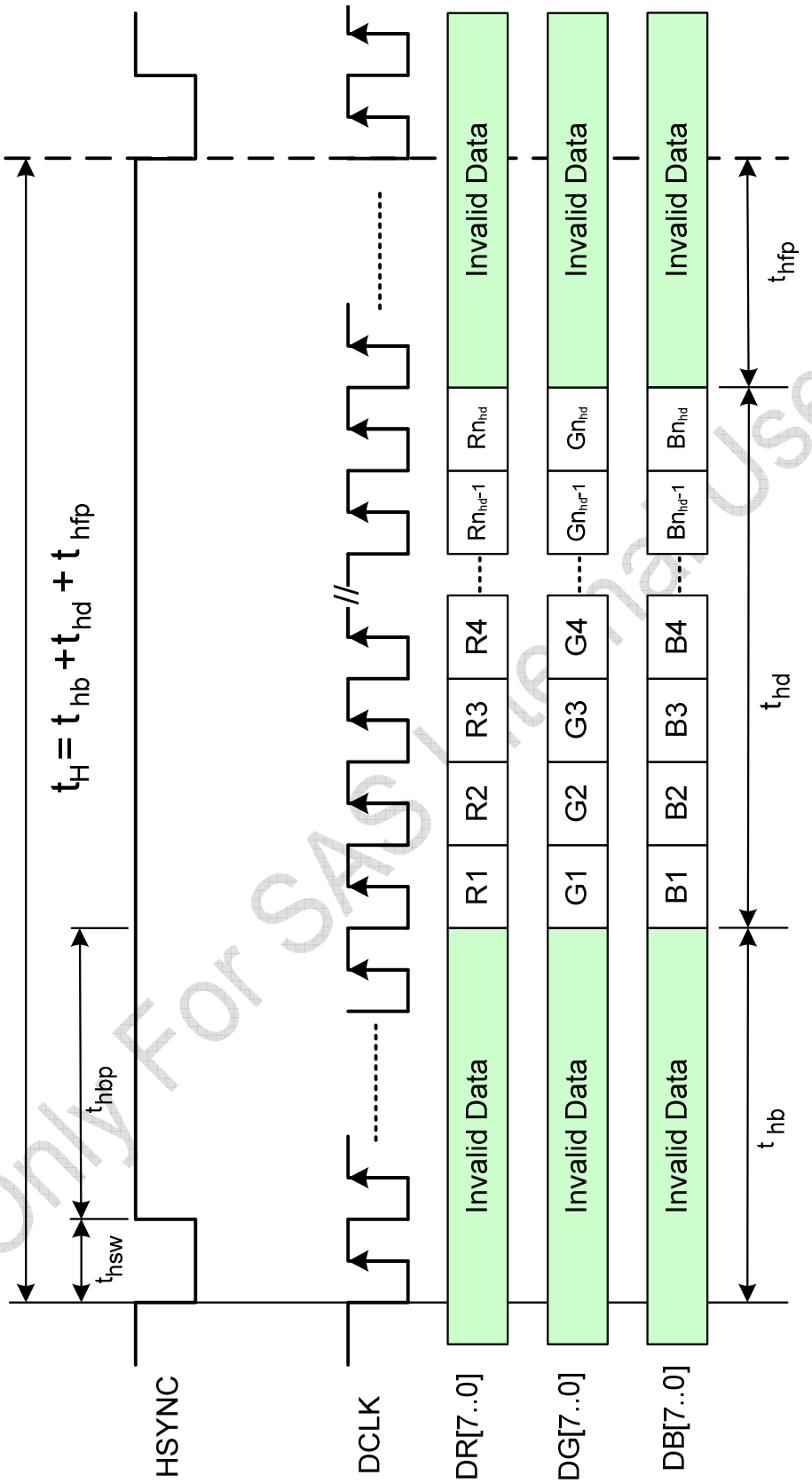


Fig.2 Parallel RGB Input Horizontal Timing Chart

5.2 YUV timing (Refer to Fig.3 Fig.4)

Parameter		Symbo	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency		$1/t_{DCLK}$	19.75	24	28.22	MHz	
HSYNC	Period	t_H	680	762	840	t_{DCLK}	
	Display period	t_{hd}	640			t_{DCLK}	
	Blanking	t_{hb}	20	81	150	t_{DCLK}	Note 1
	Front porch	t_{hfp}	20	41	50	t_{DCLK}	
	Pulse width	t_{hsw}	1	40	50	t_{DCLK}	
VSYNC	Period	t_V	484	525	560	t_H	
	Display period	t_{vd}	480			t_H	
	Blanking	t_{vb}	3	27	50	t_H	Note 2
	Front porch	t_{vfp}	1	18	30	t_H	
	Pulse width	t_{vsw}	1	9	18	t_H	

Note 1: The t_{hb} time is adjustable by setting register HBLANKING; requirement of minimum blanking time and minimum front porch time must be satisfied.

Note 2: The t_{vb} time is adjustable by setting register VBLANKING.

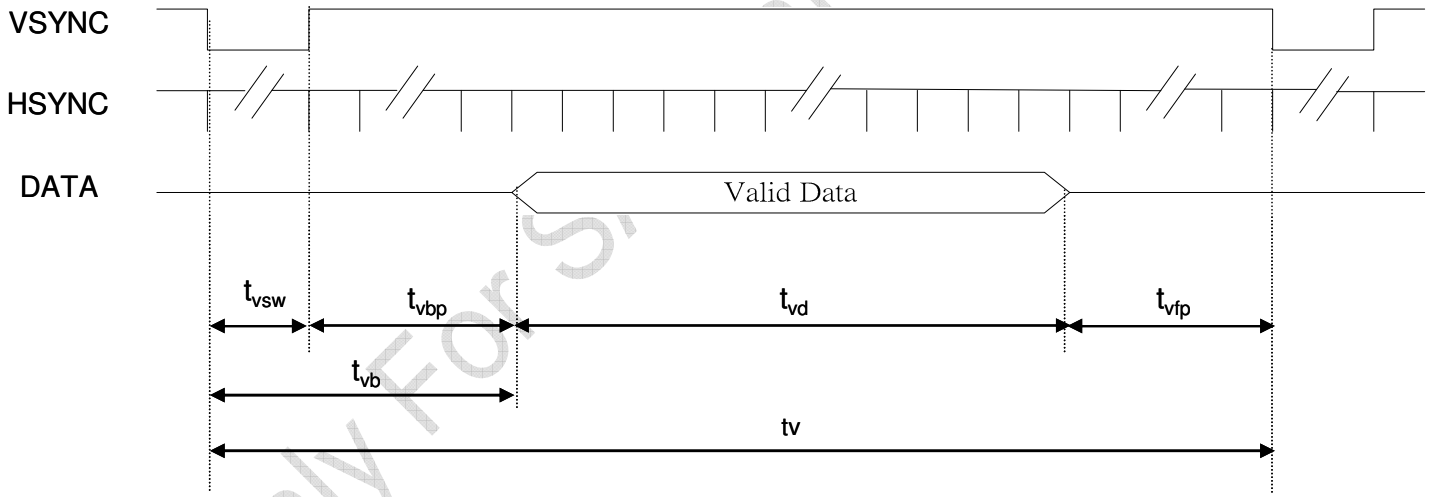


Fig.3 YUV Input Vertical Timing Chart

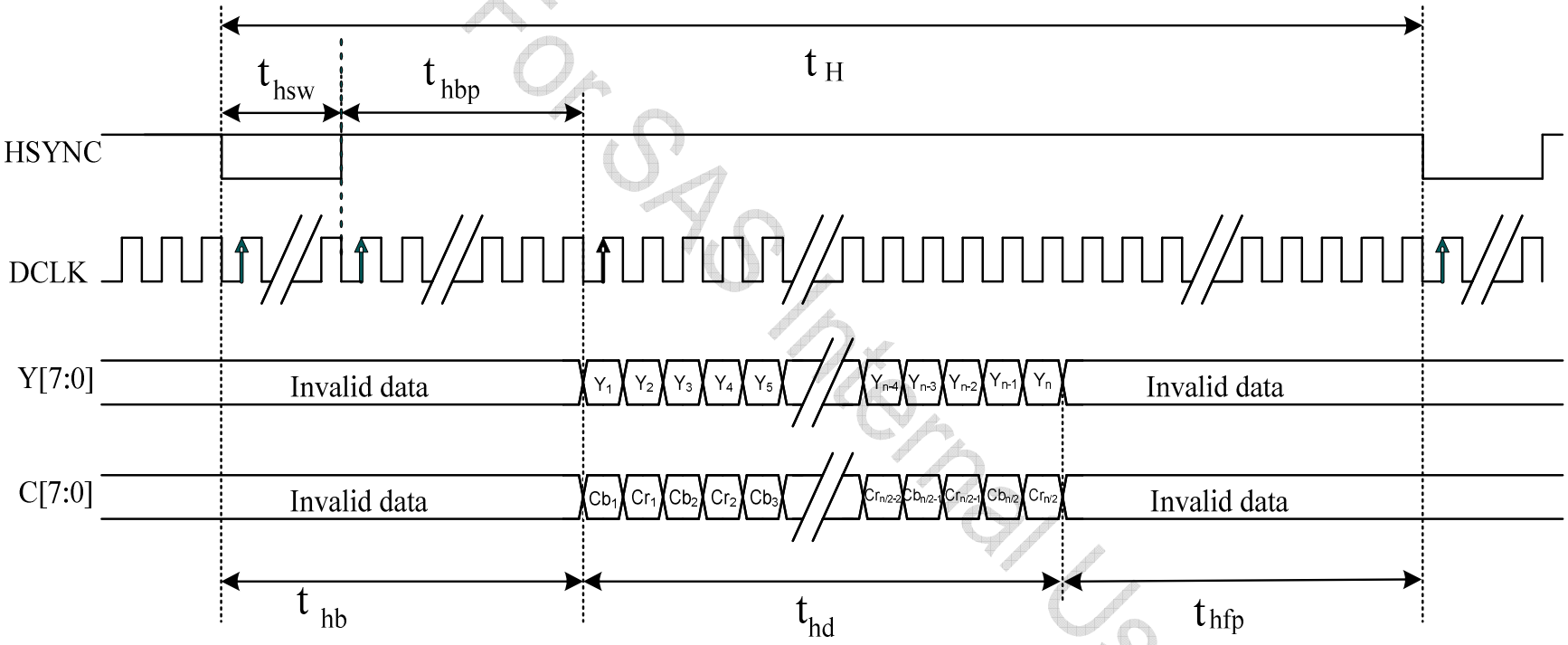
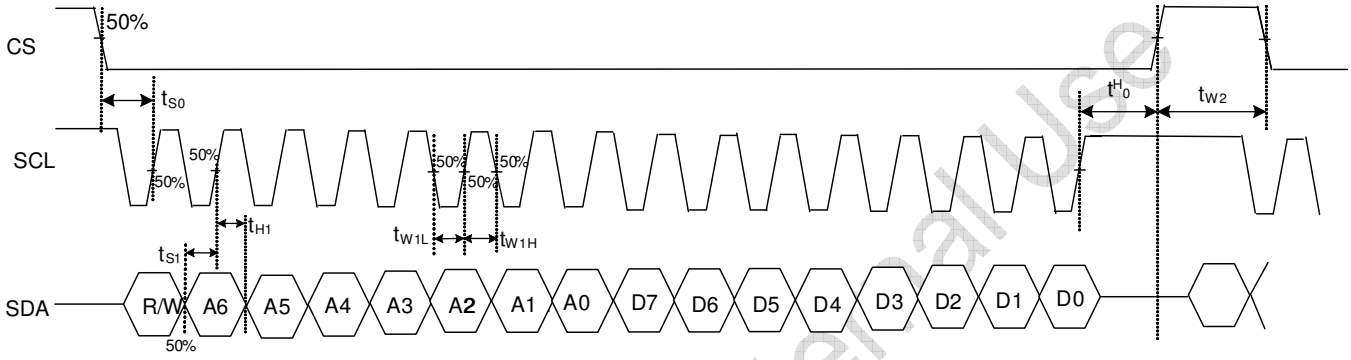


Fig.4 YUV Input Horizontal Timing Chart

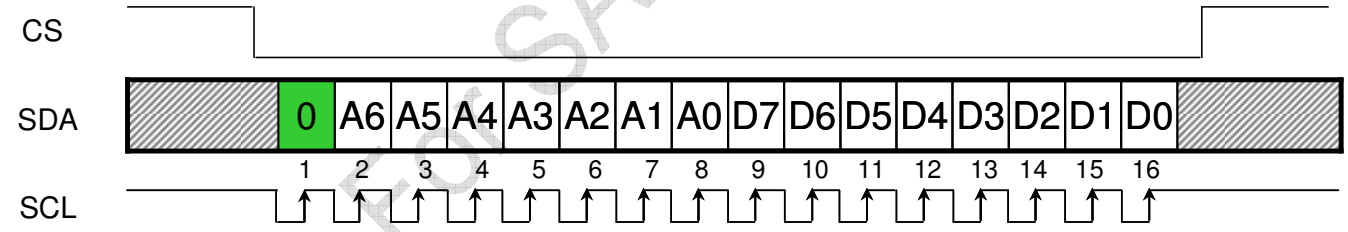
6. Serial control interface AC characteristic

Item	Symbol	Min	Typical	Max	Unit
CS input setup Time	t_{S0}	50	-	-	ns
Serial data input setup Time	t_{S1}	50	-	--	ns
CS input hold Time	t_{H0}	50	-	-	ns
Serial data input hold Time	t_{H1}	50	-	-	ns
SCL pulse low width	t_{W1L}	50	-	-	ns
SCL pulse high width	t_{W1H}	50	-	-	ns
CS pulse high width	t_{W2}	400	-	-	ns



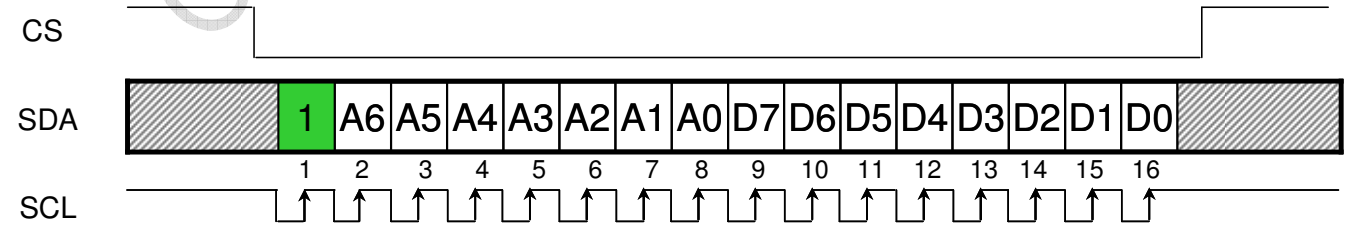
6.1 Timing chart

Write Mode:



Serial Interface Write Sequence

Read Mode:



Serial Interface Read Sequence

6.2 Register table

No.	Register address								MSB Register data							LSB
	R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	VCOM_SET(0)	VCOM(0Eh)						
R1	0	0	0	0	0	0	0	1	U2D(1)	L2R(1)	CBCR(1)	VDPOL(1)	HDPOL(1)	DCLKPOL (0)	X	IM(1)
R2	0	0	0	0	0	0	1	0	HBLANKING(51h)							
R3	0	0	0	0	0	0	1	1	X	X	VBLANKING(1Bh)					
R4	0	0	0	0	0	1	0	0	CONTRAST(40h)							
R5	0	0	0	0	0	1	0	1	X	SUB_CONTRAST_R(40h)						
R6	0	0	0	0	0	1	1	0	X	SUB_CONTRAST_B(40h)						
R7	0	0	0	0	0	1	1	1	BRIGHTNESS(40h)							
R8	0	0	0	0	1	0	0	0	X	SUB_BRIGHTNESS_R(40h)						
R9	0	0	0	0	1	0	0	1	X	SUB_BRIGHTNESS_B(40h)						
R10	0	0	0	0	1	0	1	0	X	X	X	X	X	X	GRB(1)	STB(0)
R11	0	0	0	0	1	0	1	1	(VGH, VGL setting) Please refer to recommended setting							
R12	0	0	0	0	1	1	0	0	(R gamma setting) Please refer to recommended setting							
R13	0	0	0	0	1	1	0	1	(R gamma setting) Please refer to recommended setting							
R14	0	0	0	0	1	1	1	0	(R gamma setting) Please refer to recommended setting							
R15	0	0	0	0	1	1	1	1	(R gamma setting) Please refer to recommended setting							
R16	0	0	0	1	0	0	0	0	(R gamma setting) Please refer to recommended setting							
R17	0	0	0	1	0	0	0	1	(G gamma setting) Please refer to recommended setting							
R18	0	0	0	1	0	0	1	0	(G gamma setting) Please refer to recommended setting							
R19	0	0	0	1	0	0	1	1	(G gamma setting) Please refer to recommended setting							
R20	0	0	0	1	0	1	0	0	(G gamma setting) Please refer to recommended setting							
R21	0	0	0	1	0	1	0	1	(G gamma setting) Please refer to recommended setting							
R22	0	0	0	1	0	1	1	0	(B gamma setting) Please refer to recommended setting							
R23	0	0	0	1	0	1	1	1	(B gamma setting) Please refer to recommended setting							
R24	0	0	0	1	1	0	0	0	(B gamma setting) Please refer to recommended setting							
R25	0	0	0	1	1	0	0	1	(B gamma setting) Please refer to recommended setting							
R26	0	0	0	1	1	0	1	0	(B gamma setting) Please refer to recommended setting							

"X" => Please set to '0'.

6.2.1 R0 register

No.	Register Address		MSB	Register Data						LSB
	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R0	1/0	00h	VCOM_SET(0)	VCOM(0E)						

VCOM_SET : Common voltage DC level selection.

VCOM_SET	Voltage (V)
0	VCOM voltage setting by OTP. **(Default)**
1	VCOM voltage setting by register

VCOM : Common voltage DC level selection.

VCOM D6~D0	Voltage (V)
00h	-0.1
:	:
0Eh	-0.31 **(Default)**
:	:
7Fh	-2.005

6.2.2 R1 register

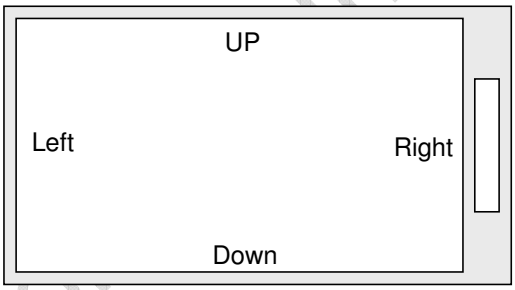
No.	Register Address		MSB			Register Data				LSB
	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R1	1/0	01h	U2D	L2R	CBCR	VDPOL	HDPOL	DCLKPOL	0	IM

U2D : Vertical scan direction selection.

U2D	Description
D7	
0	Down to up scan;
1	Up to down scan; **(Default)**

L2R : Horizontal scan direction selection.

L2R	Description
D6	
0	Right to left scan
1	Left to right scan **(Default)**



CBCR : Cb and Cr exchange position selection. This setting is only valid on YUV 16_bit mode.

CBCR	Description
D5	
0	Cr1, Cb1, Cr2, Cb2, ……
1	Cb1, Cr1, Cb2, Cr2, ……**(Default)**

CBCR='0'

	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8
	Cr1	Cb1	Cr2	Cb2	Cr3	Cb3	Cr4	Cb4

CBCR='1' (Default)

	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8
	Cb1	Cr1	Cb2	Cr2	Cb3	Cr3	Cb4	Cr4

VDPOL : Vertical polarity selection.

VDPOL	Description
D4	
0	Positive polarity
1	Negative polarity **(Default)**

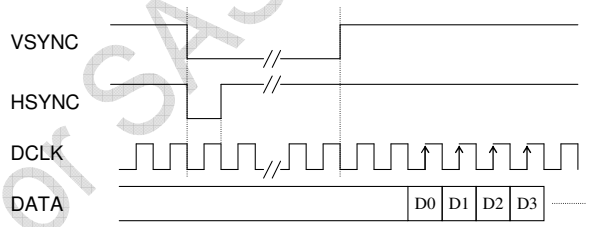
HDPOL : HSYNC polarity selection.

HDPOL	Description
D3	
0	Positive polarity
1	Negative polarity **(Default)**

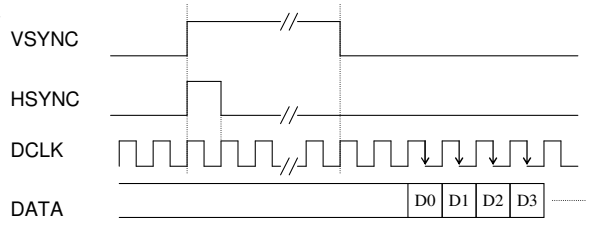
DCLK_POL : DCLK polarity selection.

DCLK_POL	Description
D2	
0	Positive polarity **(Default)**
1	Negative polarity

• HDPOL=1, VDPOL=1, DCLKPOL=0



• HDPOL=0, VDPOL=0, DCLKPOL=1



IM: Input data timing format selection.

IM	Description
0	Parallel RGB
1	YUV 16 bit

6.2.3 R2 register

No.	Register Address		MSB			Register Data				LSB
	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R2	1/0	02h	HBLANKING							

HBLANKING : Horizontal blanking setting.

MODE	HSYNC_BLANKING	Description	Unit	Remark
	D7~D0			
Parallel RGB YUV	00h	0	DCLK	
	51h	81 **(Default)**	DCLK	
	FFh	255	DCLK	

6.2.4 R3 register

No.	Register Address		MSB			Register Data				LSB
	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R3	1/0	03h	X	X	VBLANKING					

VBLANKING : Vertical blanking setting.

Interface	HSYNC_BLANKING	Description	Unit	Remark
	D7~D0			
Parallel RGB YUV	00h	0	DCLK	
	1Bh	27 **(Default)**	DCLK	
	3Fh	63	DCLK	

6.2.5 R4 register

No.	Register Address		MSB			Register Data				LSB
	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R4	1/0	04h	CONTRAST							

CONTRAST : RGB contrast level setting.

CONTRAST	Gain
D7~D0	
00h	0
:	:
40h	1 **(Default)**
:	:
FFh	3.984

6.2.6 R5 register

No.	Register Address		MSB	Register Data						LSB
	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R5	1/0	05h	X	SUB_CONTRAST_R						

SUB_CONTRAST_R : R sub-contrast level setting.

SUB_CONTRAST_R	Gain
D6~D0	
00h	0.75
:	:
40h	1 **(Default)**
:	:
7Fh	1.246

6.2.7 R6 register

No.	Register Address		MSB	Register Data						LSB
	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R6	1/0	06h	X	SUB_CONTRAST_B						

SUB_CONTRAST_B : B sub-contrast level setting.

SUB_CONTRAST_B	Gain
D6~D0	
00h	0.75
:	:
40h	1 **(Default)**
:	:
7Fh	1.246

6.2.8 R7 register

No.	Register Address		MSB			Register Data				LSB
	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R7	1/0	07h	BRIGHTNESS							

BRIGHTNESS : RGB brightness level setting.

BRIGHTNESS	Level
D7~D0	
00h	Dark (-64)
:	:
40h	Center (0) **(Default)**
:	:
FFh	Bright (+191)

6.2.9 R8 register

No.	Register Address		MSB			Register Data				LSB
	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R8	1/0	08h	X	SUB_BRIGHTNESS_R						

SUB_BRIGHTNESS_R : R sub-brightness level setting.

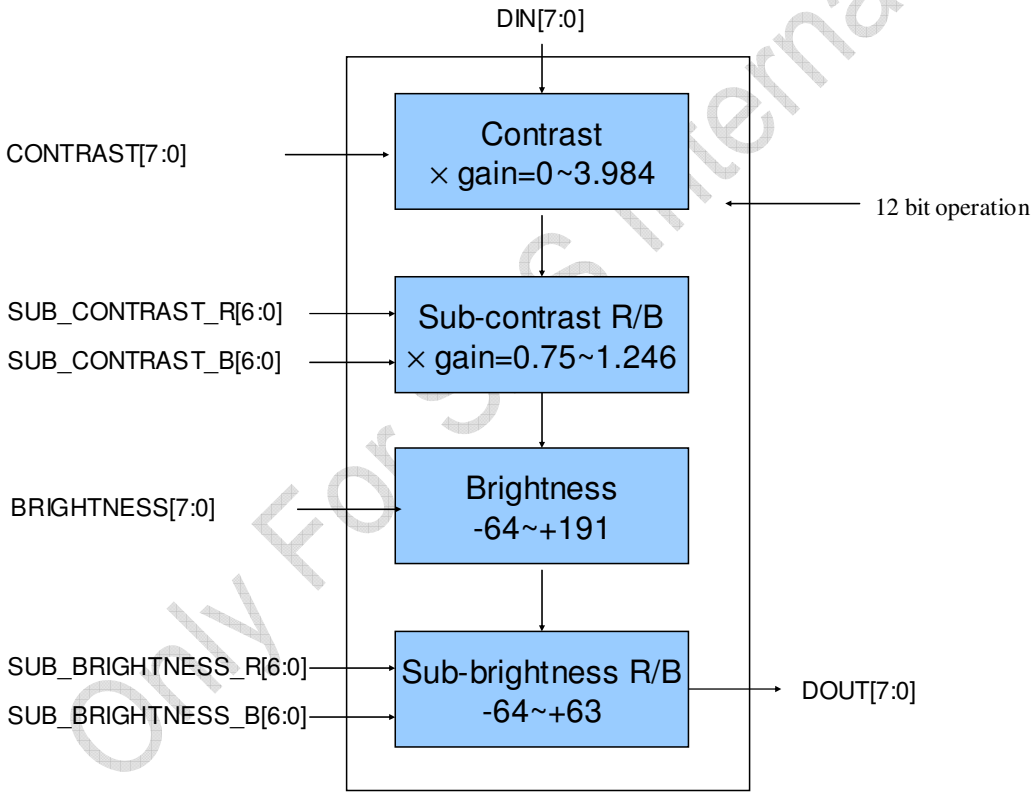
SUB_BRIGHTNESS_R	Level
D6~D0	
00h	Dark (-64)
:	:
40h	Center (0) **(Default)**
:	:
7Fh	Bright (+63)

6.2.10 R9 register

No.	Register Address		MSB	Register Data						LSB
	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R9	1/0	09h	X	SUB_BRIGHTNESS_B						

SUB_BRIGHTNESS_B : R sub-brightness level setting.

SUB_BRIGHTNESS_B D6~D0	Level
00h	Dark (-64)
:	:
40h	Center (0) **(Default)**
:	:
7Fh	Bright (+63)



Rout = Rin x CONTRAST x SUB_CONTRAST_R+ BRIGHTNESS + SUB_BRIGHTNESS_R
Gout = Gin x CONTRAST + BRIGHTNESS
Bout = Bin x CONTRAST x SUB_CONTRAST_B+ BRIGHTNESS + SUB_BRIGHTNESS_B

6.2.11 R10 register

No.	Register Address		MSB			Register Data				LSB
	$R/\overline{W}$	Address	D7	D6	D5	D4	D3	D2	D1	D0
R10	1/0	0Ah	0	0	0	0	0	0	GRB	STB

GRB : Global reset setting

GRB	Description
D1	
0	Reset all registers to default value.
1	Normal operation. **(Default)**

STB : Standby (power saving) mode selection.

STB	Description
D0	
0	Standby; timing control, DAC, and DC/DC converter are off, and register data should be kept. **(Default)**
1	Normal operation; with power on/off sequence.

C. Optical Specification (Note1, Note 2 and Note 3)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time	Rise	Tr	θ=0°	--	15	30	ms	Note 4
	Fall	Tf		--	30	50		
Contrast ratio		CR	At optimized viewing angle	600	1000	--	--	Note 5
Viewing Angle	Top	Φ_T	CR≧10	70	80	--	deg.	Note 6
	Bottom	Φ_B		70	80	--		
	Left	Φ_L		70	80	--		
	Right	Φ_R		70	80	--		
Brightness		Y_L	θ=0°	400	480	--	cd/m^2	Note 7
				330	--	--	cd/m^2	Note 7 Note 10
Chromaticity	White	x	θ=0°	Note 8	0.31	Note 8	--	Note 8
		y		Note 8	0.33	Note 8	--	
	Red	x		0.60	0.63	0.66		
		y		0.33	0.36	0.39		
	Green	x		0.28	0.31	0.34		
		y		0.60	0.63	0.66		
	Blue	x		0.12	0.17	0.18		
		y		0.04	0.07	0.10		
Uniformity		ΔY_L	%	70	75	--	%	Note 9
				50	--	--	%	Note 9 Note 10

Note 1. Ambient temperature =25℃.

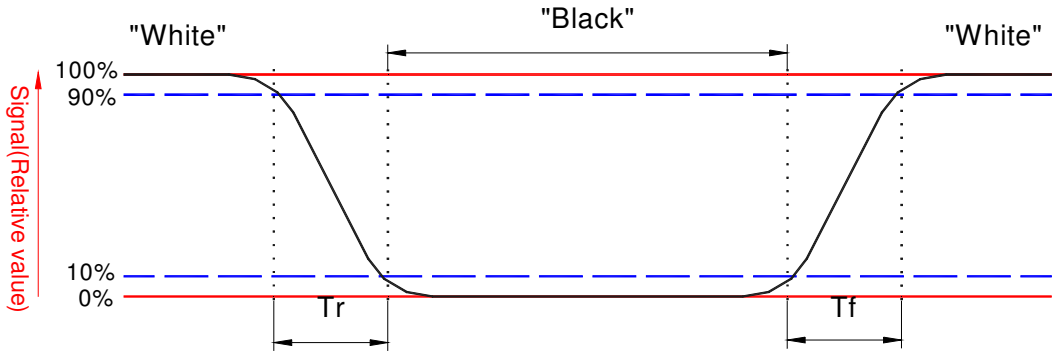
Note 2. To be measured in the dark room.

Note 3. To be measured on the center area of panel with a field angle of 1° by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

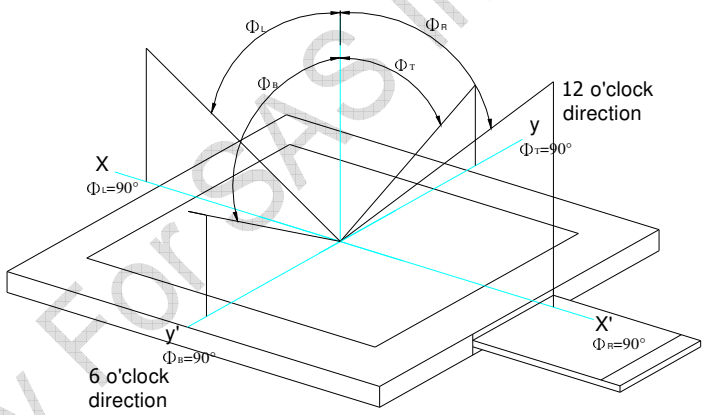


Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

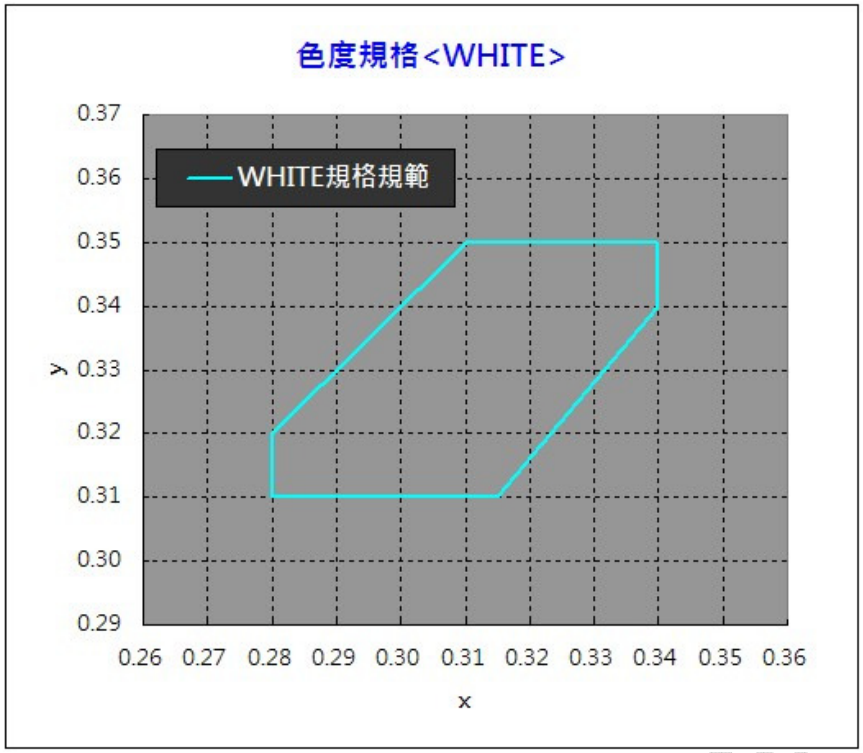
$$\text{Contrast Ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. Definition of viewing angle, ϕ, Refer to figure as below.



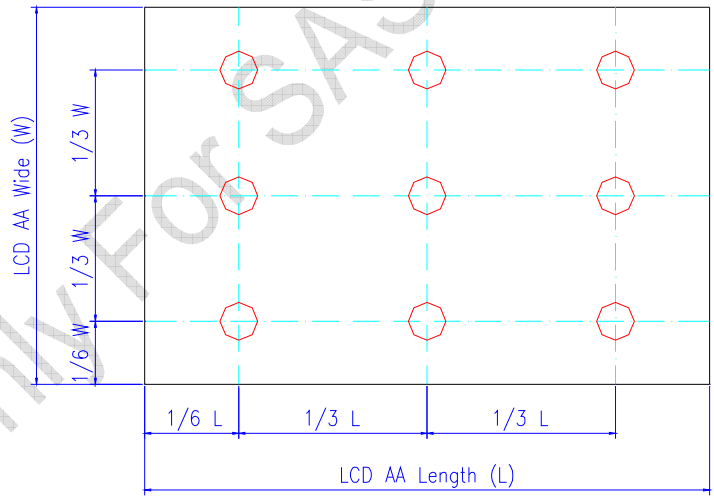
Note 7. Measured at the center area of the panel in gray level 255

Note 8. Measured at the center area of the panel in gray level 255



WHITE規格規範	
x	y
0.280	0.310
0.315	0.310
0.340	0.340
0.340	0.350
0.310	0.350
0.280	0.320

Note 9. Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

Note 10. After Reliability Test.

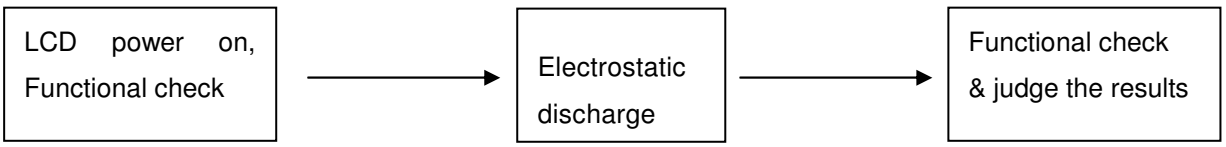
D. Reliability Test Items

No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 70℃ 240Hrs	
2	Low Temperature Storage	Ta= -30℃ 240Hrs	
3	High Temperature Operation	Tp= 60℃ 240Hrs	
4	Low Temperature Operation	Ta= -10℃ 240Hrs	
5	High Temperature & High Humidity	Tp= 60℃. 90% RH 240Hrs	Operation
6	Heat Shock	-25℃~80℃, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic Discharge	Air-mode : +/- 8kV Contact-mode : +/- 4kV	Note 3,4
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
10	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
11	Vibration (With Carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
12	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note 1. Ta: Ambient temperature.

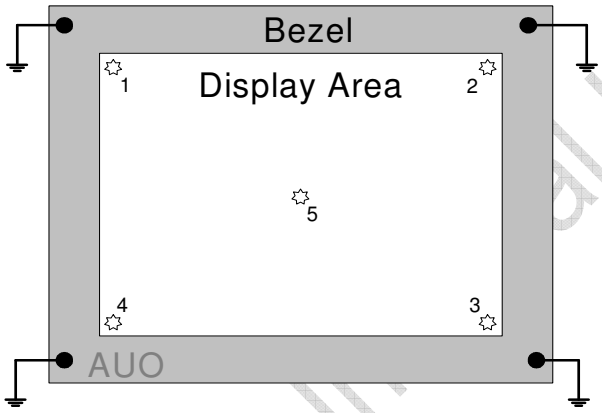
Note 2. (for test item1 to 6) Test method: chech with recovery time 2hrs in the laboratory environment.

Note 3. ESD Testing Flow as the below,



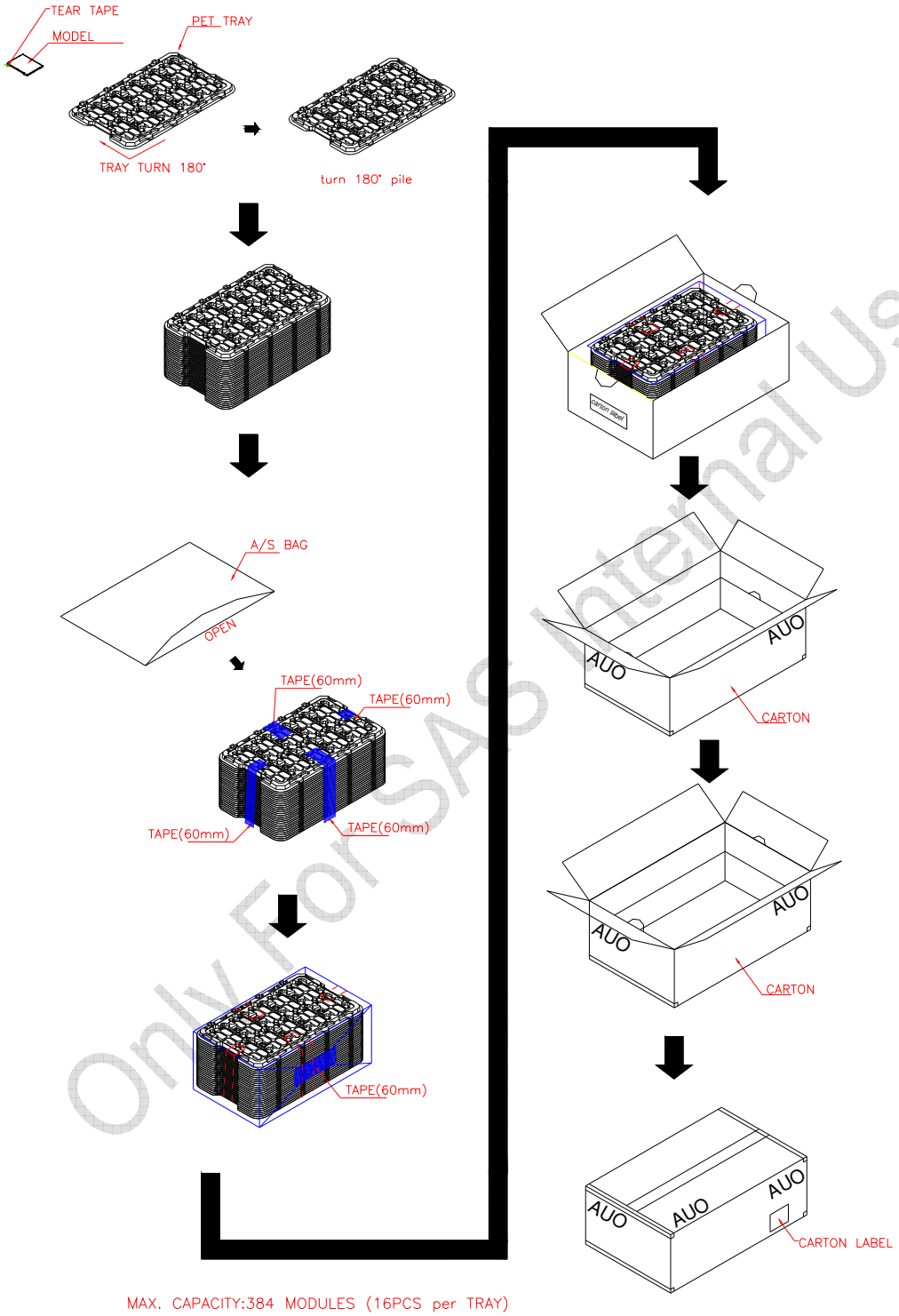
Note 4. ESD testing method.

1. Ambient: 24~26℃, 56~65%RH
2. Instruments:NoisekenESS-2000,
3. Operation System: “CX40FL-B”
4. Test Mode: Operating mode, test pattern: colorbar+8Gray scale
5. Test Method:
    a. Contact Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
    b. Air Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
6. Test point:



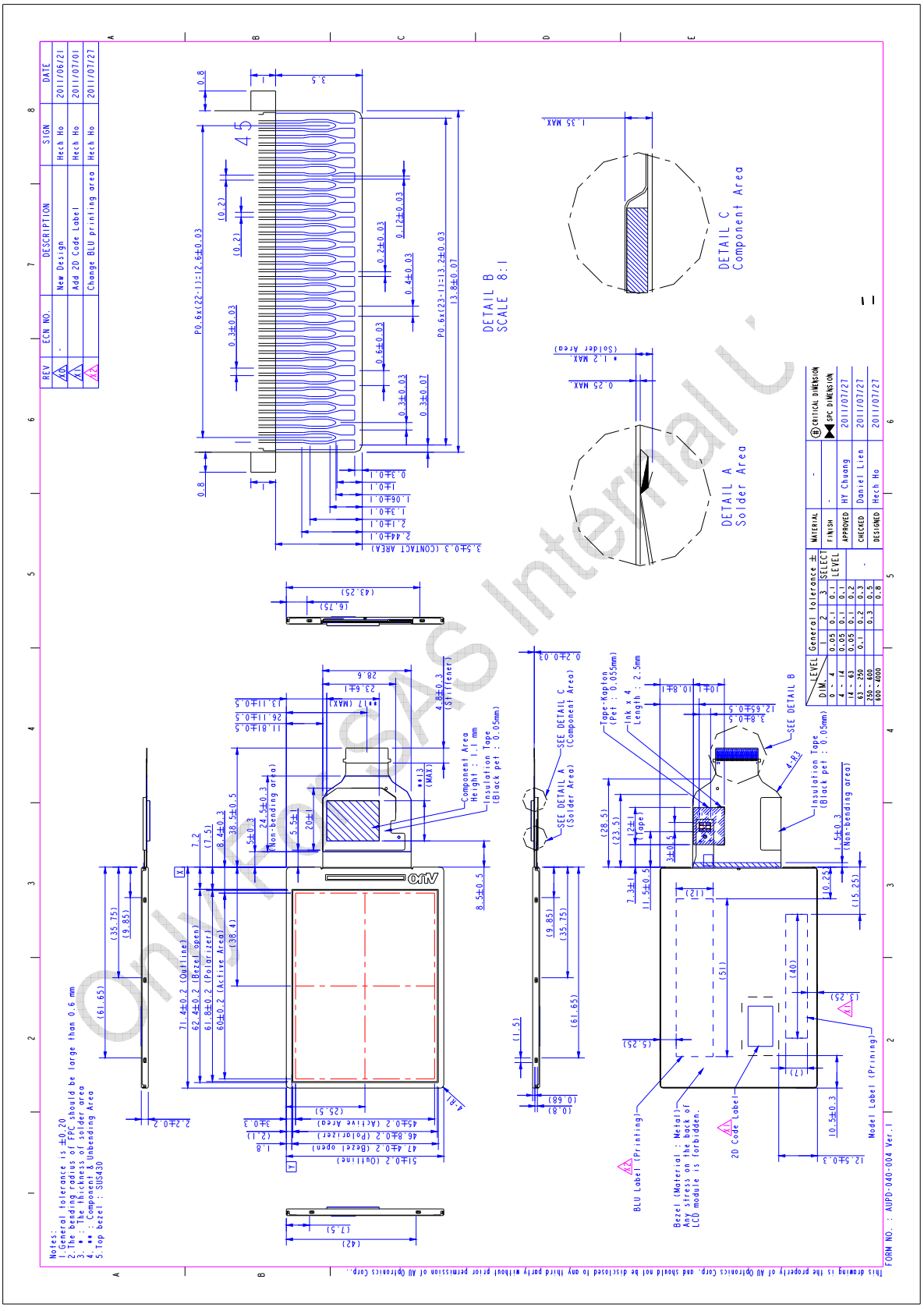
7. The metal casing is connected to power supply ground (0V) at four corners.
8. All register commands are repeating transfer.

E. Packing Form



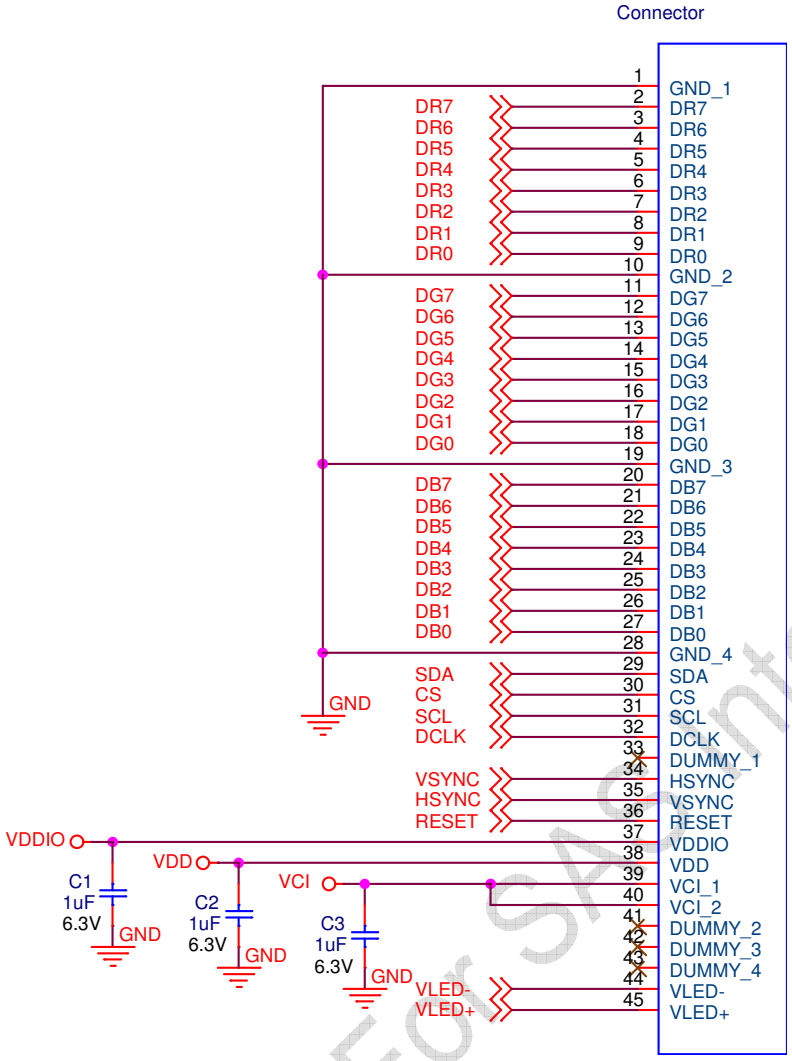
MAX. CAPACITY:384 MODULES (16PCS per TRAY)
MAX. WEIGHT: NA
Carton Outlines:520mm*340mm*250mm

F. Outline dimension



G. Application note

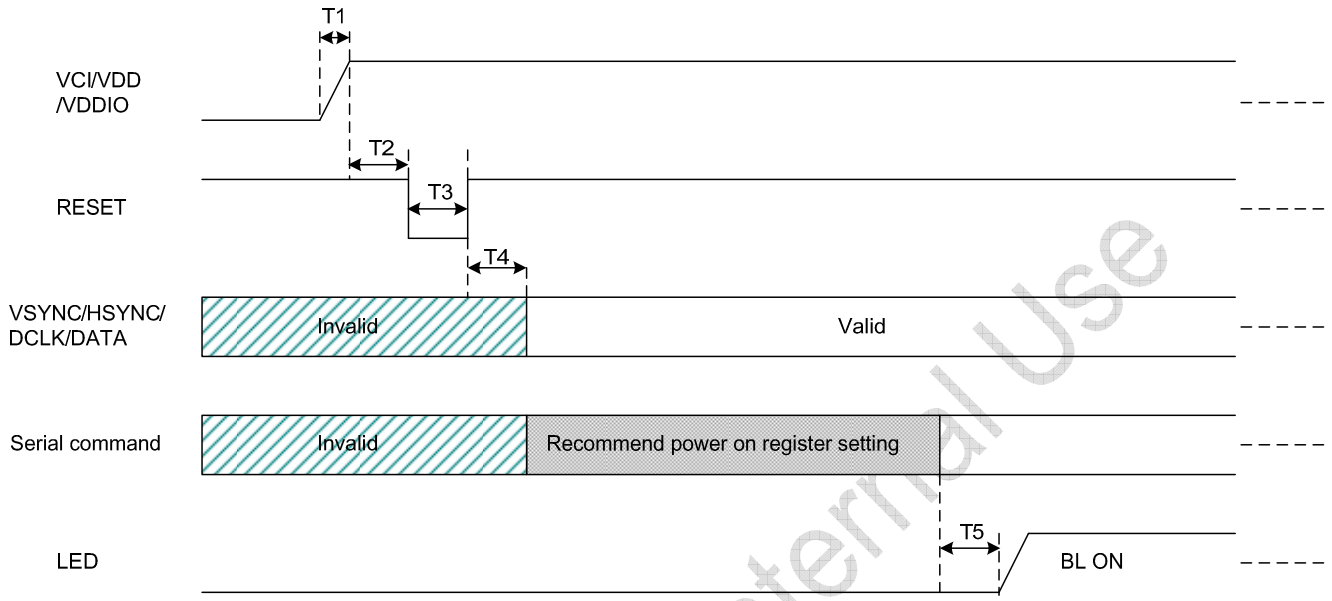
1. Application circuit



2. Power on/off sequence

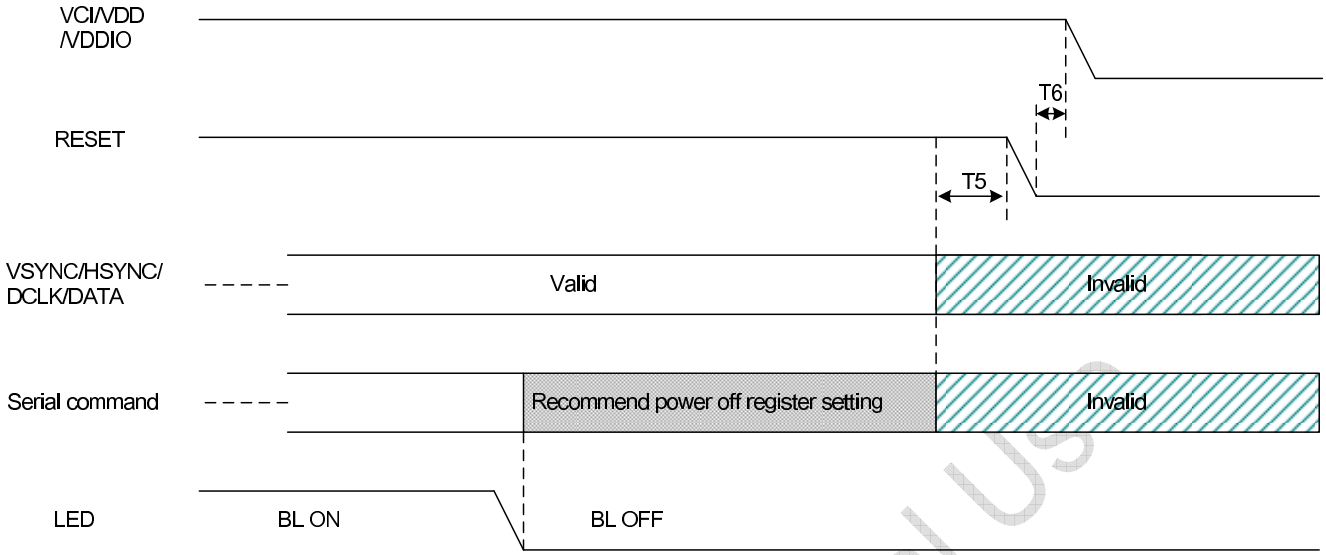
The register setting of standby mode disabling / enabling is used to control the build-in power on / off sequence.

2.1 Power on (Standby Disabling)



Note: 0ms<T1<15ms; T2≧1ms; T3≧1ms; T4≧1ms; T5≧185ms

2.2 Power off (Standby Enabling)



Note: T5≧120ms ;T6≧1ms;

3. Recommended power on/off serial command settings

3.1 Parallel RGB timing

a. Recommended Power On Register Setting

Number	Command(Binary)	Command(Hex)	Remark
1	0000 1010 0000 0011	0A03	Release STB
2	0000 0001 1111 1000	01F8	PRGB Timing
3	0000 1011 0111 0111	0B77	VGH, VGL
4	0000 1100 1100 1100	0CCC	Gamma
5	0000 1101 1100 1100	0DCC	
6	0000 1110 1010 1100	0EAC	
7	0000 1111 1000 1010	0F8A	
8	0001 0000 0000 1010	100A	
9	0001 0001 1100 1100	11CC	
10	0001 0010 1100 1100	12CC	
11	0001 0011 1010 1100	13AC	
12	0001 0100 1000 1010	148A	
13	0001 0101 0000 1010	150A	
14	0001 0110 1100 1100	16CC	
15	0001 0111 1100 1100	17CC	
16	0001 1000 1010 1100	18AC	
17	0001 1001 1000 1010	198A	
18	0001 1010 0000 1010	1A0A	

b. Recommended Power Off Register Setting

Number	Command(Binary)	Command(Hex)	Remark
1	0000 1010 0000 0010	0A02	STB

3.2 YUV timing

a. Recommended Power On Register Setting

Number	Command(Binary)	Command(Hex)	Remark
1	0000 1010 0000 0011	0A03	Release STB
2	0000 0001 1111 1001	01F9	YUV Timing
3	0000 1011 0111 0111	0B77	VGH, VGL
4	0000 1100 1100 1100	0CCC	Gamma
5	0000 1101 1100 1100	0DCC	
6	0000 1110 1010 1100	0EAC	
7	0000 1111 1000 1010	0F8A	
8	0001 0000 0000 1010	100A	
9	0001 0001 1100 1100	11CC	
10	0001 0010 1100 1100	12CC	
11	0001 0011 1010 1100	13AC	
12	0001 0100 1000 1010	148A	
13	0001 0101 0000 1010	150A	
14	0001 0110 1100 1100	16CC	
15	0001 0111 1100 1100	17CC	
16	0001 1000 1010 1100	18AC	
17	0001 1001 1000 1010	198A	
18	0001 1010 0000 1010	1A0A	

b. Recommended Power Off Register Setting

Number	Command(Binary)	Command(Hex)	Remark
1	0000 1010 0000 0010	0A02	STB

. Operating Precautions

1) Since front polarizer is easily damaged, please be cautious and not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or soft cloth.
5) Since the panel is made of glass, it may be broken or cracked if dropped or bumped on hard surface.
6) Do not open nor modify the module assembly.
7) Do not press the reflector sheet at the back of the module to any direction.
8) In case if a module has to be put back into the packing container slot after it was taken out from the container, do not press the center of the LED light bar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be damaged.

2. For Handing And System Design

(1) Do not scratch the surface of the polarizer film as it is easily damaged.

(2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.

(3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.

(4) Since this LCD panel is made of glass, dropping the module or banging it against hard objects may cause cracks or fragmentation.

(5) Certain materials such as epoxy resin (amine' s hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts (color change). Check carefully that gas from materials used in system housing or packaging do not hart polarizer.

(6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.

(7) Do not expose LCD module to the direct sunlight or to strong ultraviolet light for long time.

(8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.

(9) Do not disassemble the LCD module as it may cause permanent damage.

(10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below.

① Operators

Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body.

② Equipment and containers

Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower.

③ GND

To avoid ESD (Electro Static Discharde) damage, be sure to ground yourself before handling TFT-LCD Module.

④Humidity

Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.

⑤Transportation/storage

Storage materials must be anti-static to prevent causing electrostatic discharge.

⑥Others

Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

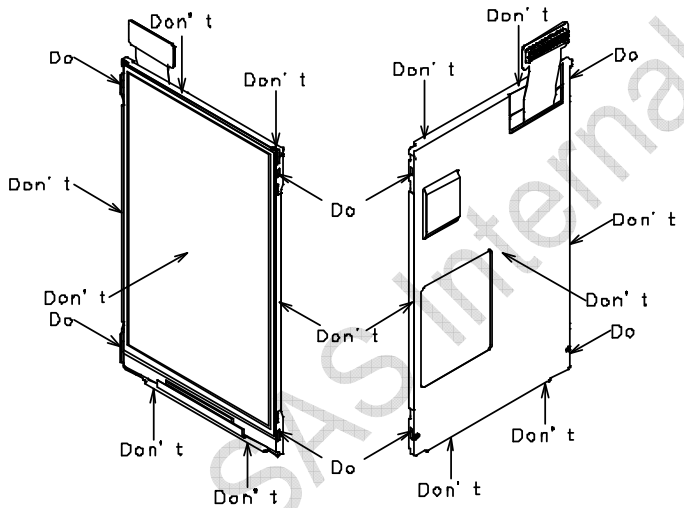
(11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress

or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.

(12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.

(13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers is also prohibited.

(14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel, COG and other electric parts are not damaged.



(15) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.

(16) LCD panel is susceptible to mechanical stress and even the slightest stress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

(17) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when peeling off this protective film. Ion blower and ground strap are recommended.

(18) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.

(19) This LCD module does not contain nor use any ODS (1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

3. For Operating LCD Module

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) At the shipment, adjust the contrast of each LCD module with electric volume. LCD contrast may vary from panel to panel depending on variation of LCD power voltage from system.

(3) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 ℃ and it becomes stable.

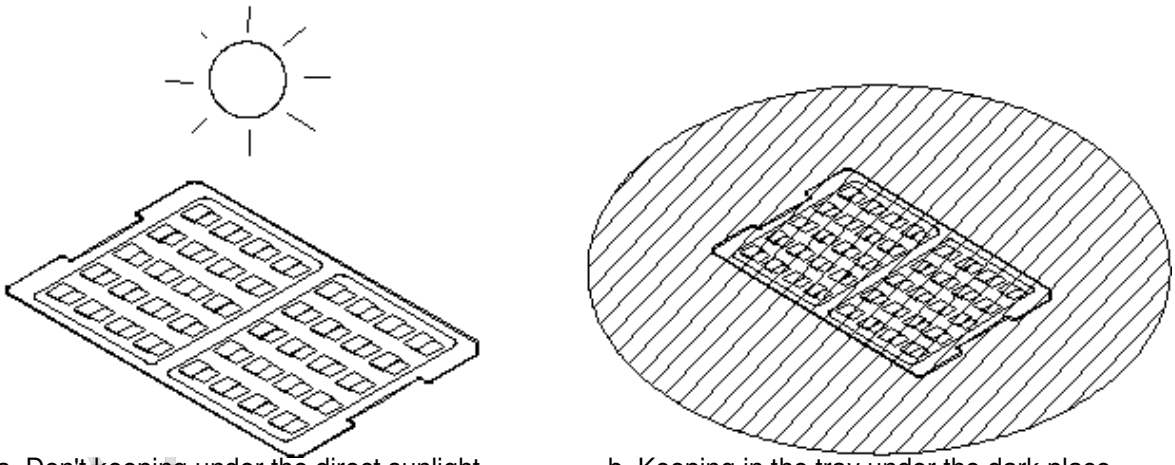
4. Precaution For Storage

(1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.

(2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity (25±5℃,60±10%RH) in order to avoid exposing the front polarizer to chronic humidity.

(3) Keeping Method

DON'T DO



a. Don't keeping under the direct sunlight. b. Keeping in the tray under the dark place.

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) Be sure to prevent light striking the chip surface.

5. Other Notice

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) As electrical impedance of power supply lines (VCC-GND) are low when LCD module is working, place the de-coupling capacitor near by LCD module as close as possible.

(3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.

(4) Generally, at power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.
(5) Don’ t touch to FPC surface, exposed IC chip, electric parts and other parts, to any electric, metallic materials.
(6) No bromide specific fire-retardant material is used in this module.
(7) Do not display still picture on the display over 2 hours as this will damage the liquid crystal.
(8) The connector used in this LCD module is the one AUO have not ever used.
Therefore, please note that the quality of this connector concerned is out of AUO's guarantee.

6. Precaution for Discarding Liquid Crystal Modules

COG: After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.
LCD panel: Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal panel only contains an extremely small amount of liquid crystal (approx.100mg) and therefore it will not leak even if the panel should break.
-Its median lethal dose (LD50) is greater than 2,000 mg/kg and a mutagenetic (Aims test: negative) material is employed.