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5.1" HD
Product Specification
Rev. P0

Customer Name	:	通用
Product Name	:	5.1" HD 720 AMOLED
Model Name	:	BF051FBM-AK1-7D02
Description	:	5.1" HD (720×1520) 16M Color

Proposed by			Customer's Approval
Designed	Checked	Approved	

Chengdu BOE Optoelectronics Technology CO., LTD

Revision History

Rev.	ECN No.	Description of Change	Date	Prepared
P0	-	-.Initial issue	2021.09.02	Hufei Yang

Content

1. General Description

1-1. Introduction

BOE 5.1” HD is a color active matrix AMOLED module using Low Temperature Poly-silicon TFT’s (Thin Film Transistors) as active switching devices. This module has a 5.1 inch diagonally measured active area with HD resolutions (720horizontal by 1520vertical pixel arrays). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors.

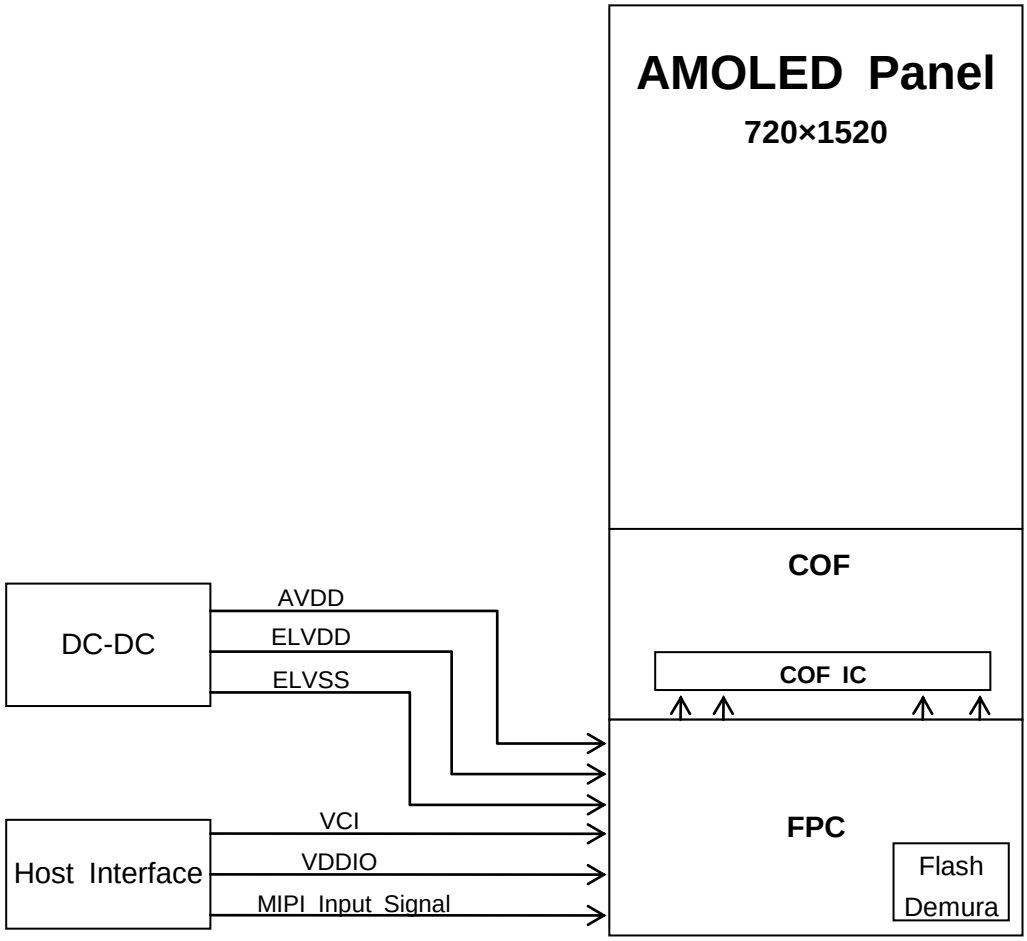

Figure 1

1-2. Driver IC Block Diagram

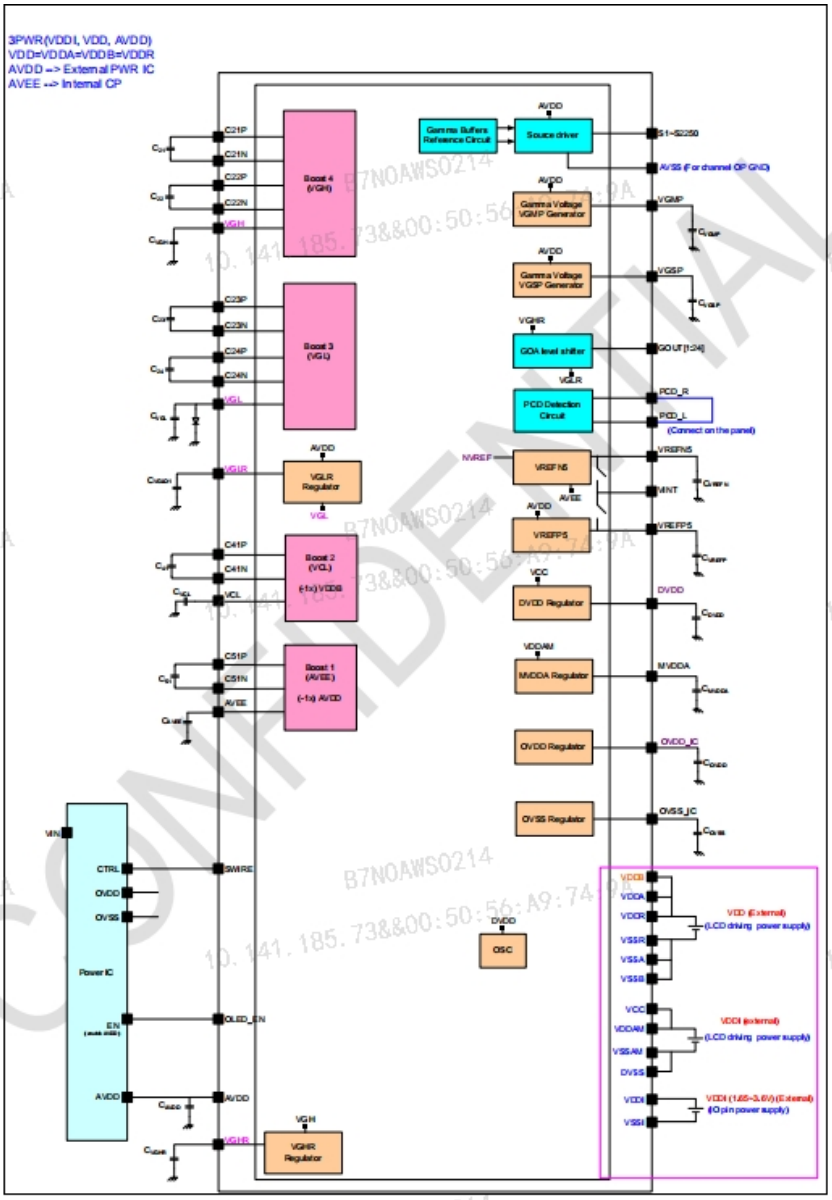

Figure 2

1-3. Features

1) AMOLED Display type with 3D Cover Glass
2) Display Format : 5.1” HD Real RGB : 720×1520
3) Interface : MIPI-DSI 4 lanes
4) Driver IC : RM692F9
5) Polarizer : CPOL(with PSA)+Flexible Touch Sensor

1-4. Application

- Smart Mobile Phone

2. Mechanical Specification

Table 1

Item	Specifications	Unit	Remark
Panel outline	57.604(W) × 120.584(H)×0.13(T)	mm	
Number of dots	720(W) × RGB × 1520(H)	Dots	HD
Active area	55.404(W) × 116.964(H)	mm	
Diagonal Inch	5.1	inch	
Pixel pitch	76.95(W) × 76.95(H)	um	
Pixel Arrangement	RGB		
Glass Thickness	0.57	mm	

3. Absolute Maximum Ratings

Table 2

Item	Symbol	Min.	Max.	Unit	Note
I/O Voltage	VDDIO	1.62	1.98	V	
Operation Voltage	VCI	2.60	3.60	V	
EL Driving Voltage	ELVDD	4.40	4.80	V	
	ELVSS	-5.00	-1.40	V	
Supply voltage (TSP)	VCC	2.7	3.6	V	
Operating temperature	Topr	-20	70	℃	
Storage temperature	Tstg	-40	80	℃	

4. Electrical Characteristics

Test Condition: Temp=25±2℃

Table 3

Item		Symbol		Condition	Min.	Typ.	Max.	Unit	Remark
ELVDD		ELVDD		-	4.40	4.60	4.80	V	
ELVSS		ELVSS		-	-5.0	-2.40	-1.40	V	Controlled by DDIC
AVDD		AVDD		-	5.40	6.70	7.60	V	
VCI		VCI		-	2.60	3.00	3.60	V	
VDDIO		VDDIO		-	1.62	1.80	1.98	V	
Current Consumption (Display)	Display on mode	IC	VCI	White pattern	-	3.76	-	mA	Full White
			VDDIO		-	16.53	-	mA	
			AVDD		-	14.2	-	m	

						2		A	
		Panel	ELVDD		-	138.5	-	mA	Full White
			ELVSS		-	138.8	-	mA	
Frame Frequency		F_{rm}		-	59	60	61	Hz	

Notes :

1. The value is just the reference value. The customer may optimize the setting value.
2. The current of Vin is just the reference value, because it depends on the efficiency of Power IC.
3. IC Power Consumption $P_{IC}=V_{VDDIO}*I_{VDDIO}+V_{VCI}*I_{VCI}+V_{AVDD}*I_{AVDD}$

EL Power Consumption $P_{EL}=V_{ELVDD}*I_{ELVDD}+V_{ELVSS}*I_{ELVSS}$

Total Power Consumption $P_{total}=P_{EL}+P_{IC}$

5. Electro-optical Characteristics

The test of optical specifications shall be measured in a dark room (ambient luminance ≤1lux and temperature = 25±2℃) with the equipment of Luminance meter. We refer to θ, Ø=0º (=θ_3) as the 3 o'clock direction (the "right"), θ, Ø=90º (= θ_{12}) as the 12 o'clock direction ("upward"), θ, Ø=180º (= θ_9) as the 9 o'clock direction ("left") and θ, Ø=270º (= θ_6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay.

Table 4

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Brightness			θ=0° At Center	315	350	385	cd/m^2	
Contrast ratio		CR	θ=0°	10,000:1	30,000:1	-	-	Note2
Brightness Uniformity		LRU	W255	80	85	-	%	Note3
Color of CIE coordinate	White	x_W	θ=0°	/	0.292	/	CIE 1931	Note4
		y_W		/	0.317	/		
	Red	x_R		0.65	0.68	0.71		
		y_R		0.29	0.32	0.35		
	Green	x_G		0.21	0.26	0.31		
		y_G		0.66	0.71	0.76		
	Blue	x_B		0.10	0.14	0.18		
		y_B		0.012	0.052	0.092		
Color Gamut			θ=0° vs. NTSC	84	100	-	%	
Gamma			-	2.0	2.2	2.4	-	
Life time	LT95		B10 BW	300			hrs	

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the panel surface (see Figure 3).

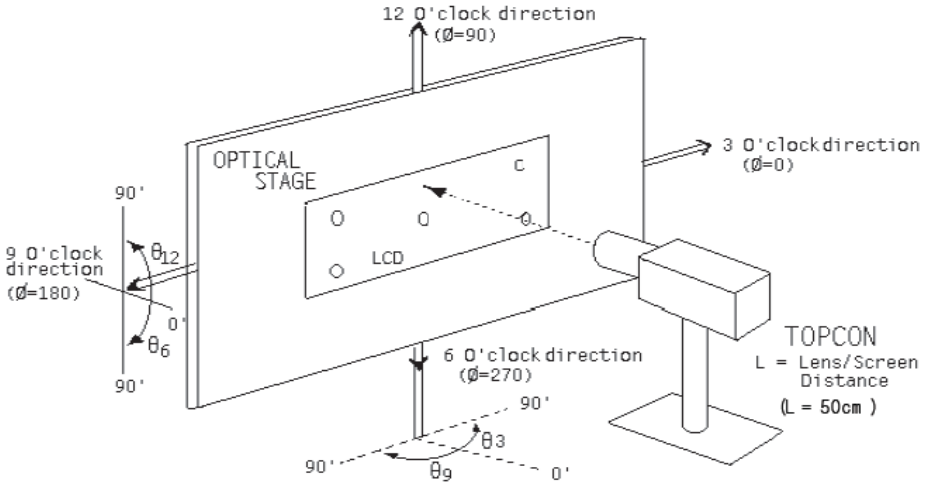

Figure 3

2. Contrast measurements shall be made at viewing angle of θ= 0º and at the center of the panel surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (see Figure 3) Luminance Contrast Ratio (CR) is defined mathematically.

$$\mathrm{CR} = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Uniformity. LRU Refer to figure as below：

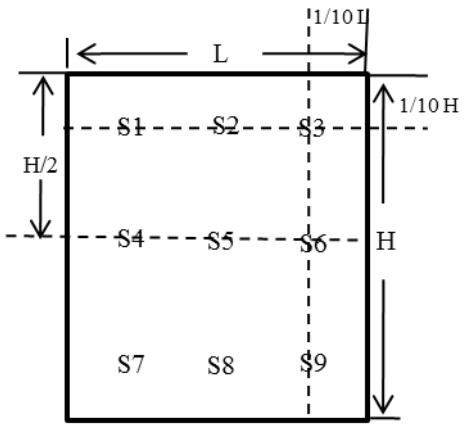

Figure 4

Uniformity measurements shall be made atθ=0° and at the different points of the panel surface. Luminance shall be measured with all pixels in the view field set to W/R/G/B at 255 Gary level, respectively.
Luminance uniformity=Lmin/Lmax ×100%

4. The color chromaticity coordinates specified in Table 4 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. FPC Pin Assignment

Main FPC assignment- AMOLED Panel Input/output Signal Interface.

Recommended connector: WP27D-P040VA3-R15000.

Table 5

No.	Name	Remark
1	GND	GND PIN
3	D3N	MIPI Data Lane 3-
5	D3P	MIPI Data Lane 3+
7	GND	GND PIN
9	D0N	MIPI Data Lane 0-
11	D0P	MIPI Data Lane 0+
13	GND	GND PIN
15	CKN	MIPI CLK Lane -
17	CKP	MIPI CLK Lane +
19	GND	GND PIN
21	D1N	MIPI Data Lane 1-
23	D1P	MIPI Data Lane 1+
25	GND	GND PIN
27	D2N	MIPI Data Lane 2+
29	D2P	MIPI Data Lane 2-
31	GND	GND PIN
33	ID (GND)	ID PIN
35	NC	NC
37	ELVSS	EL Low power
39	ELVSS	EL Low power
2	VPP(MTP_PWR)	MTP Power
4	ELON2(SWIRE)	Swire PIN（communication to DCDC）
6	VDDP_EN(OLEN_EN)	EN PIN（Enable signal communication to DCDC
8	TE	TE Flag PIN(communication to AP)
10	ERR_FG	ERR Flag Pin(communication to AP)
12	RESX(RETN)	Reset Signal
14	VDDI	1.8V VDDIO Power
16	NC	NC
18	VLIN1_7.6V(AVDD)	AVDD POWER
20	NC	NC
22	VCI_3.0V	VCI POWER
24	TSP_AVDD_3.3V	TSP Analog power
26	NC	NC
28	TSP_SDA	TSP Data Lane

30	TSP_SCL	TSP CLK Lane
32	TSP_INT	TSP initial signal PIN
34	TSP_RESET	TSP Reset PIN
36	NC	NC
38	ELVDD	EL High Power
40	ELVDD	EL High Power
41	GND	GND
42	GND	GND
43	GND	GND
44	GND	GND

<Pin layout ofB-to-Bcontact pads>

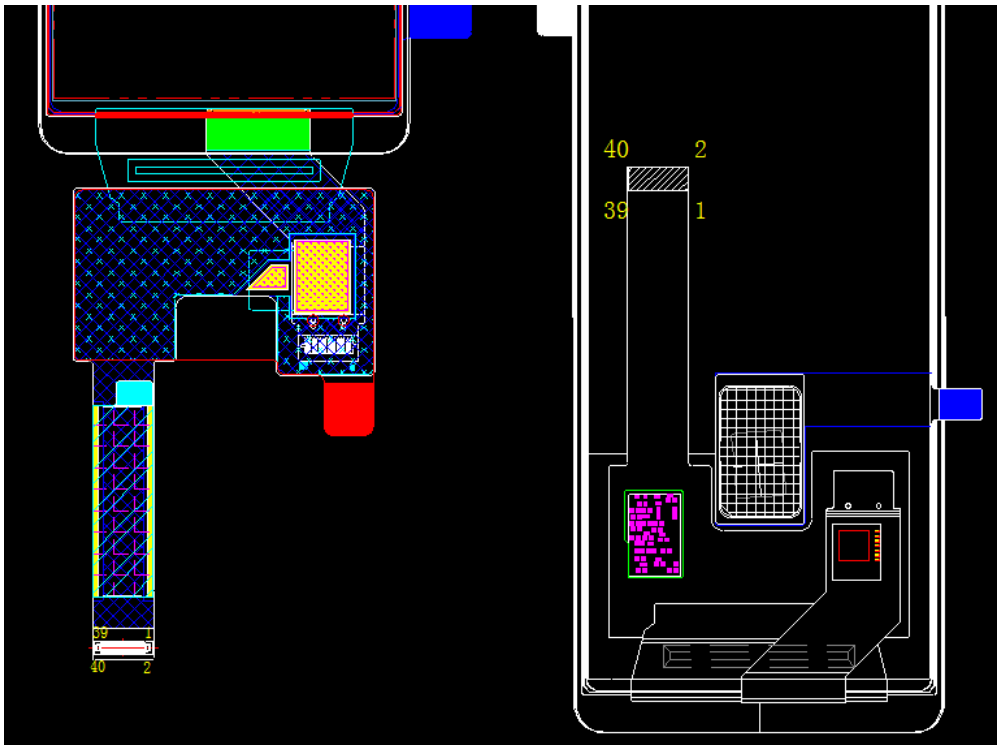

Figure5

7. AC Characteristics（For reference only)）

7-1. MIPI DSI Characteristics

7-1-1. DC Characteristics for MIPI DSI

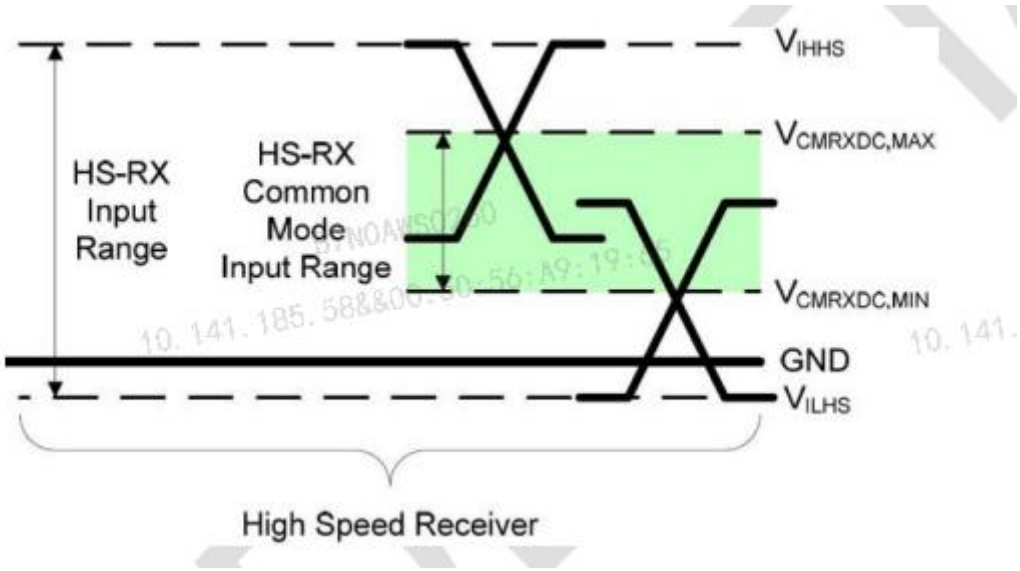

Figure 6 MIPI DSI Signaling Levels

Table 6

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit
HS_RX	V_{IDTH}	Differential input high threshold	-	-	70	mV
	V_{IDTL}	Differential input low threshold	-70	-	-	
	V_{IHHS}	Single-ended input high voltage	-	-	460	
	V_{ILHS}	Single-ended input low voltage	-40	-	-	
	$V_{TERM-EN}$	Single-ended threshold for HS termination enable	-	-	450	
	$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70	-	330	
	Z_{ID}	Differential input impedance	-	100	-	Ω
LP_RX	V_{IL}	Logic0 voltage not in ULP State	-	-	550	
	V_{IH}	Logic1 input voltage	880	-	-	mV
	V_{LEAK}	I/O leakage current	-10	-	10	uA
LP_TX	V_{OL}	The venin output low level	-50	-	50	mV
	V_{OH}	The venin output high level	1.1	1.2	1.3	V
	Z_{OLP}	Output impedance of LP transmitter	110	-	-	Ω

7-1-2. MIPI DSI High-Speed RX Clock and Data-Clock Timing

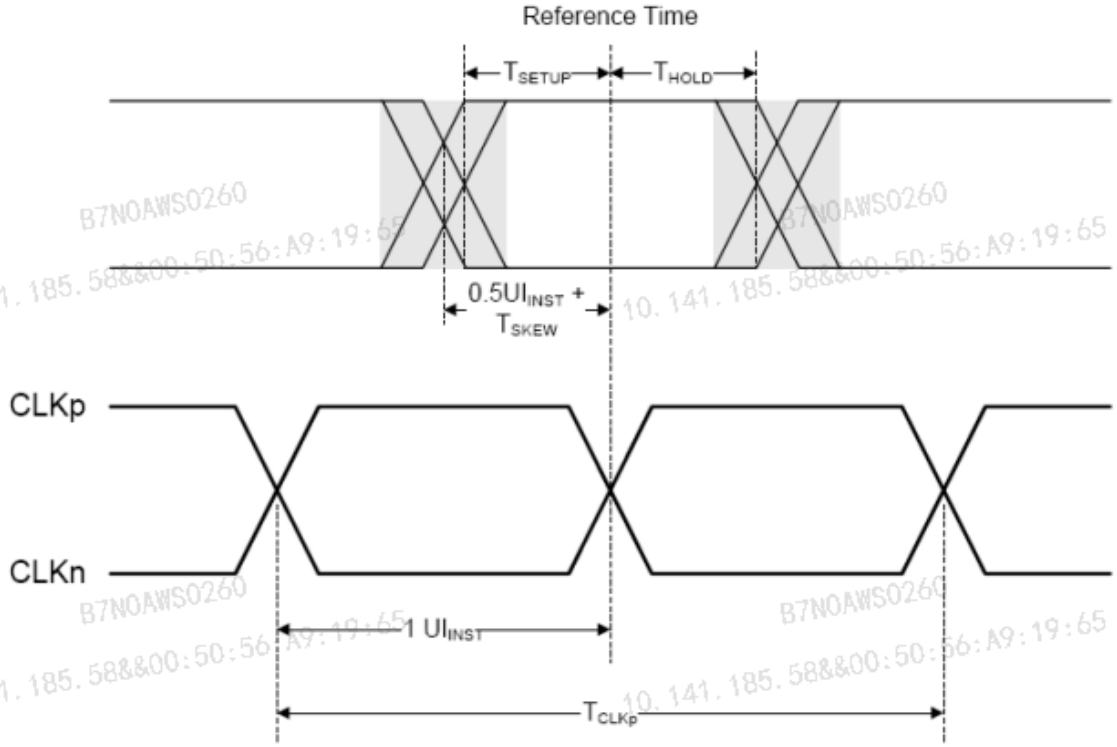

Figure 7 MIPI Data to Clock Timing Definitions

Table 7-1(Actual Value)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{DSICLK}	DISCLK Frequency	VDDI=1.65~3.3V	T.B.D.		550	MHz
T_{CLKP}	DSICLK Cycle time		1		10	Ns
T_{DSIR}	DSI Data Transfer Rate		T.B.D.		1100	Mbps
$T_{SKEW[TX]}$	Data to Clock Skew		-0.15		0.15	UI_{INST}
T_{SETUP}	Data to Clock Setup time		0.15	-	-	UI_{INST}
			0.15	-	-	ns
T_{HOLD}	Data to Clock Hold time		0.15	-	-	UI_{INST}
			0.15	-	-	ns
UI_{INST}	UI instantaneous		1		12.5	ns

Table 7-2(Design Value)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{DSICLK}	DISCLK Frequency	VDDI=1.65~3.3V	T.B.D.		500	MHz
T_{CLKP}	DSICLK Cycle time		1		10	Ns
T_{DSIR}	DSI Data Transfer Rate		T.B.D.		1000	Mbps
$T_{SKEW[TX]}$	Data to Clock Skew		-0.15		0.15	UI_{INST}
T_{SETUP}	Data to Clock Setup time		0.15	-	-	UI_{INST}
			0.15	-	-	ns
T_{HOLD}	Data to Clock Hold time		0.15	-	-	UI_{INST}
			0.15	-	-	ns
UI_{INST}	UI instantaneous		1		12.5	ns

7-1-3. Global Operation Timings

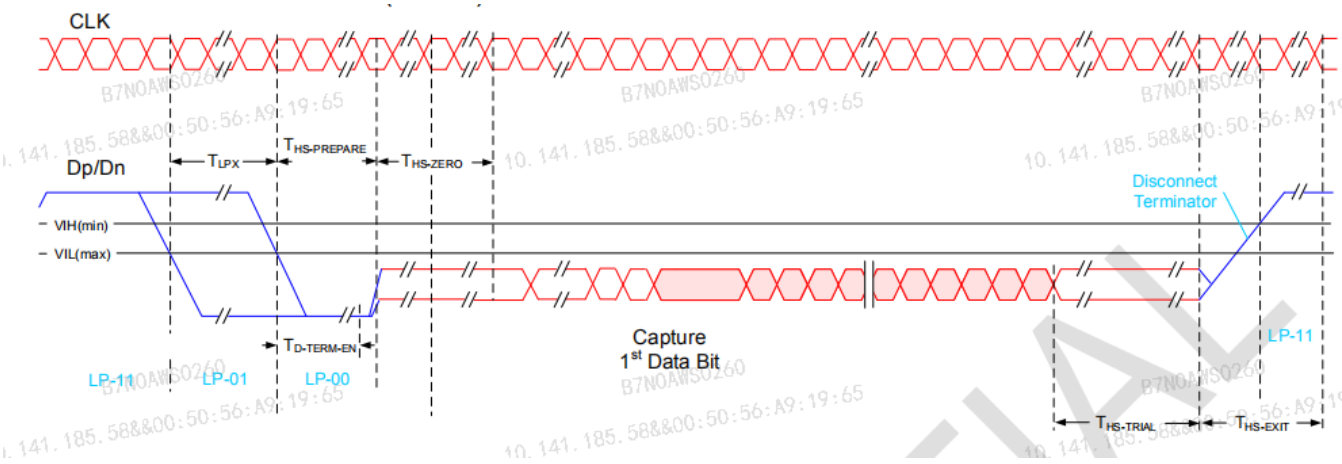

Figure8 MIPI HS Data Transmission in Bursts

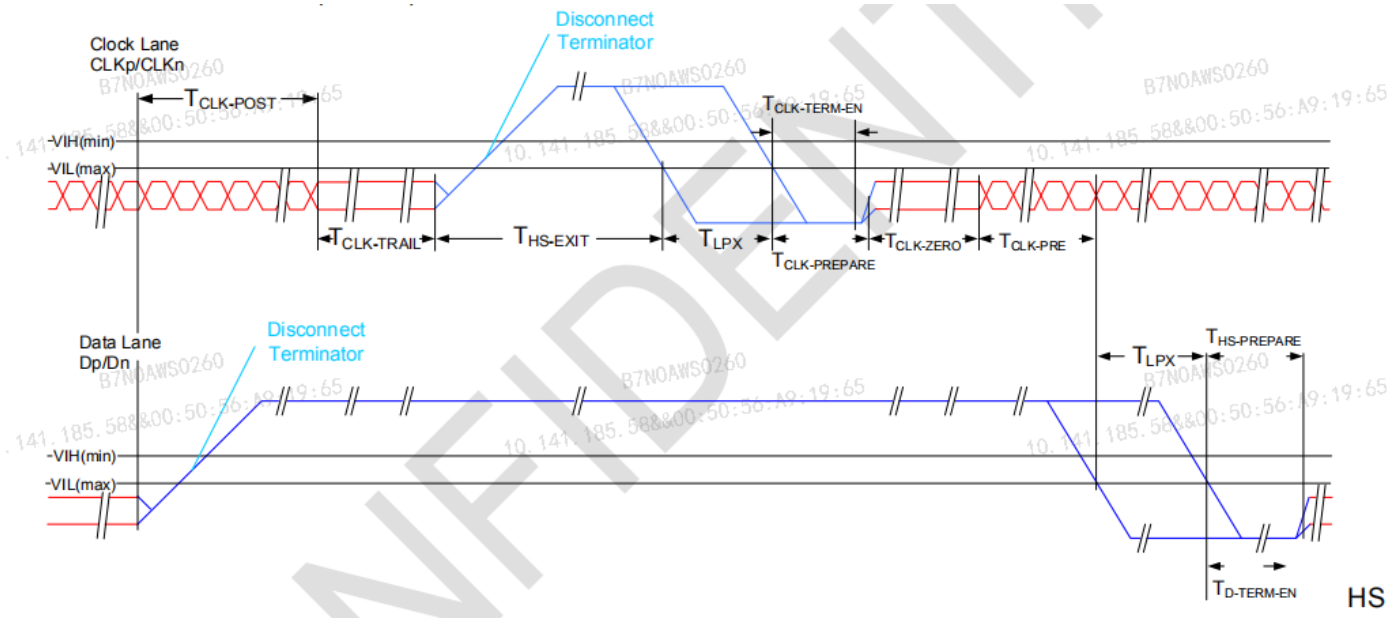

Figure9 MIPI switching the Clock Lane between Clock Transmission and LP mode

Table 8

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to beginning of $T_{CLK-TRAIL}$	60 ns +52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driver by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	UI

$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-00 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE.}$	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dncrosses V_{ILMAX}.	Time for Dn to reach VTERM-EN	-	38	ns
$T_{CLK-TRAL}$	Time that the transmitter drives the HS-00 state after the last payload clock bit of a HS HS transmission burst.	60	-	-	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + Time to that the transmitter drives the HS-00 state prior to starting the clock.	300	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses V_{ILMAX}.	Time for Dn to reach VTERM-EN	-	35ns+4*UI	-
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAL}$, to the start of the LP-11 state following a HS burst.	-	-	105 ns +n*12*UI	-
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following HS burst.	100	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-00 Line state starting the HS transmission.	40ns+4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI	-	-	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions , starting from the beginning of $T_{HSPREPARE}$	85 ns + 6*UI	-	145 ns +10*UI	ns
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40	-	55 ns + 4*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	Max(n*8*UI, 60ns +n 4* UI)	-	-	ns
T_{INIT}	-	-	-	-	-
T_{LPX}	Transmitted length of any Low-Power state period	-	56.6	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MARSTER)}$/$T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	

T_{TA-GET}	Time that the new transmitter drives the bridge state (LP-00) after accepting control during a Link Turnaround.	$5*T_{LPX}$			ns
T_{TA-GO}	Time that the new transmitter drives the bridge state (LP-00) before releasing control during a Link Turnaround.	$4*T_{LPX}$			ns
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link turnaround.	T_{LPX}	-	$2*T_{LPX}$	ns
T_{WAKEUP}	Time that a transmitter drivers a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms

7-1-4. AC Characteristics of MIPI DSI Characteristics

Table 9

Symbol	Parameter	Min.	Typ.	Max.	Unit
Thost-enable	Host output enable time	0	-	24*t-bit	ns
Thost-disable	Host output disable time, entire length of the Turnaround 1 field	0	-	24*t-bit	
Tclient-enable	Client output enable time, entire length of the Turnaround 1 field	0	-	24*t-bit	
Tclient-disable	Client output disable time, measured from the end of the last bit of the Turnaround 2 field.	0	-	24*t-bit	

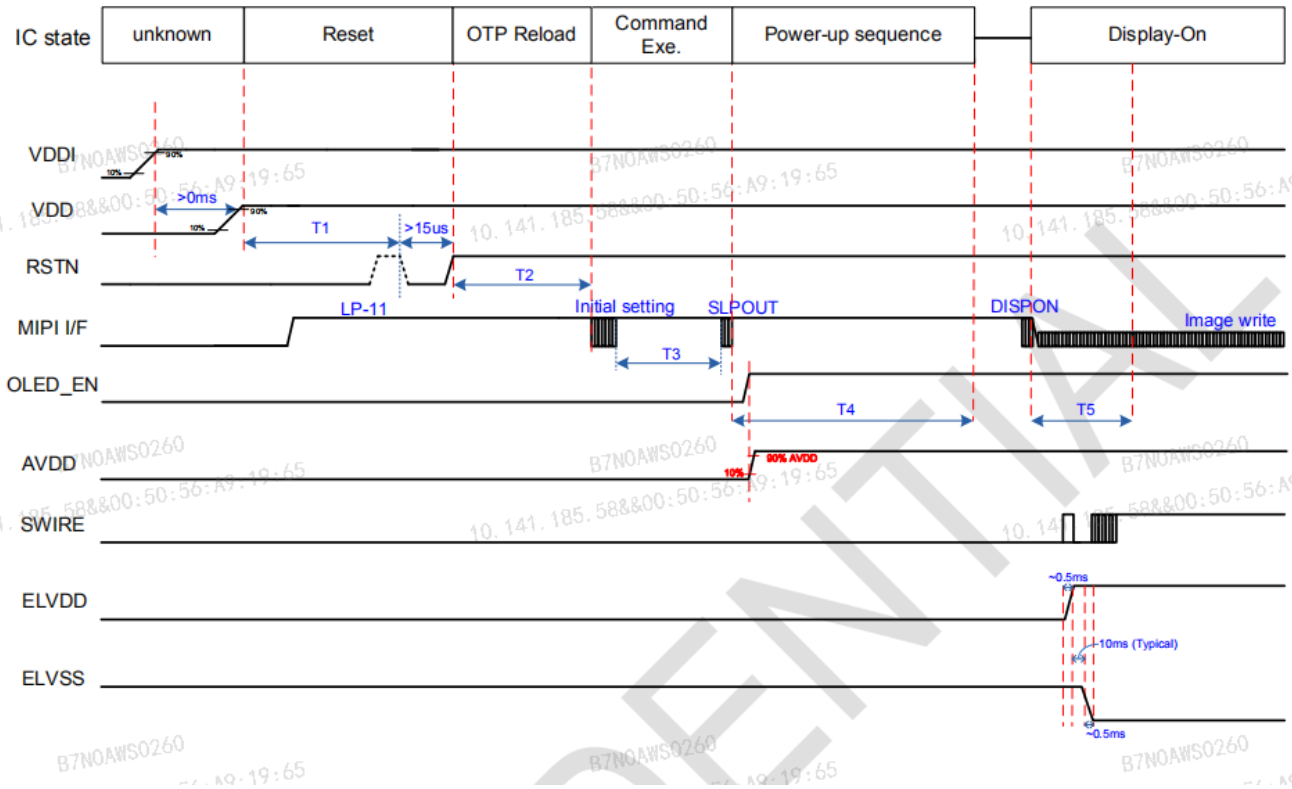

Figure10

7-2. Touch Panel I2C Timing Characteristics(EE)

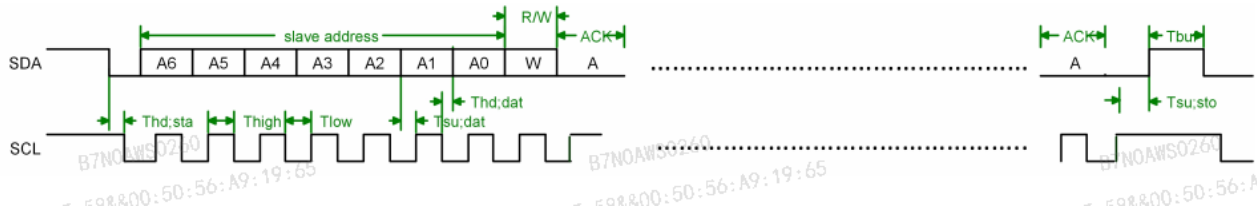

Figure 11

Table 10

Parameter	Symbol	Min.	Max.	Unit
SCL Low Period	t_{lo}	1.3	-	us
SCL High Period	t_{hi}	0.6	-	us
SCL setup time for START condition	t_{st1}	0.6	-	us
SCL setup time for STOP condition	t_{st3}	0.6	-	us
SCL hold time for START condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

7-3. Touch panel external reset timing

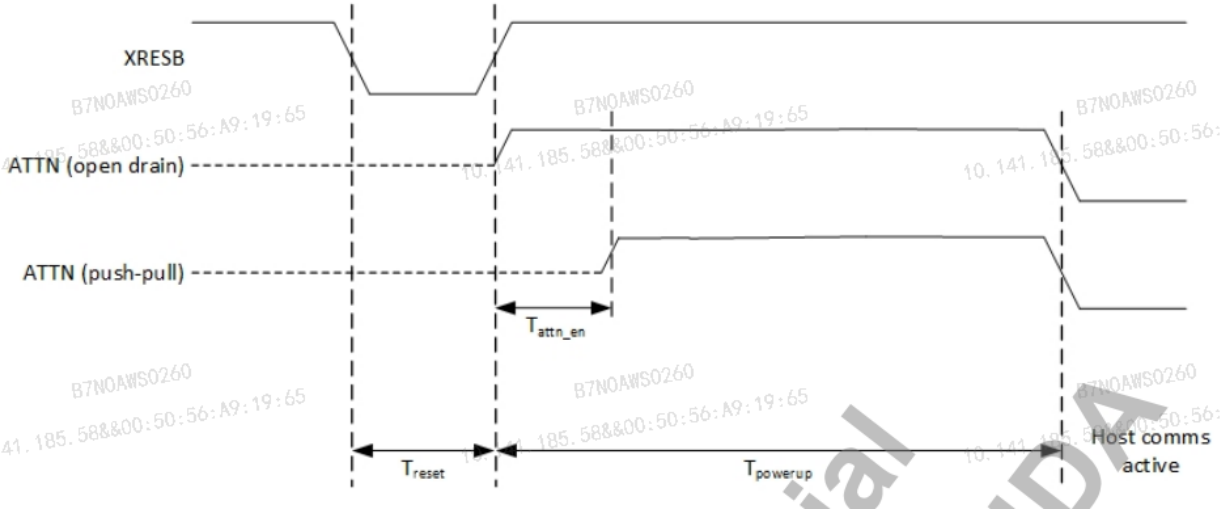

Figure 12

8. Recommended Operating Sequence

8-1. Display Power on/off Sequence

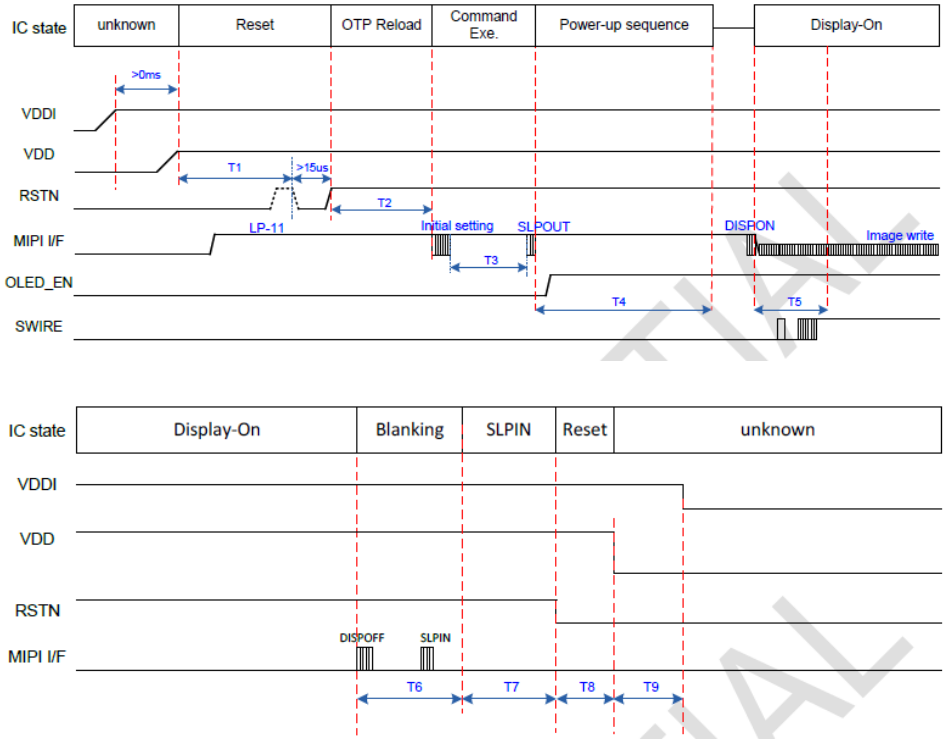

Figure 13Power On/Off Sequence

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	10	-	-	ms	Effective hardware reset period
T2	10	-	-	ms	OTP reload time
T3	0	-	-	ms	Initial code input finish to SLPOUT command input
T4	-	96	-	ms	Normal power-up sequence
T5	2	-	-	VS	Display-On Blanking region

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T6	2	-	-	VS	Display-Off blanking region
T7	1	-	-	VS	Blanking region
T8	1	-	-	ms	Effective hardware reset period
T9	2	-	-	ms	Power off period

Figure 14

8-2. Touch Panel Power on Sequence

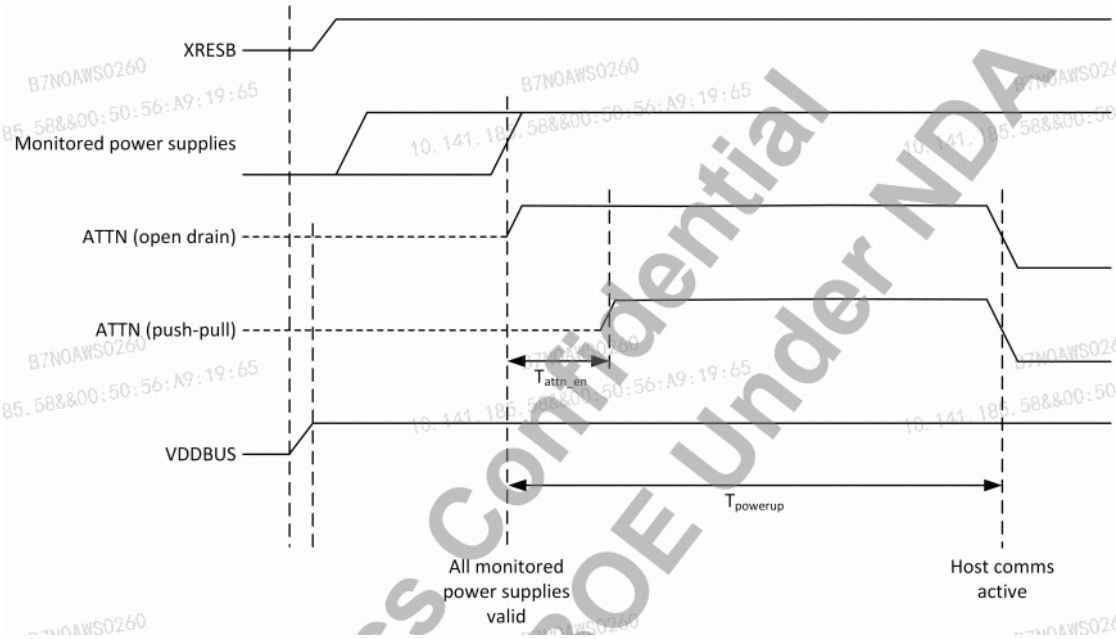

Figure 15

8-4. Initial Code

Version: Rev0.
Diagonal Inch: 5.1
Driver IC: RM692F9

Table11MIPISetting

LABEL	SETTING	VALUE
(number)	Lane	4
MIPI mode	CMD or Video	
1	x-size	720
2	y-size	1520
3	HBP	38
5	HFP	26
6	VBP	8
7	VSW	17

8	VFP	16
9	DCLK_POL	

Table12PowerSetting

Item	Voltage	Setting
input	VDDI	1.8
	VCI	3
	AVDD	
	ELVDD	4.6
	ELVSS	-2.4
output	VGH	6.6
	VGL	-6
	Vref	/

Table13

Enter AOD	FE	00
	39	00
Exit AOD	FE	00
	38	00

HBM 可直接切 DBV

9. Outline Information

9-1. Total Outline

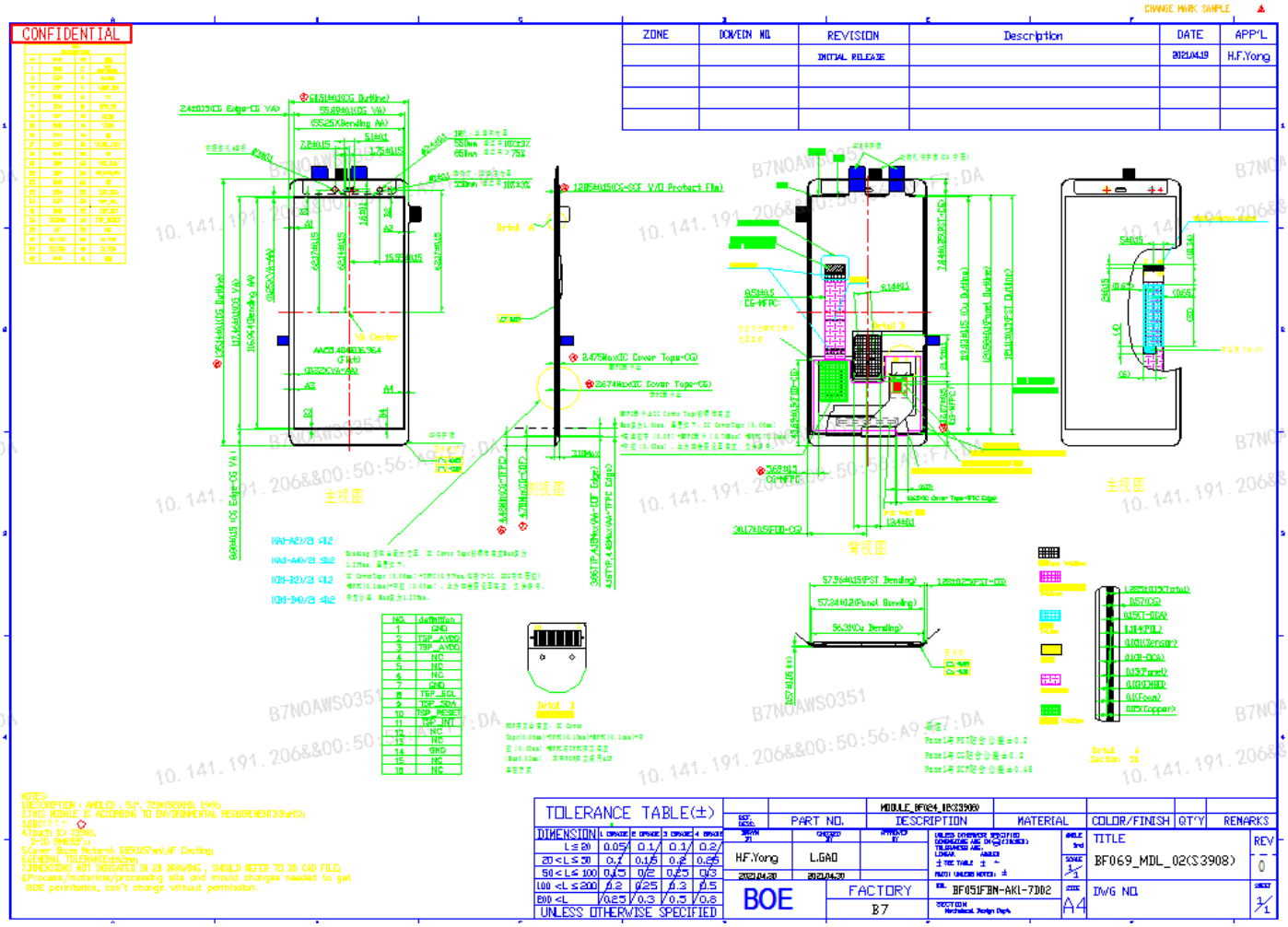

Figure15

9-2. Main FPCB Drawing

9-2-1.Main FPC Schematic Diagram

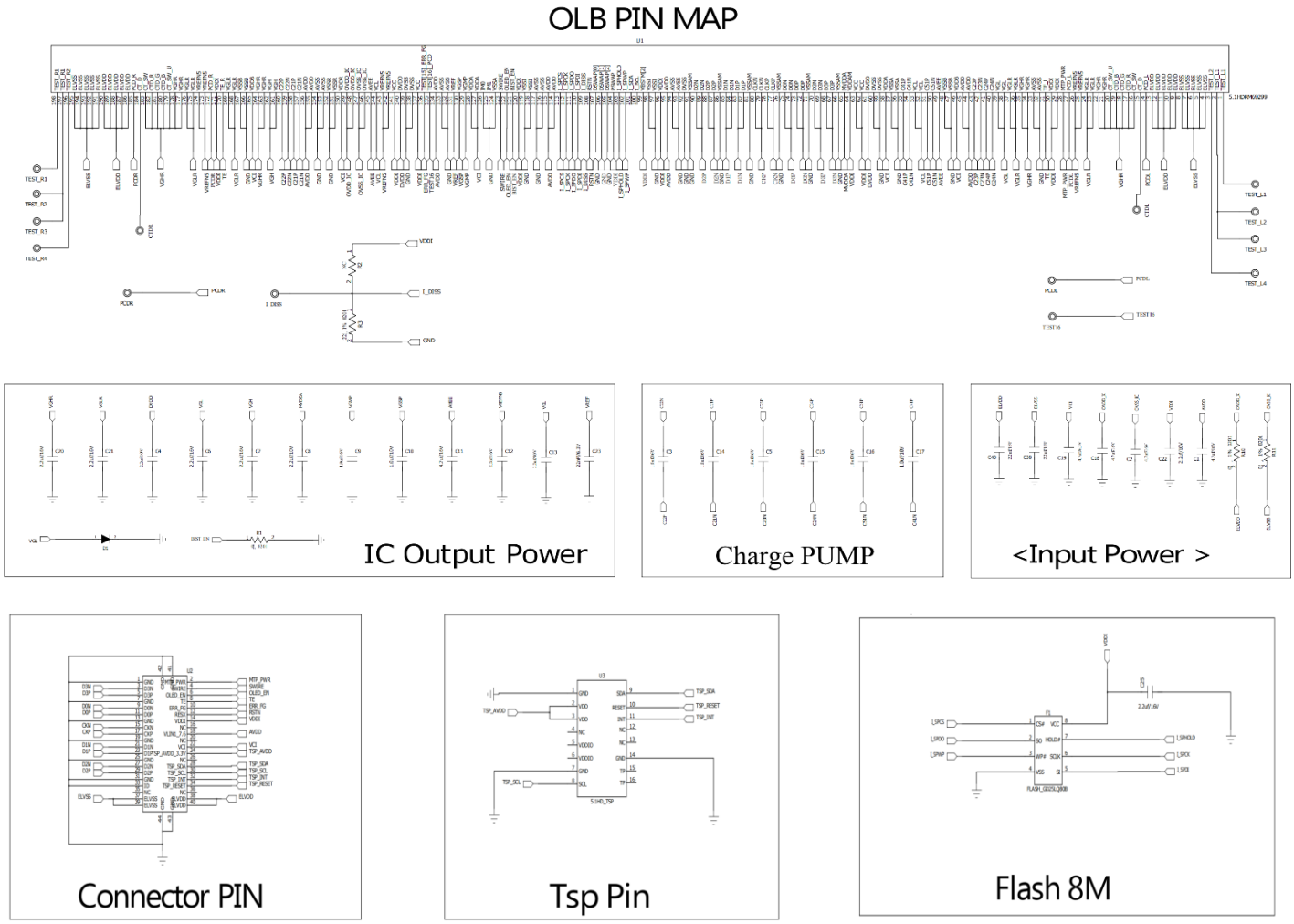

Figure16

9-2-2.Main FPC Electronic Part List

Table 14

CATEGORY	REFRENCE	SPECIFICATION	VALUE	耐压值	封装	材质	Q'ty	MAKER
CAPACITOR	C20-21,C6-7,C25, C12,C40,C38		2.2uF	16V	0402	X5R	8	
	C4		2.2uF	10V	0402	X5R	1	
	C9,C3,C14,C5,C15,C16		1.0uF	16V	0402	X5R	6	
	C11,C18,C2,C1		4.7uF	16V	0402	X5R	4	
	C12,C40,C38		2.2uF	16V	0402	X5R	3	
	C10,C17		1.0uF	10V	0402	X5R	2	
	C23		22nF	6.3V	0201	X5R	1	
	C8,C13,C22		2.2uF	10V	0201	X5R	3	
	C19		4.7uF	6.3V	0402	X5R	1	
Resistor	R10,R11,R1		0Ω		0201		3	5%
	R3		220Ω		0201		1	1%
DIODE	D1	LRB521S-30T1G					1	
FLASH	F1	GD25LQ80CEIGR					1	

9-2-3.Main FPC Placemen

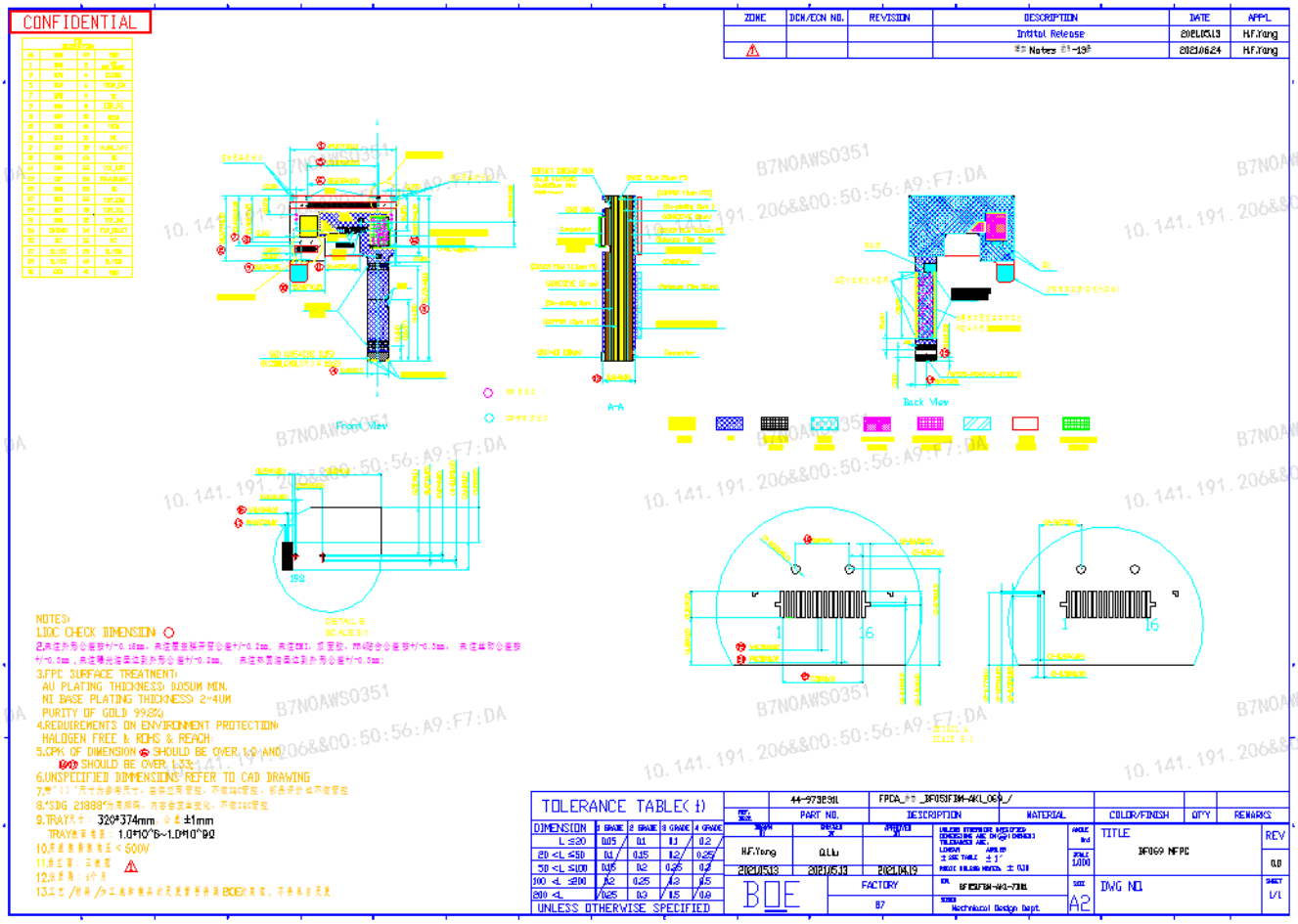

Figure17

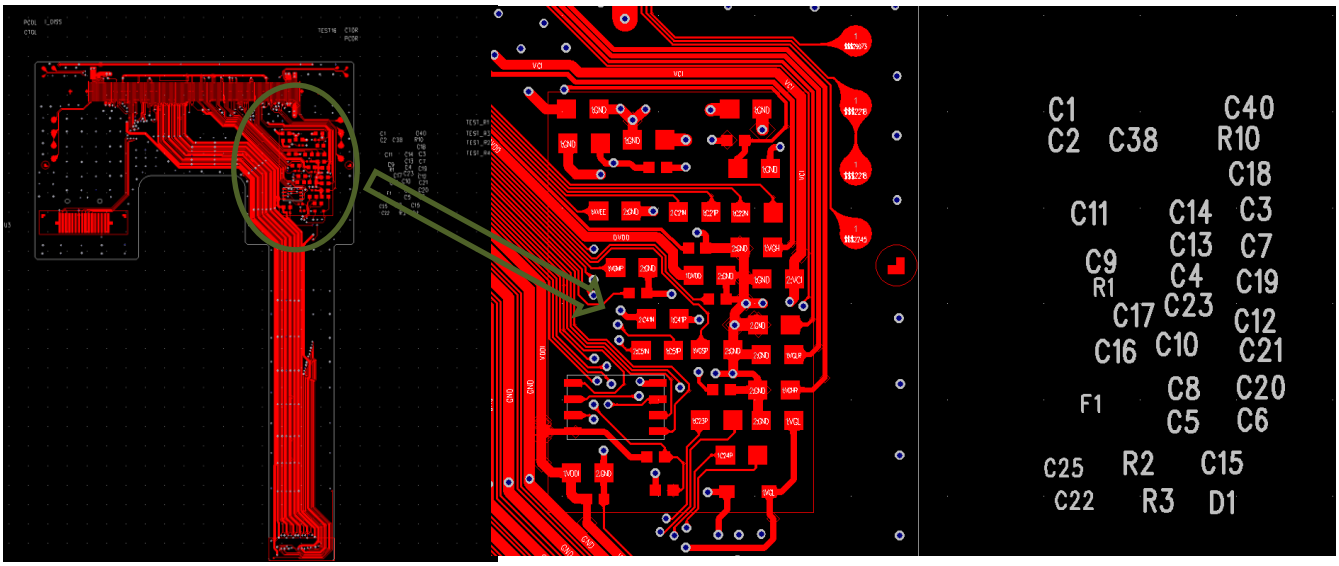

Figure18

9-3. TSP FPCB Drawing

9-3-1.TSP FPC Schematic Diagram

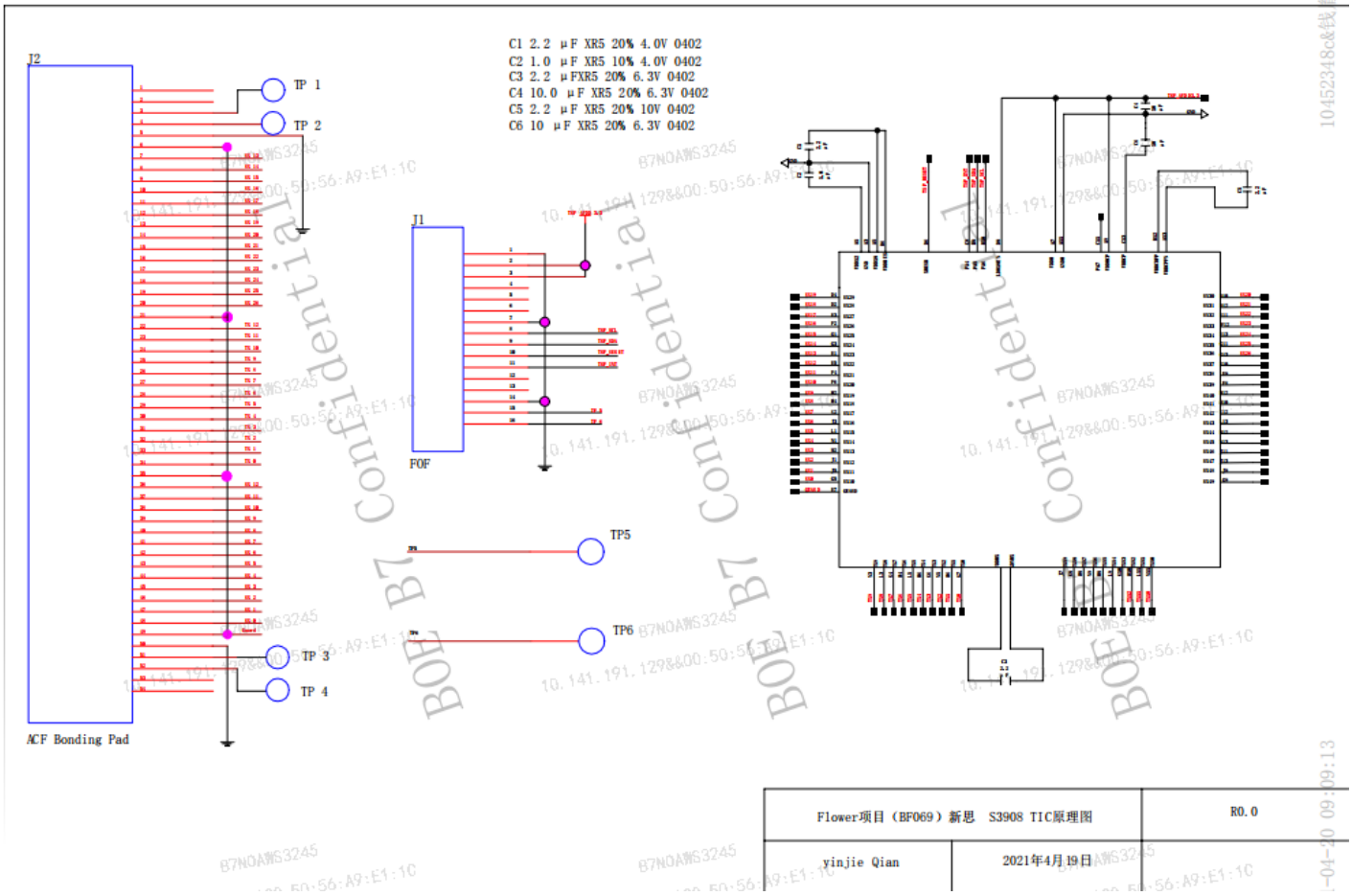

Figure19

9-3-2.TSP FPC Electronic Part List

Table 15

CATEGORY	REFERENCE	SPECIFICATION	VALUE	耐压值	封装	材质	Q'ty	MAKER
CAPACITOR	C1、C3、C5		2.2uF	4V	0402	X5R	10	厂商 Taiyo,Murata
	C4、C6		10uF	6.3V	0402	X5R	10	
	C2		1.0	4	0402	XR5	10	

9-3-3.TSP FPC Placement

Figure20

10. Reliability

10-1. Environmental test

Table 16

No.	Item	Condition	Qnty	Result	Judgment Criterion
1	HTS	80℃,storage ,120hr	10 ea	OK	1. No clearly visible defects or remarkable deterioration of display quality. However, any polarizer's deteriorations by the high temperature/ High humidity Storage test and the High temperature/ High humidity Operation test are permitted; 2. No function-related abnormalities; 3. Optical criteria: White △u'v' ≤0.02.
2	LTS	-40℃,storage ,120hr	10 ea	OK	
3	THO	60℃,90%RH,operation ,120 hr	10 ea	OK	
4	HTO	70℃,operation ,120hr	10 ea	OK	
5	LTO	-20℃,operation ,120hr	10 ea	OK	
6	TST	-40℃~80℃, 1h/Cycle,100 Cycles	10ea	OK	
7	Hast	110℃,85%RH, storage ,8hr	10 ea	OK	

10-2. other test

Table 17

No.	Item		Condition	Qnty	Result	Judgment Criterion
1	ESD	Air	±2/4/8kV(9 points on the CG surface，More than ±8kV except chip position)	5ea	OK	1. No clearly visible defects or remarkable deterioration of display quality. However, any polarizer's deteriorations by the high temperature/ High humidity Storage test and the High temperature/ High humidity Operation test are permitted; 2. No function-related abnormalities; 3. Optical criteria: White△u'v' ≤0.02.
		Contact	±2/4/6kV(FPC Copper leakage)	5 ea	OK	
2	Box Vibration		Random Vibration 1 Corner, 3 Edges,6 Surfaces	1Box	OK	

11. Handling Precautions

11-1. Mounting Method

The AMOLED panel module can easily get damaged. Since the module is constructed as to be fixed by utilizing fitting holes in the printed circuit board. Extreme care should be used when handling the AMOLED modules.

11-2. Caution of AMOLED Handling and Cleaning

When cleaning the display surface, use soft cloth solvent as recommended below and wipe gently.

- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface. Do not use the following solvent.

- Water
- Ketone
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns. Do not use the following solvent on the pad and prevent it from being contaminated.

- Soldering flux
- Chlorine(Cl), Sulfur(S)
- Spittle, Fingerprint

If the product is not wrapped with a desiccant added pad, ITO pattern can be damaged by corrosion. BOE suggests wrapping a product with a desiccant unless customers particularly indicate that they do not want it. In case ITO pattern corrodes due to the usage of chlorine, sulfur or customer's mishandling of the product, the responsibility lies with the customer.

11-3. Caution against Static Charge

For AMOLED module, use C-MOS LSI drivers, therefore we recommend that you ; Connect any unused input terminal to Panel, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity. It could occur static electricity when taping off the film which protects AMOLED. Against static charge, you should make sure that the product is safe or not by experiment in advance.

11-4. Packing

- The packing principle is that AMOLED module should keep its packing condition at the time of delivery.
- For safety & avoiding the module damage, Carton box must stack the below 4 boxes. When storing the AMOLED after unpacking, note the followings.
- AMOLED module is consisted of flexible materials. It should avoid pressure, especially the back and edgeof the product. It should avoidstrong impact, and being dropped from a height.
- To prevent modules from degradation, do not operate or store them in a place where they are directly exposed to sunlight or high temperature/humidity.

11-5. Caution for Operation

- If you do not follow normal POWER ON, OFF sequence or abnormal operating, then AMOLED module can be damaged electro-optically and does not recover. Do not change software without

BOE confirmation.

- Response time may extremely delay at a temperature lower than operating range; AMOLED does not normally operate at a high temperature. But this may recover at a proper temperature.
- When you set optimal operating voltage to AMOLED module, you can see the optimal contrast of AMOLED. So, add voltage controllable function at SET Module.
- AMOLED module may not display normally when abnormal power or pressing power is added. Therefore you should secure AMOLED module maximum power at set not to have any pressure affect AMOLED module.
- Electro-chemical reaction may occur when there is humidity on pad; therefore, you should use AMOLED Module below maximum operating humidity.
- AMOLED Module Power Vdd should be designed to protect surge current at SET Module.
- You should not damage connector and cable for AMOLED module assembly by force folding or by applying extreme power.
- AMOLED may not display normally when it is interfered by surrounding elements, therefore you should consider setting design not to damage AMOLED module by surrounding elements.
- To satisfy EMI standards, you should plan your design after considering emitting energy.
- We cannot guarantee display characteristics outside viewing area, therefore your set window should be fixed into viewing area.
- Image-sticking may occur if AMOLED displays same image for a long time, so you need to make a change for AMOLED.
- When remove the window protective film, necessarily need to apply as a way to prevent Cushion and conductive tape Delamination.
  - As an upper Figure, thehandler takes off the direction of the arrow to remove the protective film.

11-6. Storage

- Place in a dark place where neither exposure to direct sunlight nor any fluorescent light is permitted and keep at room temperature & room humidity.
- Store with no contact with polarizer surface.
  [It is recommended to store them as they have been contained in the inner container when we delivered them.]

11-7. Safety Precautions

- Disassembly or modification may cause electric shock, damages to sensitive part inside of the AMOLED module, dust adhesion, or scratches on the display part.
- In the event that the contents of AMOLED module are on skin, wipe them with a paper towel or gauge and wash the part well, and receive medical attention if necessary.
- Do not use the AMOLED module for the special purpose besides display units.
- Be careful of the glass chips that may cause injury to fingers of skin, when the display part is broken.
- For keeping safe quality from outer exposure or contamination, modules should be consumed within 2 months after unpacking.

11-8. Precautions before us

You should discuss the following case with BOE.

- In case of any questions about contents of this Specification.
- In case of occurring new problems not mentioned at this Specification.
- In case of your request about income inspection specification change.
- In case of occurring new problem at your driving test.

◆ **If BOE has to change the conditions specified in thespecification, previously the negotiation shall be held and decided.**

12. Packing Specification

12-1. Box Pack

● MDL

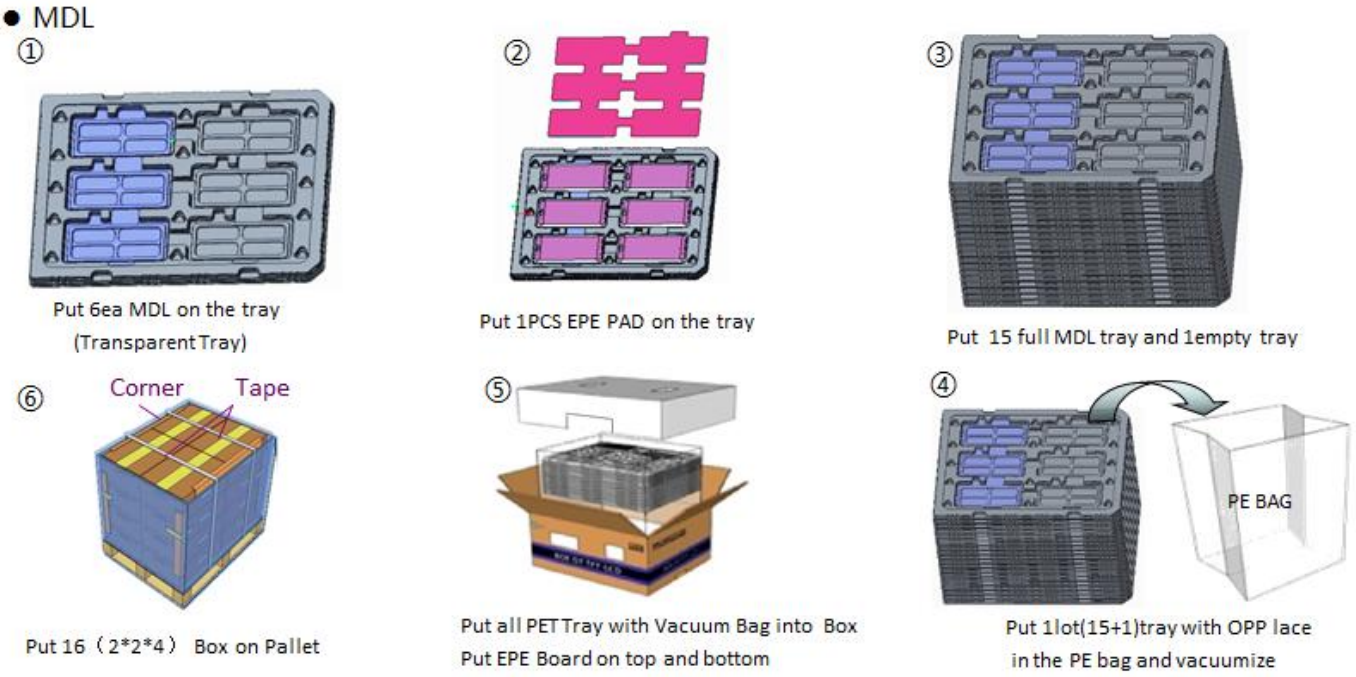

Figure21

● Packing Specification

Table18 packing specification

	Item	specifications	Notes
1	Tray	500*310*16（mm）	6pcs/tray
2	Tray Lot	15+1	
3	Height of Tray Lot	165（mm）	
4	Box	590*390*270（mm）	90pcs/box
5	Pallet	1200*800*150（mm）	