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SONY

Ver.1.2

1.7cm (0.68inch) Active Matrix Color OLED Microdisplay

ECX343EN

1 Overview / Applications

ECX343EN is a 1.7cm (0.68inch) diagonal 1920 (RGB) x 1200 active matrix color OLED Microdisplay panel module using based on a single crystal silicon transistor.

The module integrates a panel driver circuit, it is compact, lightweight, and high definition.

Potential applications: Head-mounted displays, View finders, Small monitors, AR/VR Glass, etc.

2 Features

Small size heigh definition：0.68inch, WUXGA display dots 1920 (RGB) x 1200 = 6.91 million dots
Maximum luminance：5,000cd/m^2 (panel unique maximum luminance)
Power consumption：500mW @ 2000cd/m^2
Contrast ：more than 100,000:1 @ 500 to 5000cd/m^2
Color gamut ：sRGB 108 % (area ratio)
Display bit depth：R 8bit G 8bit B 8bit
Response speed：0.01ms or less
Frame rate ：60 to 120Hz
Compact and light：Panel outline 13×20.5×1.5 (mm)、Mass 0.9(g)
Orbit ：Total number of dots : 1952 (RGB)×1232 = 7.21 million dots
Input interface ：RGB 24bit/YCbCr 24bit, 16bit LVDS input interface
Built-in sequence：One frame start-up sequence is available

3 Functions

・Dual line progressive drive

Simultaneous 2 vertical lines scan with the same data can compatible higher frame rate and reasonable power consumption.

・Up/down and right/left Inversion

Up/down and right/left inverse display of the panel can be set by the registers.

・Luminance setting

Peak luminance setting can be changed. (Peak luminance: Luminance at maximum gray level)

・Direct duty setting

The ratio of the light-emitting period in one vertical scan period can be set.

・Luminance changing speed

When you use the luminance setting, it is possible to change the speed to reach the set luminance.

・OLED illumination mode selection

Support for both rolling and global illumination mode, selectable.

・Orbit function

Scanning area shift for relaxing burn-in phenomena.

・Power saving function

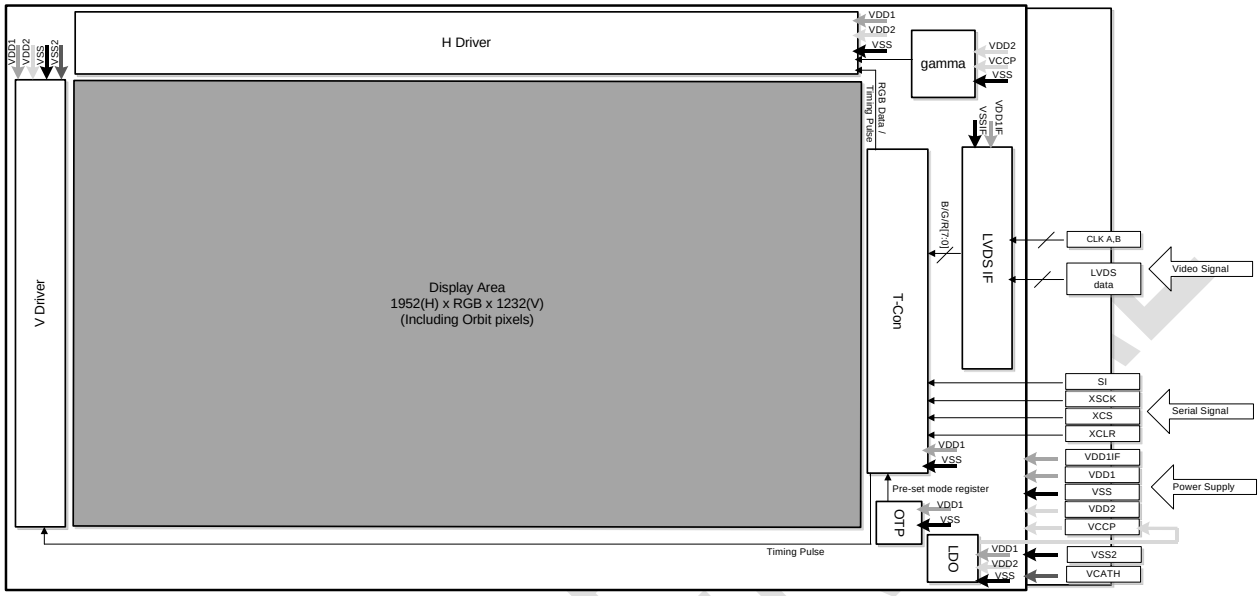
To be able to halt some circuits for power save purpose.

・SPI access

Support serial communication of normal / burst transfer.

4 Contents

5 System Block Diagram



6 Absolute Maximum Ratings

Item	Symbol	Min.	Maximum Ratings	Unit
1.8V power supply	VDD1	-0.3	2.0	V
1.8V power supply	VDD1IF	-0.3	2.0	V
3.3V power supply	VDD2	-0.3	4.0	V
-6.6V power supply	VSS2	-8.5	0.3	V
	VDD2 - VSS2	0	12.5	V
-6.6V power supply	VCATH	-8.5	0.3	V
Logic input voltage *	Vi	-0.3	VDD1+0.3	V
IF input voltage **	ViIF	-0.3	VDD1IF+0.3	V
Storage temperature	Tpnl	-30	80	°C

*Pin # 12-14,17

**Pin # 20-31,35-46

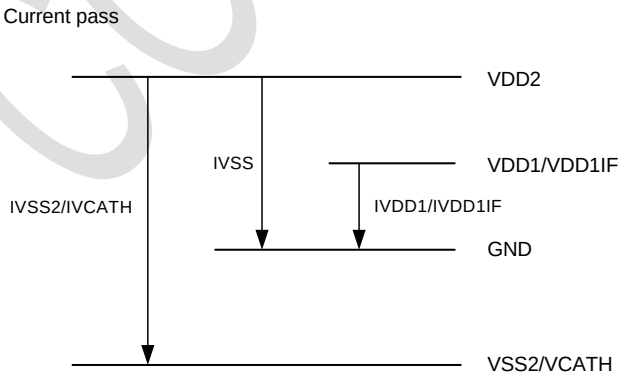
7 Electrical characteristics

7.1 Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
1.8V power supply	VDD1	1.62	1.8	1.98	V
1.8V power supply	VDD1IF	1.62	1.8	1.98	V
3.3V power supply	VDD2	3.0	3.3	3.6	V
-6.6V power supply	VSS2	-6.9	-6.6	-6.3	V
-6.6V power supply	VCATH	-6.9	-6.6	-6.3	V
Panel temperature range	Tpnl	-20	40	70	˚C

7.2 Current Consumption

Item	Symbol	Condition		Stand-by	60Hz Drive WUXGA	120Hz Drive WUXGA		Unit
		Drive	Luminance cd/m^2	Typical value	Typical value	Typical value	Maximum value.	
(Drive)		VDD1=1.8V VDD1IF=1.8V VDD2=3.3V VSS=GND VSS2=-6.6V VCATH=-6.6V all white clock frequency =75MHz Tpnl = 40℃ LVDS						
VDD1	IVDD1			0.1	13	23	25	mA
VDD1IF	IVDD1IF			0	35	41	46	mA
VDD2 – VSS	IVSS			0	14	17	26	mA
VDD2 – VSS2	IVSS2			0	0.2	0.2	0.3	mA
（EL）								
VDD2－VCATH	IVCATH		0	0	0	0	0	mA
			3500		60	60	70	mA
			5000		86	86	100	mA



7.3 SPI、LVDS

7.3.1 SPI

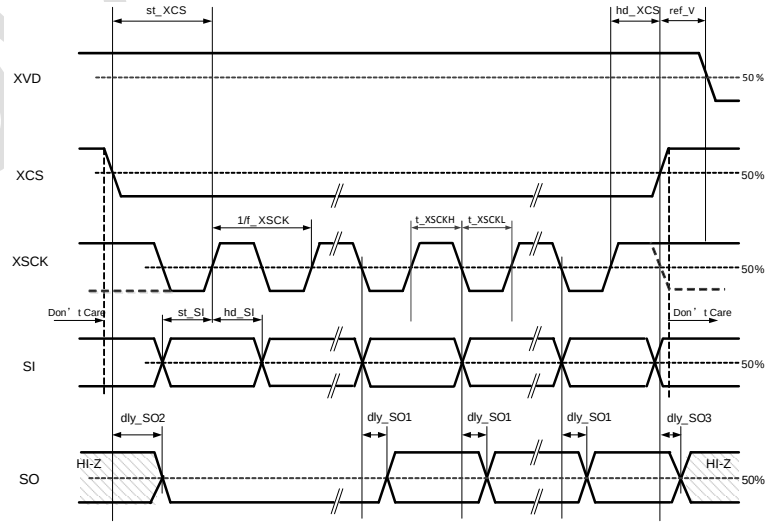
DC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level input voltage	VIH		0.7xVDD1		VDD1	V
Low-level input voltage	VIL		0		0.3xVDD1	V
High-level input voltage	Vt+	Schmitt input	0.7xVDD1		VDD1	V
Low-level input voltage	Vt-	Schmitt input	0		0.3xVDD1	V
Vt+ - Vt-	Vhys	Schmitt input		0.5		V
Logic High-level output voltage	VOH	IO = -1.0mA	VDD1 - 0.4			V
Logic Low-level output voltage	VOL	IO = +1.0mA			0.4	V

AC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
XSCK frequency	f_XSCK				10	MHz
XSCK High time	t_XSCKH		10			ns
XSCK Low time	t_XSCKL		10			ns
XCS setup time	st_XCS		25			ns
XCS hold time	hd_XCS		25			ns
SI setup time	st_SI		25			ns
SI hold time	hd_SI		25			ns
SO output delay 1	dly_SO1				30	ns
SO output delay 2	dly_SO2				25	ns
SO output delay 3	dly_SO3				21	ns
V sync reflected time	Ref_V		10			*clock

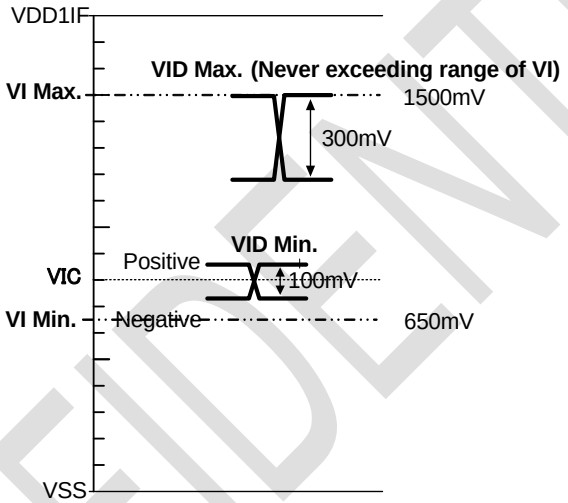
*clock = Input clock



7.3.2 LVDS

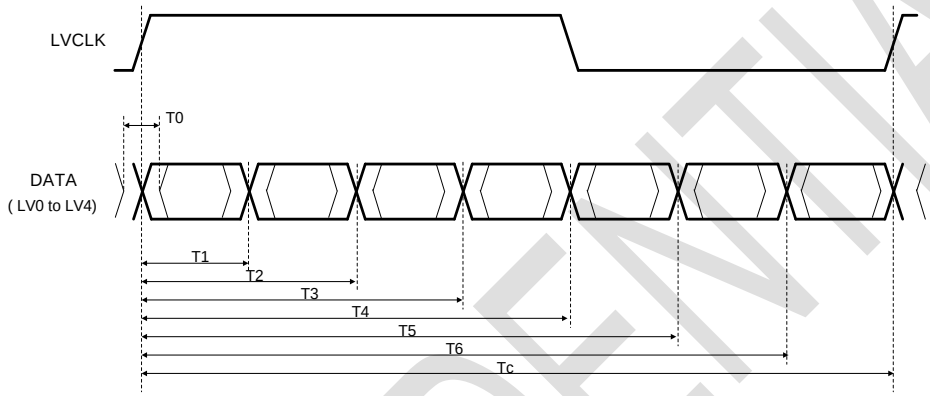
DC Characteristics

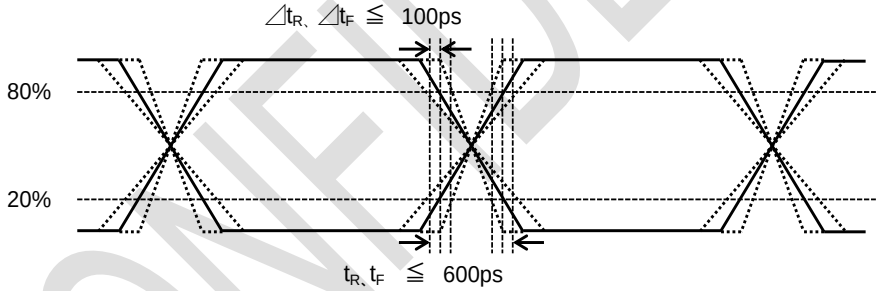
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	VDD1IF		1.62	1.8	1.98	V
Differential voltage range	VID	RL=100Ω	100		300	mV
Differential voltage deviation (Between lanes)	⊿VID	RL=100Ω	-10		10	%
Input voltage range	VI	RL=100Ω	650		1500	mV
Common voltage deviation (Between lanes)	⊿VIC	RL=100Ω	-100		100	mV

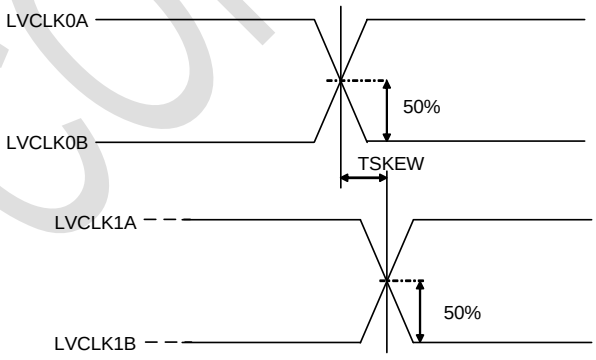


AC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock Pulse Period	Tc	54MH to 75MHz	13.333		18.519	ns
Clock Data Rise/Fall Time	tR, tF	20% to 80% At Panel Input			600	ps
Clock Data Rise/Fall Time Deviation (Between Lanes)	⊿tR,⊿tF				100	ps
Clock Skew	TSKEW				1000	ps
Delay of serial bit data (n:0 to 6)	Tn		(n/7)Tc-0.265		(n/7)Tc+0.265	ns



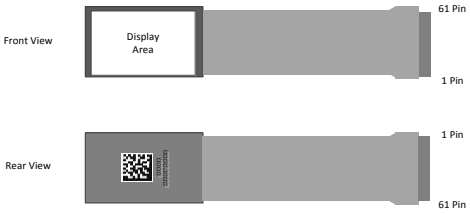




8 Circuit Example

8.1 Pin description

8.1.1 Pin Assignment



Pin No. (FPC Side)	Symbol	I/O Type	Voltage System	Description	Equivalent circuit 7.1.2
1	VCCP_I	Power Input	3.3V	Reference Voltage	No.10
2	VCCP_O	Power output	3.3V	Reference Voltage	No.12
3	VCCP_I	Power Input	3.3V	Reference Voltage	No.10
4	VDD2	Power Input	3.3V	VDD2 Power Supply	No.10
5	VSS	GND	3.3V	Ground	No.11
6	VCATH	Power Input	-6.6V	EL Cathode Power Supply	No.9
7	VSS	GND	3.3V	Ground	No.11
8	VSS2	Power Input	-6.6V	VSS2 Power Supply	No.8
9	TEST	Input	1.8V	Test Pin (Connect to Ground)	No.7
10	VDD1	Power Input	1.8V	VDD1 Power Supply	
11	TEST	Input	1.8V	Test Pin (Connect to Ground)	No.4
12	XCS	Input	1.8V	SPI Access Chip Select	No.1
13	XSCK	Input	1.8V	SPI Access Clock	No.1
14	SI	Input	1.8V	SPI Access Data Input	No.1
15	SO	Output	1.8V	SPI Access Data Output	No.2
16	TEST	Output	1.8V	Test Pin (Open)	No.3
17	XCLR	Input	1.8V	System Reset Signal	No.1
18	VSSIF	GND	1.8V	Interface Ground *1	
19	VDD1IF	Power Input	1.8V	Interface VDD1Power Supply	
20	LVCLK0A	Input	1.8V	LVDS clock (Positive *2)	No.5
21	LVCLK0B	Input	1.8V	LVDS clock (Negative *2)	No.5
22	LV0A	Input	1.8V	Data signal (Positive *2)	No.5
23	LV0B	Input	1.8V	Data signal (Negative *2)	No.5
24	LV1A	Input	1.8V	Data signal (Positive *2)	No.5
25	LV1B	Input	1.8V	Data signal (Negative *2)	No.5
26	LV2A	Input	1.8V	Data signal (Positive *2)	No.5
27	LV2B	Input	1.8V	Data signal (Negative *2)	No.5
28	LV3A	Input	1.8V	Data signal (Positive *2)	No.5

Pin No. (FPC Side)	Symbol	I/O Type	Voltage System	Description	Equivalent circuit 7.1.2
29	LV3B	Input	1.8V	Data signal (Negative *2)	No.5
30	LV4A	Input	1.8V	Data signal (Positive *2)	No.5
31	LV4B	Input	1.8V	Data signal (Negative *2)	No.5
32	VDD1IF	Power Input	1.8V	Interface VDD1 Power Supply	No.5
33	VSSIF	GND	1.8V	Interface Ground *1	No.5
34	VDD1IF	Power Input	1.8V	Interface VDD1Power Supply	No.5
35	LV5A	Input	1.8V	Data signal (Positive *2)	No.5
36	LV5B	Input	1.8V	Data signal (Negative *2)	No.5
37	LV6A	Input	1.8V	Data signal (Positive *2)	No.5
38	LV6B	Input	1.8V	Data signal (Negative *2)	No.5
39	LV7A	Input	1.8V	Data signal (Positive *2)	No.5
40	LV7B	Input	1.8V	Data signal (Negative *2)	No.5
41	LV8A	Input	1.8V	Data signal (Positive *2)	No.5
42	LV8B	Input	1.8V	Data signal (Negative *2)	No.5
43	LV9A	Input	1.8V	Data signal (Positive *2)	No.5
44	LV9B	Input	1.8V	Data signal (Negative *2)	No.5
45	LVCLK1A	Input	1.8V	LVDS clock (Positive *2)	No.5
46	LVCLK1B	Input	1.8V	LVDS clock (Negative *2)	No.5
47	VDD1IF	Power Input	1.8V	Interface VDD1 Power Supply	
48	VSSIF	GND	1.8V	Interface Ground*1	
49	VSS2	Power Input	-6.6V	VSS2 Power Supply	No.8
50	VCCP_I	Power Input	3.3V	Reference Voltage	No.10
51	VCATH	Power Input	-6.6V	EL Cathode Power Supply	No.9
52	VSS	GND	3.3V	Ground	No.11
53	VDD2	Power Input	3.3V	VDD2 Power Supply	No.10
54	VCCP_I	Power Input	3.3V	Panel Power Supply	No.6
55	VREF1	Power output	3.3V	Reference Voltage	No.6
56	VREF2	Power output	3.3V	Reference Voltage	No.6
57	VREF3	Power output	3.3V	Reference Voltage	No.6
58	VREF4	Power output	3.3V	Reference Voltage	No.6
59	TEST	Output	3.3V	Test Pin (Open)	No.12
60	VSS	GND	1.8V	Ground	
61	VDD1	Power Input	1.8V	VDD1 Power Supply	

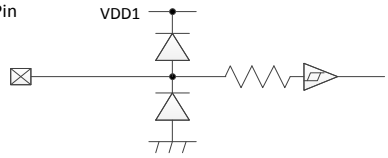
*1：Independent grounding for VSSIF from other grounding is recommened as much as possible.

*2：Please refer “13.1 Swapping function” with regarding to Positive/Negative（Pin No. 20 to 31 , 35 to 46）

8.1.2 Equivalent Circuits

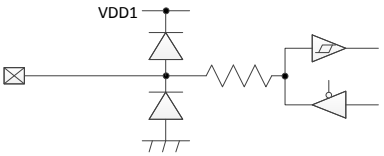
No.1 Schmitt Pin

12.XCS
13.XSCK
14.SI
17.XCLR



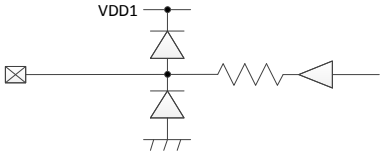
No.2 Schmitt Pin

15.SO



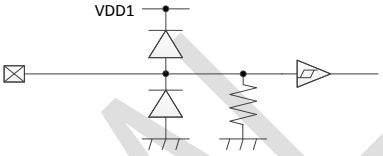
No.3

16.TEST



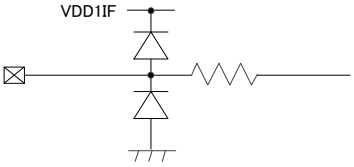
No.4 Schmitt Pin

11.TEST



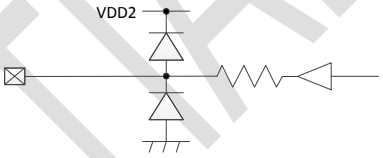
No.5

20.LVCLK0A
21.LVCLK0B
22.LV0A
23.LV0B
24.LV1A
25.LV1B
26.LV2A
27.LV2B
28.LV3A
29.LV3B
30.LV4A
31.LV4B
35.LV5A
36.LV5B
37.LV6A
38.LV6B
39.LV7A
40.LV7B
41.LV8A
42.LV8B
43.LV9A
44.LV9B
45.LVCLK1A
46.LVCLK1B



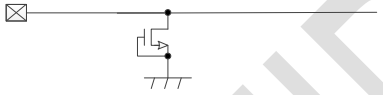
No.6

54.VCCP_I
55.VREF1
56.VREF2
57.VREF3
58.VREF4



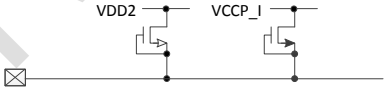
No.7

9.TEST



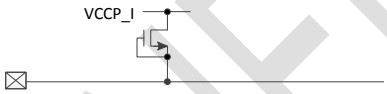
No.8

8.VSS2
49.VSS2



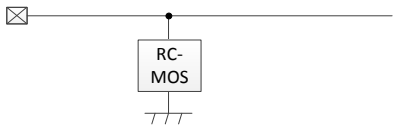
No.9

6.VCATH
51.VCATH



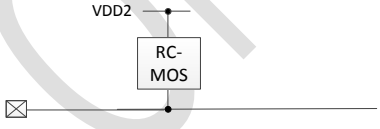
No.10

1.VCCP_I
3.VCCP_I
4.VDD2
50.VCCP_I
53.VDD2



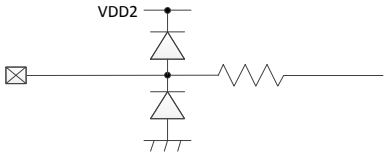
No.11

5.VSS
7.VSS
52.VSS



No.12

2.VCCP_O
59.TEST



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8.2 Peripheral Circuit Example

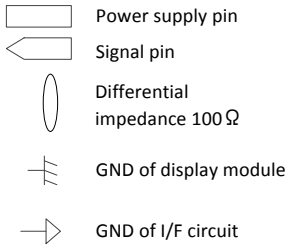
1)Capacitance specification
X5R or B

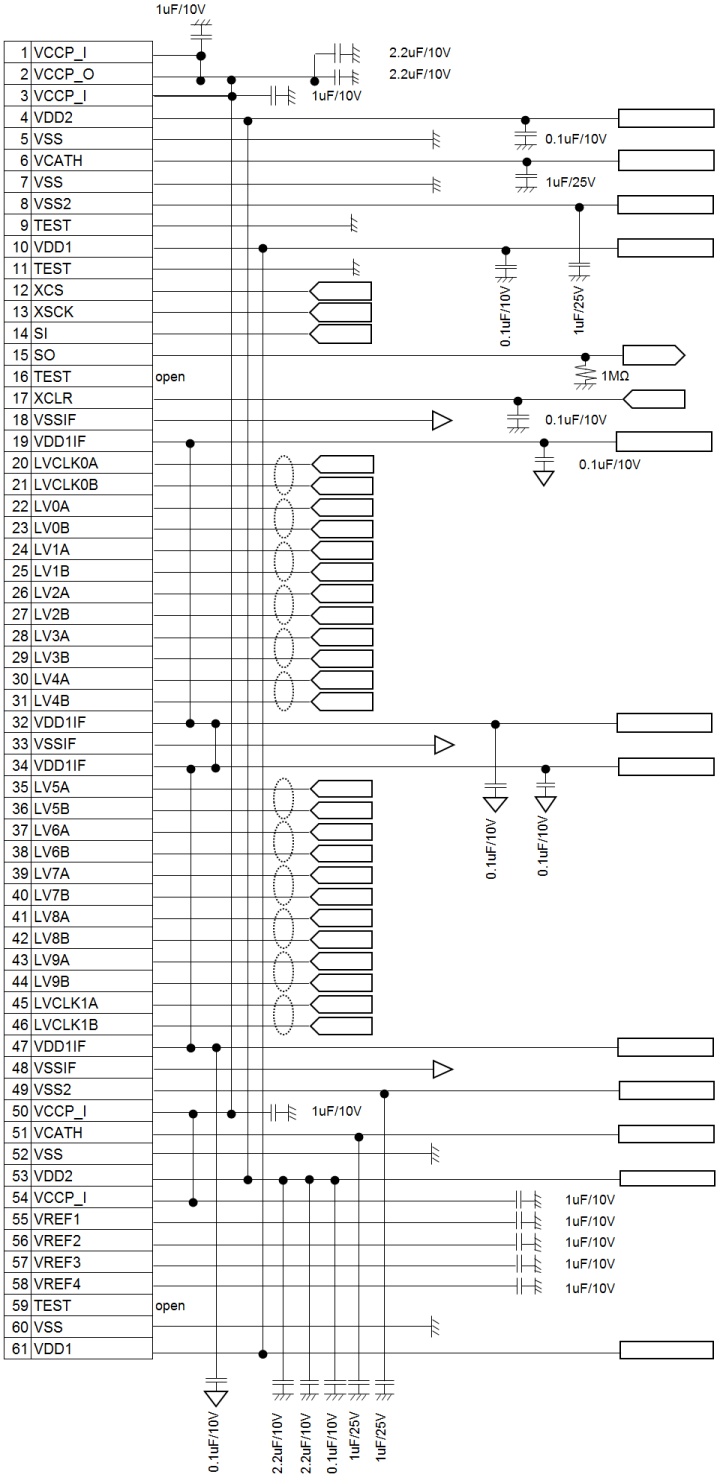
2)Capacitance for power supply
Please connect the capacitance directly to each power Supply . If effective capacitance is not enough it can affect display picture quality.

3)Connection between 1pin,2pin,3pin and 50pin
Please design connection between them as short as possible.

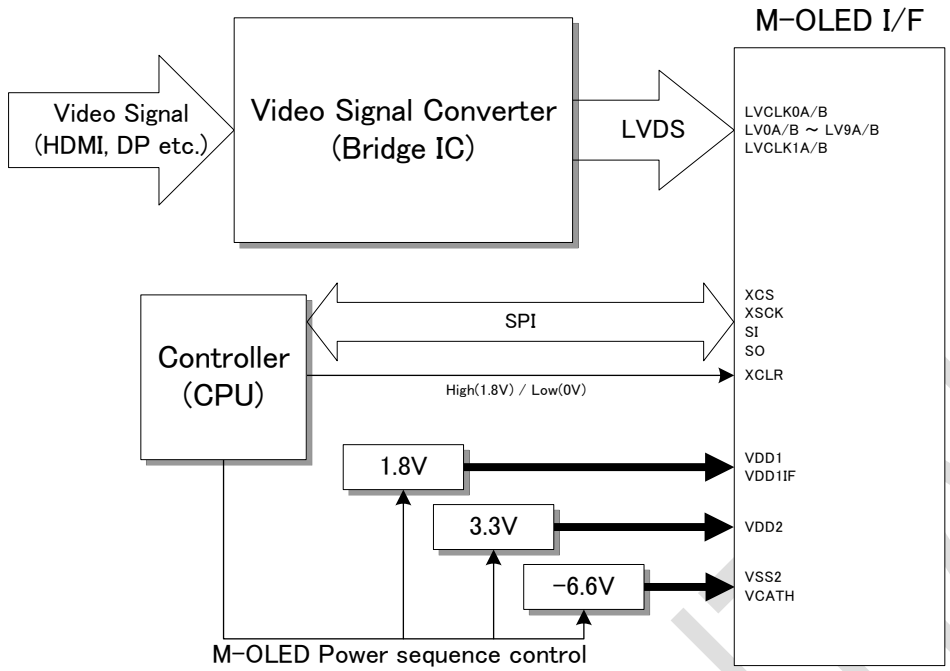
4)Please connect un-used pin based on selected interface specification to ground pin of input interface circuit.

5)VSSIF
Please allocate independent GND pattern for VSSIF.





8.3 Design Reference



9 Register Map

The registers that need to be set to display are as follows. (Some of them are the same as the default settings.)

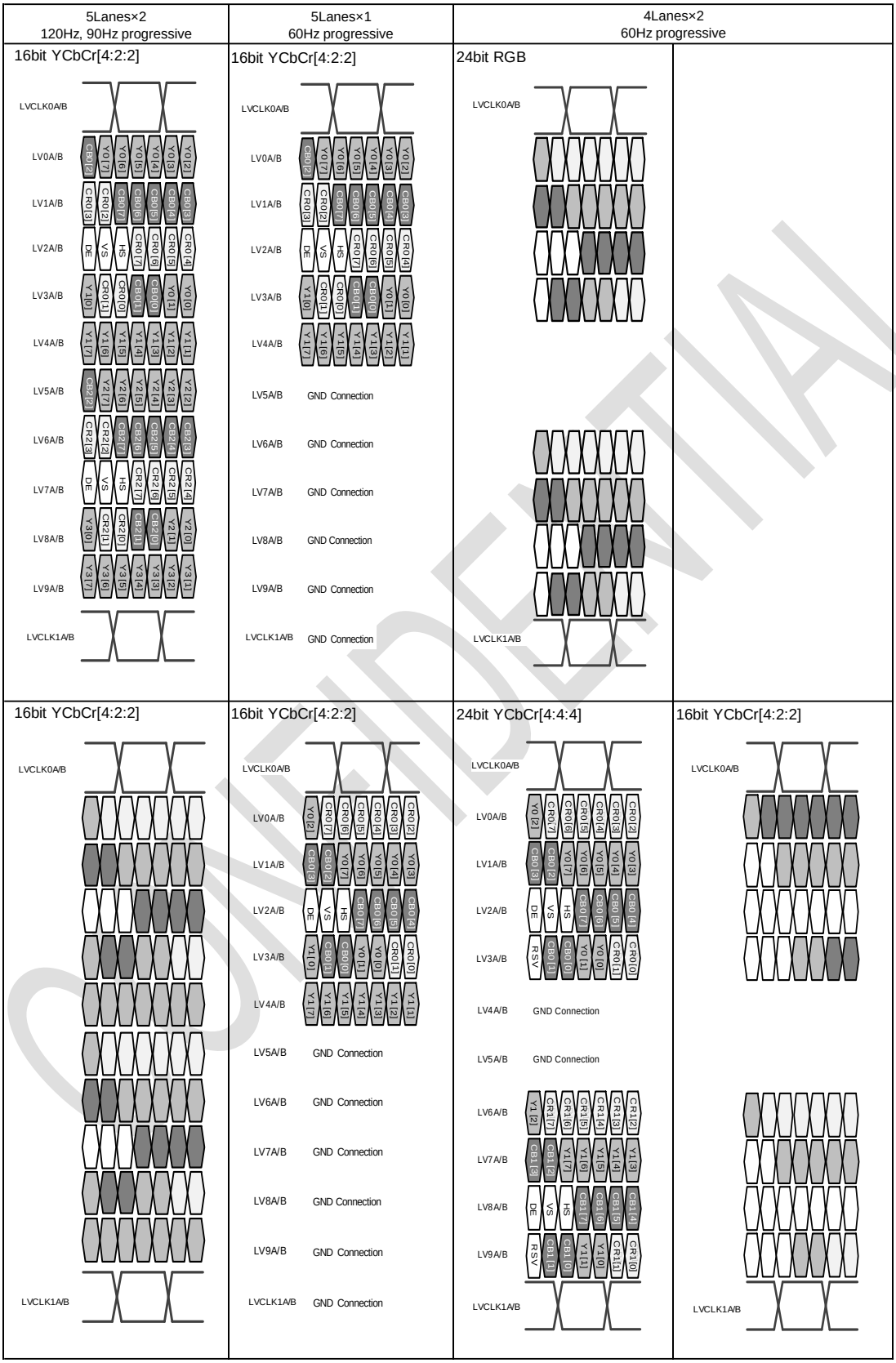
Please change according to your settings

Do not change from the default values

										Progressive				Dual-line progressive				Dual-line progressive with 1line offset			
Addr.	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	Initial	120Hz 5Lx2	60Hz 5Lx1	60Hz 4Lx2	90Hz 5Lx2	240Hz 5Lx2	120Hz 5Lx1	120Hz 4Lx2	180Hz 5Lx2	240Hz 5Lx2	120Hz 5Lx1	120Hz 4Lx2	180Hz 5Lx2
0x00						PS2	PS1	PS0	00	00	00	00	00	00	00	00	00	00	00	00	00
0x01									00	00	00	00	00	00	00	00	00	00	00	00	00
0x02				DE_SEL	DWN	RGT	DE_DLY[1:0]		8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C
0x03	RGB_YCB	YCB_DEC	YCB_CMPLE	YCB_OFSET		LVDS_MAP	YCB_P	FORMAT_SEL_DATA	D9	D9	D9	58	D9	D9	D9	58	D9	D9	D9	58	D9
0x04	PN_POL[1:0]		PINSWP[1:0]		PRTSWP	IFSW[2:0]			05	05	04	03	05	05	04	03	05	05	04	03	05
0x05			ORBIT_H[5:0]						00	00	00	00	00	00	00	00	00	00	00	00	00
0x06			ORBIT_V[5:0]						00	00	00	00	00	00	00	00	00	00	00	00	00
0x07								LUMINANCE	10	20	20	20	20	20	20	20	20	20	20	20	20
0x08									00	00	00	00	00	00	00	00	00	00	00	00	00
0x09									00	00	00	00	00	00	00	00	00	00	00	00	00
0x0A									00	00	00	00	00	00	00	00	00	00	00	00	00
0x0B									00	00	00	00	00	00	00	00	00	00	00	00	00
0x0C									00	00	00	00	00	00	00	00	00	00	00	00	00
0x0D									10	10	10	10	10	10	10	10	10	10	10	10	10
0x0E									44	44	44	44	44	44	44	44	44	44	44	44	44
0x0F		C_SLOPE [2:0]							00	00	00	00	00	00	00	00	00	00	00	00	00
0x10					WB_CALEN	L_SEAMLESSEN	L_AT_CALEN		00	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
0x11									04	04	04	04	04	04	04	04	04	04	04	04	04
0x12							REQUEST_LV[9:8]		00	01	01	01	01	01	01	01	01	01	01	01	01
0x13	REQUEST_LV[7:0]								0F	5E	5E	5E	5E	5E	5E	5E	5E	5E	5E	5E	5E
0x3E	VDRMODE	OESW							20	21	21	21	21	A1	A1	A1	A1	E1	E1	E1	E1
0x43									40	40	40	40	40	20	20	20	20	20	20	20	20
0x44									29	29	29	29	29	11	11	11	11	11	11	11	11
0x45									D9	D9	D9	D9	D9	69	69	69	69	6A	6A	6A	6A
0x46									02	02	02	02	02	01	01	01	01	01	01	01	01
0x47									71	71	71	71	71	39	39	39	39	39	39	39	39
0x49									18	18	18	18	18	08	08	08	08	08	08	08	08
0x4B									22	22	22	22	22	11	11	11	11	11	11	11	11
0x4C									72	72	72	72	72	3A	3A	3A	3A	3A	3A	3A	3A
0x4D									71	71	71	71	71	39	39	39	39	39	39	39	39
0x4E									04	04	04	04	04	02	02	02	02	02	02	02	02
0x4F									7D	7D	7D	7D	7D	3B	3B	3B	3B	3B	3B	3B	3B
0x50									18	18	18	18	18	08	08	08	08	08	08	08	08
0x51									22	22	22	22	22	11	11	11	11	11	11	11	11
0x52									73	73	73	73	73	3B	3B	3B	3B	3B	3B	3B	3B
0x53									72	72	72	72	72	3A	3A	3A	3A	3A	3A	3A	3A
0x54									04	04	04	04	04	02	02	02	02	02	02	02	02
0x55									7D	7D	7D	7D	7D	3B	3B	3B	3B	3B	3B	3B	3B
0x56									18	18	18	18	18	08	08	08	08	08	08	08	08
0x5A									19	19	10	10	19	19	10	10	19	19	10	10	19

Addr.	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	Initial	Progressive				Dual-line progressive				Dual-line progressive with 1line offset			
										120Hz 5Lx2	60Hz 5Lx1	60Hz 4Lx2	90Hz 5Lx2	240Hz 5Lx2	120Hz 5Lx1	120Hz 4Lx2	180Hz 5Lx2	240Hz 5Lx2	120Hz 5Lx1	120Hz 4Lx2	180Hz 5Lx2
0x61									1F	1F	11	11	17	1F	11	11	17	1F	11	11	17
0x62									06	06	03	03	05	06	03	03	05	06	03	03	05
0x63									01	01	00	00	01	01	00	00	01	01	00	00	01
0x64									D7	D7	ED	ED	61	D7	ED	ED	61	D7	ED	ED	61
0x65									0B	0B	06	06	08	0B	06	06	08	0B	06	06	08
0x66									10	10	00	00	10	10	00	00	10	10	00	00	10
0x67									2A	2A	17	17	20	2A	17	17	20	2A	17	17	20
0x68									EF	EF	F9	F9	73	EF	F9	F9	73	EF	F9	F9	73
0x69									10	10	00	00	10	10	00	00	10	10	00	00	10
0x6A									0E	0E	09	09	0B	0E	09	09	0B	0E	09	09	0B
0x6B									CB	CB	E7	E7	58	CB	E7	E7	58	CB	E7	E7	58
0x6C									11	11	00	00	11	11	00	00	11	11	00	00	11
0x6D									DA	DA	EE	EE	64	DA	EE	EE	64	DA	EE	EE	64
0x6E									E7	E7	F5	F5	6D	E7	F5	F5	6D	E7	F5	F5	6D
0x6F									10	10	10	10	10	10	10	10	10	10	10	10	10
0x70									32	32	19	19	26	32	19	19	26	32	19	19	26
0x71									22	22	11	11	1A	22	11	11	1A	22	11	11	1A
0x72									0B	0B	06	06	08	0B	06	06	08	0B	06	06	08
0x73									2C	2C	16	16	21	2C	16	16	21	2C	16	16	21
0x75									1C	1C	0E	0E	15	1C	0E	0E	15	1C	0E	0E	15
0x76									04	00	00	00	00	00	00	00	00	00	00	00	00
0x77								FRAME_MD	05	00	00	00	00	00	00	00	00	00	00	00	00
0x78									06	00	00	00	00	00	00	00	00	00	00	00	00
0x79									07	00	00	00	00	00	00	00	00	00	00	00	00
0x7A									08	00	00	00	00	00	00	00	00	00	00	00	00
0x7B									09	00	00	00	00	00	00	00	00	00	00	00	00
0x7C									10	00	00	00	00	00	00	00	00	00	00	00	00
0x7D									11	00	00	00	00	00	00	00	00	00	00	00	00
0x80								RD_ON	00	00	00	00	00	00	00	00	00	00	00	00	00
0x81	RD_ADDR[7:0]								00	00	00	00	00	00	00	00	00	00	00	00	00
0x82									00	00	00	00	00	00	00	00	00	00	00	00	00
0x83									00	03	03	03	03	03	03	03	03	03	03	03	03
0x84									64	84	84	84	84	84	84	84	84	84	84	84	84
0x85									12	14	14	14	14	14	14	14	14	14	14	14	14
0x89									04	04	04	04	04	02	02	02	02	02	02	02	02
0x8A									E2	E2	E2	E2	E2	71	71	71	71	71	71	71	71
0x8B	DT_AT_CALEN	DUTYCYCLE[6:0]							E3	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA
0x8E									10	00	00	00	00	00	00	00	00	00	00	00	00
0xBF									00	08	08	08	08	08	08	08	08	08	08	08	08
0xF2									01	01	01	01	01	00	00	00	00	00	00	00	00
0xF3									38	38	38	38	38	9C	9C	9C	9C	9C	9C	9C	9C
0xF4									40	40	40	40	40	20	20	20	20	20	20	20	20
0xF5									7E	E1	E1	E1	E1	70	70	70	70	70	70	70	70
0xF6									42	42	42	42	42	21	21	21	21	21	21	21	21
0xF7									71	71	71	71	71	38	38	38	38	38	38	38	38
0xF8									7E	E1	E1	E1	E1	70	70	70	70	70	70	70	70
0xF9									42	42	42	42	42	21	21	21	21	21	21	21	21
0xFA									71	71	71	71	71	38	38	38	38	38	38	38	38
0xFB									7E	E1	E1	E1	E1	70	70	70	70	70	70	70	70
0xFC									70	70	70	70	70	70	70	70	70	70	70	70	70
0xFD									18	00	00	00	00	00	00	00	00	00	00	00	00
0xFE									FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

10 Video Signal Transfer Format



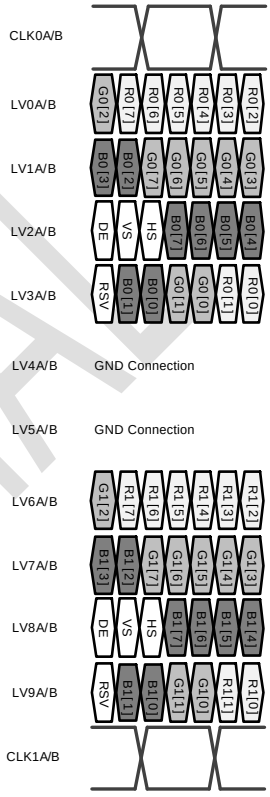
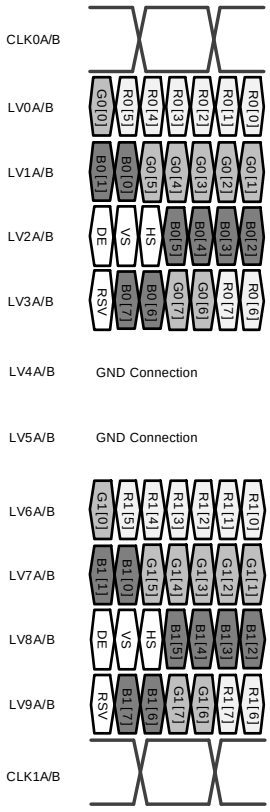
Setting the registers appropriately for the video signal transfer format based on table in below.

◆Register Settings

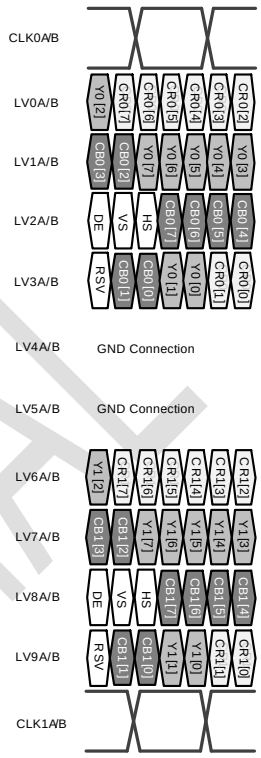
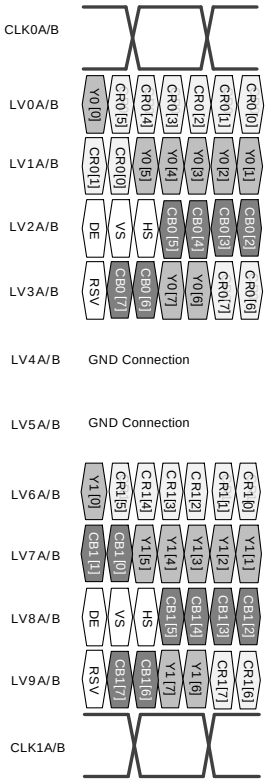
Address	DATA	Register	Function / Setting
0x03	[0]	FORMAT_SEL_DATA	YCbCr format selection 0: 4:4:4 (24bit) 1: 4:2:2 (16bit)
	[1]	YCB_P	Selection of YCbCr (YPbPr) input pattern 0: Cb and Pb first (Default) 1: Cr and Pr first
	[2]	LVDS_MAP	Selection of LVDS data mapping 0: Based on JEITA (Default) 1: Based on VESA
	[4]	YCB_OFSET	YCbCr Input offset selection 0: Complement on 2 (-128 to 127) (Default) 1: Positive value(0 to 255)
	[5]	YCB_CMPLE	4:2:2 CbCr input interpolation selection 0: Linear interpolation 1: Preliminary interpolation (Default)
	[6]	YCB_DEC	Selection of YCbCr / YPbPr conversion 0: YCbCr (BT. 601) 1: YPbPr (BT. 709) (Default)
	[7]	RGB_YCB	Selection of RGB / YCbCr (YPbPr) format 0: RGB 1: YCbCr and YPbPr
0x04	[2:0]	IFSW	Selection of Interface input mode 000: Reserved（Don't use this mode） 001: Reserved（Don't use this mode） 010: Reserved（Don't use this mode） 011: 4lanes×2 100: 5lanes×1 101: 5lanes×2 110: Reserved（Don't use this mode） 111: Reserved（Don't use this mode）

SONY

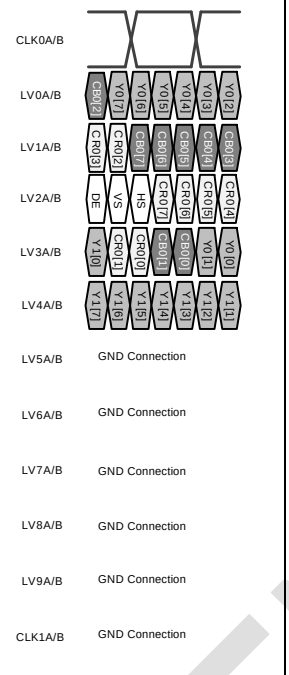
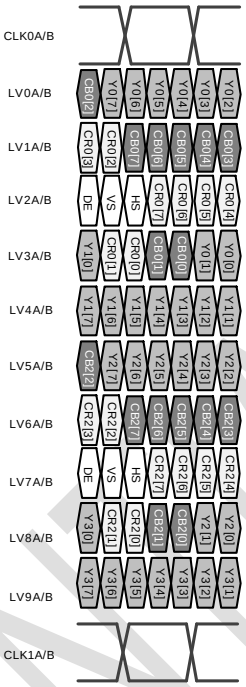
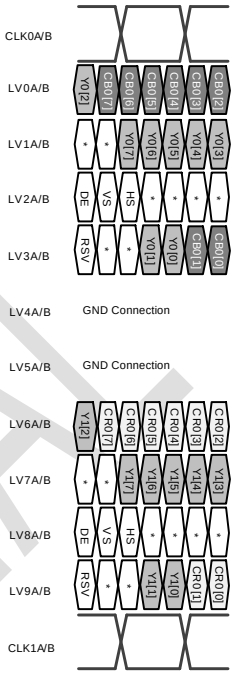
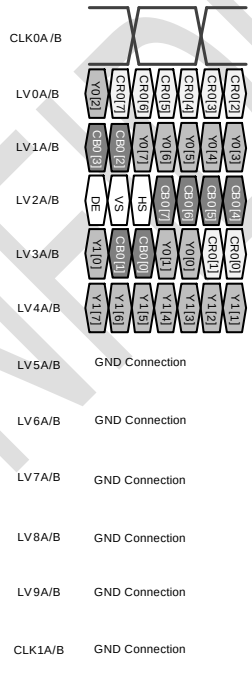
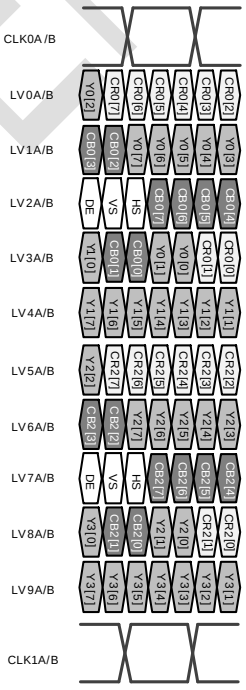
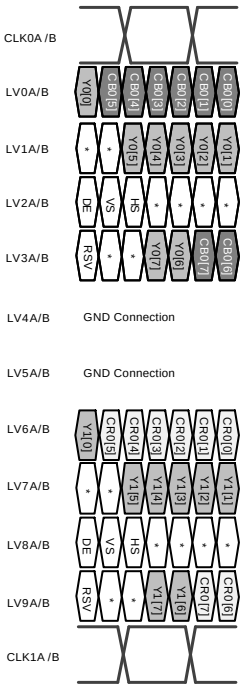
◆Register setting and transfer data format in case for YCB_DEC=0. (In case of YCB_DEC=1, Cb should be Pb and Cr shoud be Pr.)

RGB _YCB	YCB _P	FORMAT _SEL_ DATA	LVDS _MAP	5Lanes×1 (IFSW=100)	5Lanes×2 (IFSW=101)	4Lanes×2 (IFSW=011)
0	—	—	0			
			1			

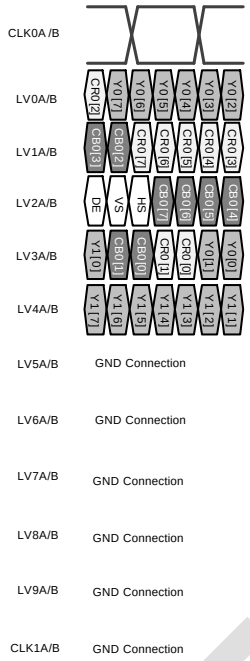
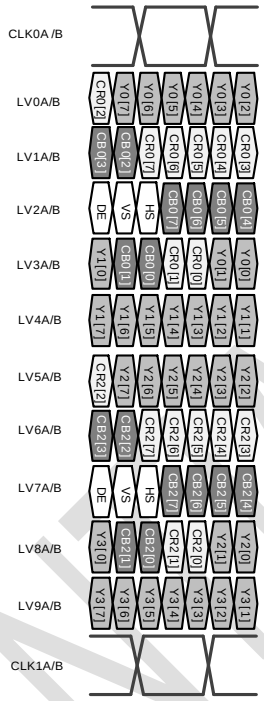
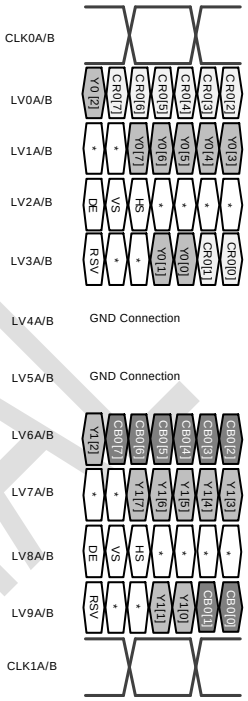
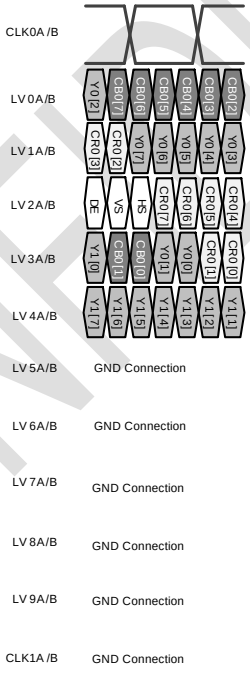
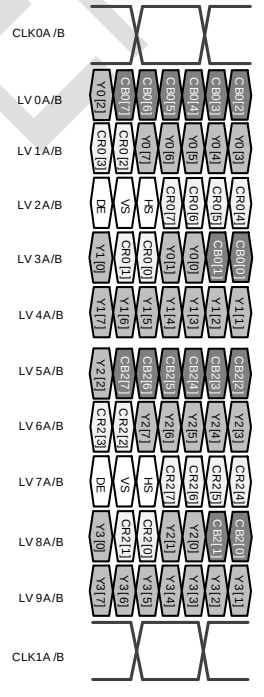
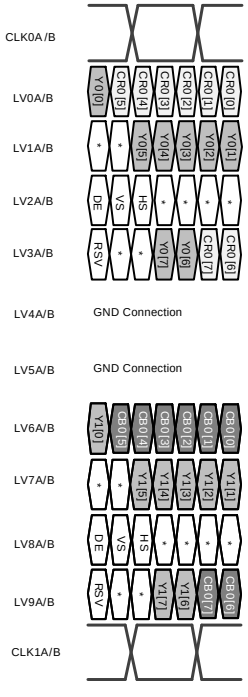
SONY

RGB _YCB	YCB _P	FORMAT _SEL_ DATA	LVDS _MAP	5Lanes×1 (IFSW=100)	5Lanes×2 (IFSW=101)	4Lanes×2 (IFSW=011)
1	—	0	0			
			1			

SONY

RGB _YCB	YCB _P	FORMAT _SEL_ DATA	LVDS _MAP	5Lanes×1 (IFSW=100)	5Lanes×2 (IFSW=101)	4Lanes×2 (IFSW=011)
1	0	1	0			
			1			

SONY

RGB _YCB	YCB _P	FORMAT _SEL_ DATA	LVDS _MAP	5Lanes×1 (IFSW=100)	5Lanes×2 (IFSW=101)	4Lanes×2 (IFSW=011)
1	1	1	0			
			1			

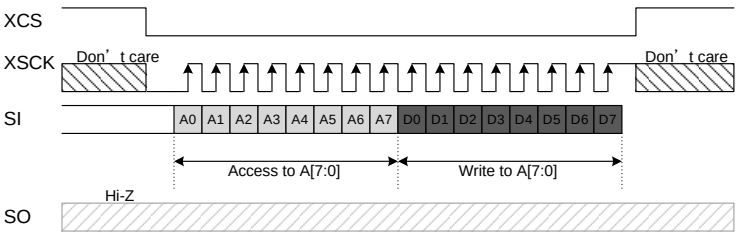
11 SPI Access

11.1 Serial I/F Write Access

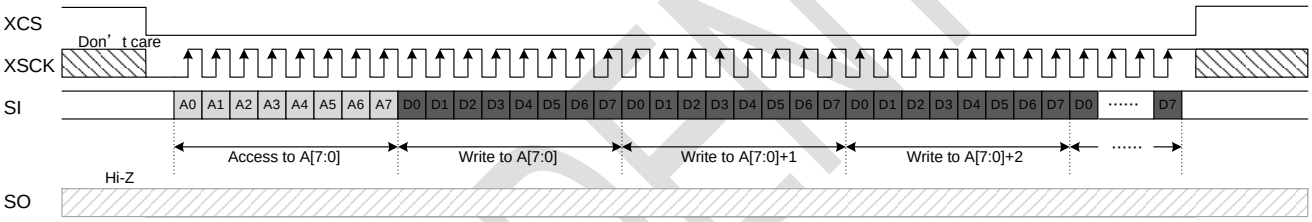
Serial communication of normal / burst transfer, LSB first is supported for write operation.

Input an address of the target register from SI (pin #14), then input data to the address.

The timing of write access is shown in below.



Write Access Normal Transfer (LSB First)



Write Access Burst Transfer (LSB First)

・Data capturing starts at XCS fall position.

・During XCS is low status, Data should be captured at 16th XCS rise position.

・The first 8bit data are recognized as the address, and next coming 8bit are recognized as the write value.

・During XCS is low status, Data can't be captured and are invalid If the number of XCS pulse is less than 15 times.

・During XCS is low status, if changing to burst transfer mode and data capturing for address A should complete along with 16th XSCK rising timing. After 16th XSCK pulse, , from 17th to 24th data should be captured for address A+1, from 25th to 32nd data for address A+2. After that, such increment of the address is automatically applied.

・Only 8xN (N is an integer greater than or equal to 2) data should be captured If the number of XCS pulse is not equal to the multiple of 8.

11.2 Serial I/F Read Access

In Read mode, serial communication support both normal and burst transfer mode, based on LSB first mode.

◆Register Settings

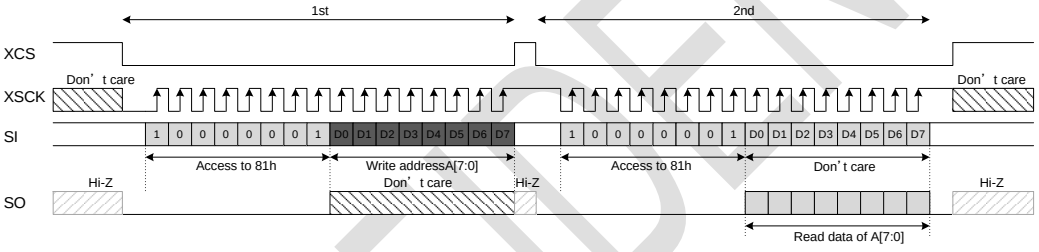
Address	DATA	Register name	Function / Setting
0x80	[0]	RD_ON	Register read on / off 0: Off (Default) 1: On
0x81	[7:0]	RD_ADDR	Register read address setting

Setting "RD_ON" to 1, and then execute 2 times serial communication.

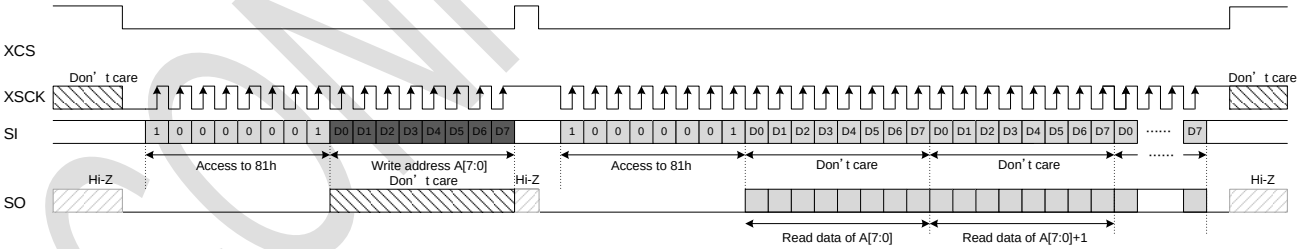
1st serial communication: Write the address of the target register to "RD_ADDR".

2nd serial communication: Read the data of the target register from SO (pin #15) after accessing to the "RD_ADDR".

The timing of read access is shown in below.



Read Access Normal Transfer（LSB First）

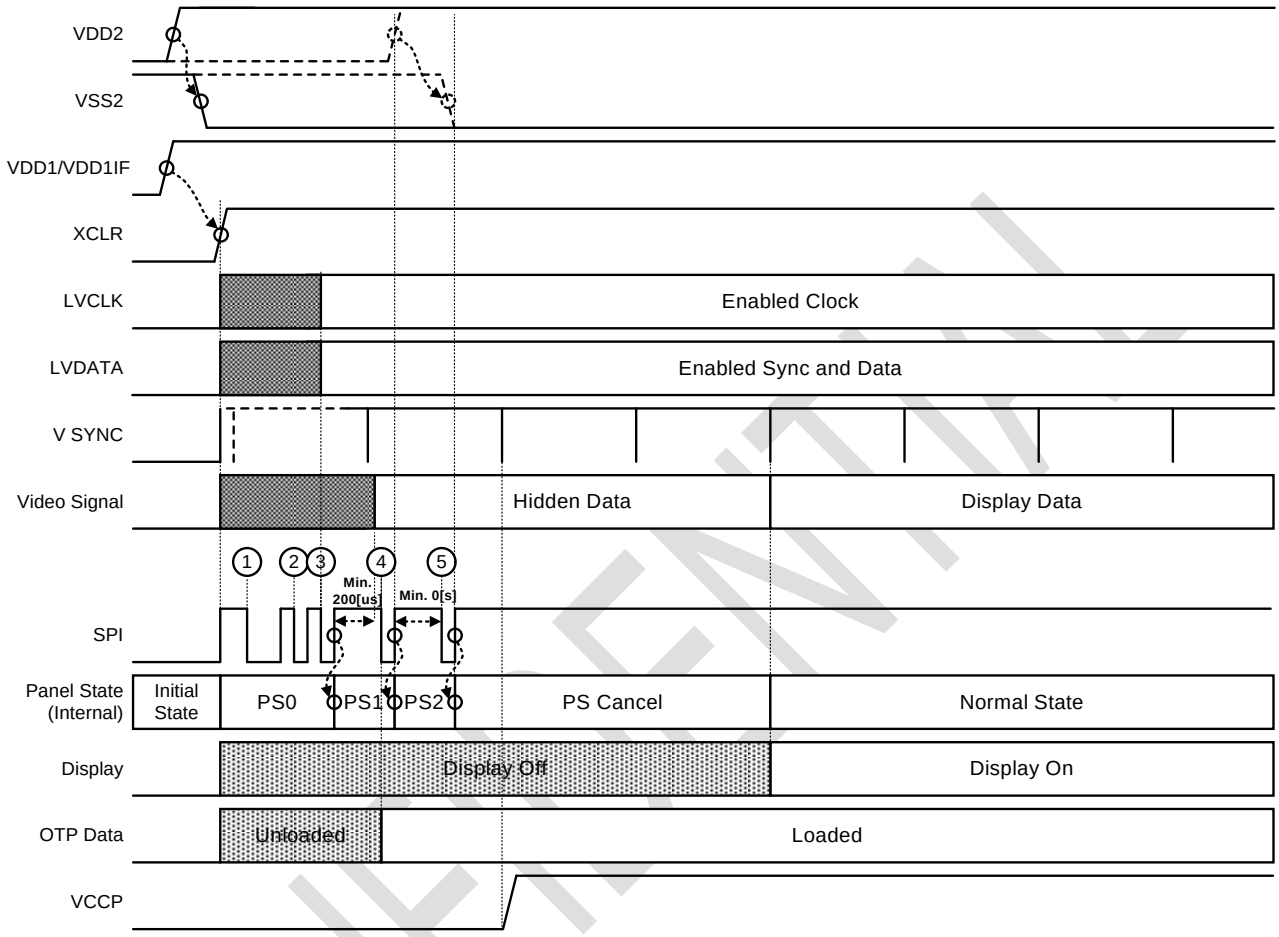


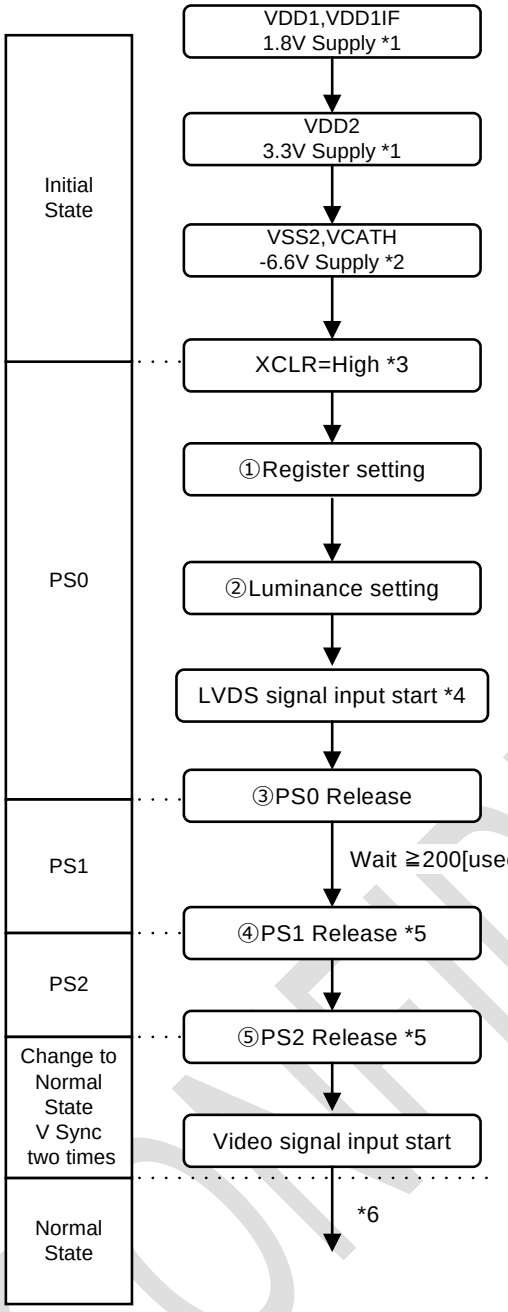
Read Access Burst Transfer（LSB First）

Unless XCS status is high, transfer mode is recognized as burst and the target address should automatically be incremented for every 8 data.

12 Sequence

12.1 ON Sequence





*1
Order of 1.8V supply and 3.3V supply can be swapped.

*2
Please surely supply -6.6V after 3.3 V supply.

*3
Please surely set XCLR to High, after 1.8V supply.

① Please set “Map 0”, address 0x01 to 0xBF. Register value depends on data format, resolution, etc.

② Luminance setting
“Address 0x10” should be “Data 0x0A”.
Please set Address 0x12, 0x13 (=/0x0F).
Value of Data depends on Luminance.
E.g. Data value can be 0x64 in case of 1000cd/cm2

*4
Please surely input H Sync, V Sync and LVCLK signals before ③ PS0 Release.

③ PS0 Release
“Address 0x00” should be “Data 0x01”.

④ PS1 Release
“Address 0x00” should be “Data 0x03”.

⑤ PS2 Release
“Address 0x00” should be “Data 0x07”.

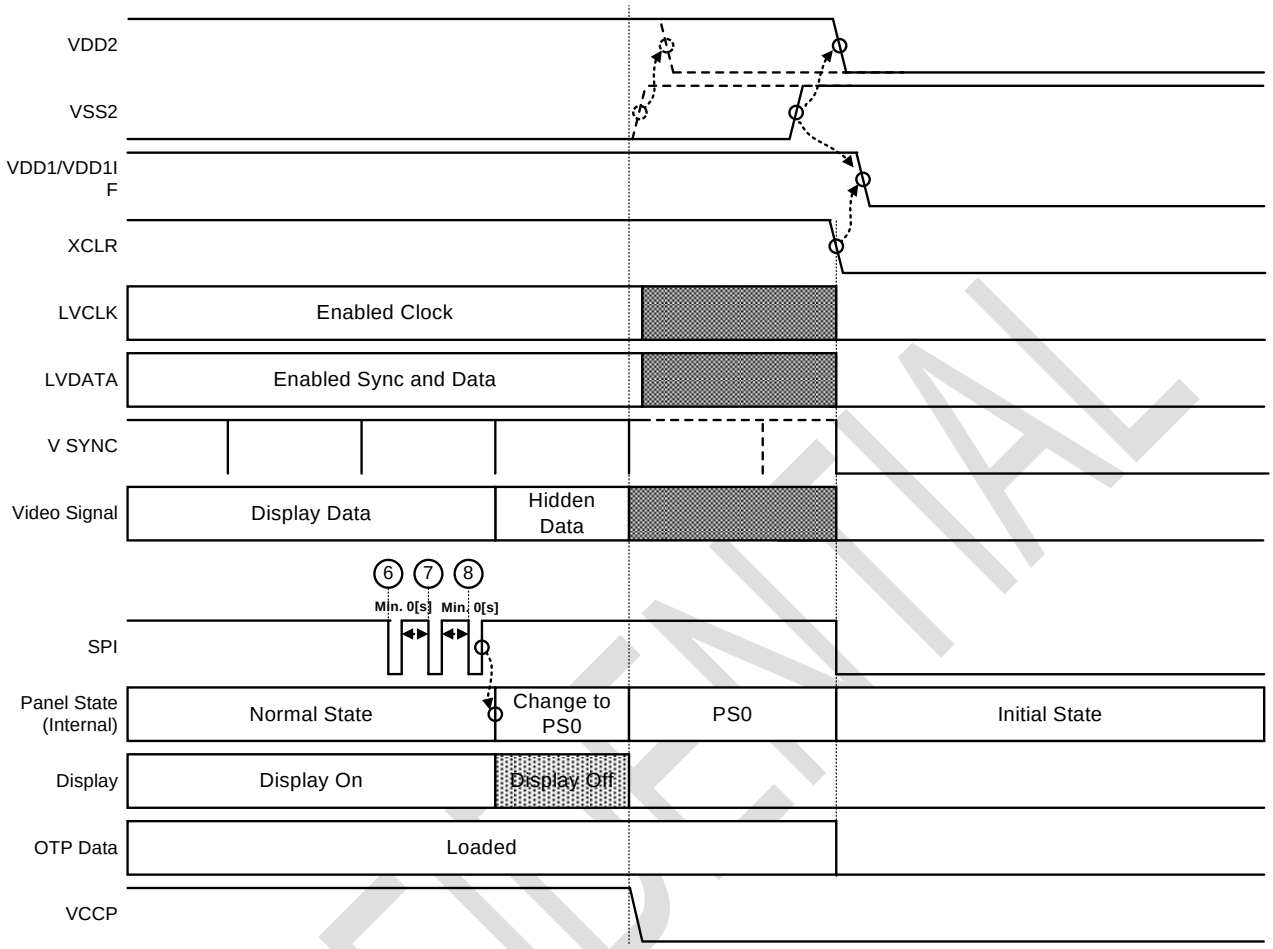
*5
④ and ⑤ can be simultaneously implemented.
To simultaneously implement, please set “Address 0x00” should be “Data 0x07”.

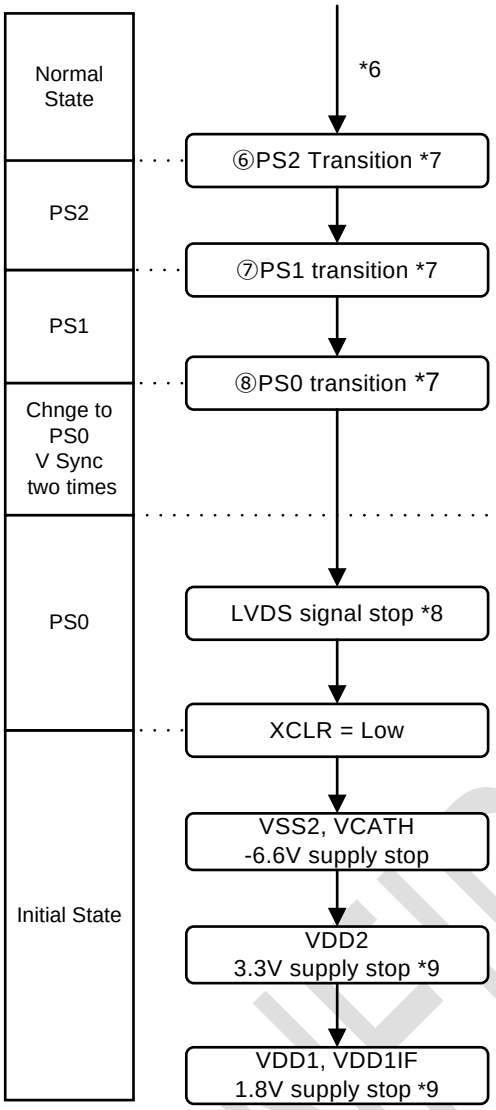
*6
The following data will be ignored except in Normal State.
・DE
・R[0]～[7]、G[0]～[7]、B[0]～[7]
・Y[0]～[7]、CB[0]～[7]、CR[0]～[7]

Register value can stay even in PS status unless XCLR=L.
Please surely supply -6.6V after +3.3V supply completed.
Please surely complete to supply +3.3V and -6V before timing of ⑤.

Initial State: Invalid status to read LVDS signal
PS0 : All Circuits are PS status. (Register setting is available, V synchronize register can be reflected at PS2.)
PS1 : I/F Circuits are active status. (Register setting is available, V synchronize register can be reflected at PS2. Available to read out OTP value in PS1.)
PS2 : Internal Clock is active status. (Register setting is available, Available to read out OTP value in PS2.)
Normal State: Valid status to read LVDS signal

12.2 OFF Sequence





*6
The following data will be ignored except in Normal State.
・DE
・R[0]～[7]、G[0]～[7]、B[0]～[7]
・Y[0]～[7]、CB[0]～[7]、CR[0]～[7]

⑥ Please transfer to PS2 status.
"Address 0x00" should be "Data 0x03".

⑦ Please transfer to PS1 status.
"Address 0x00" should be "Data 0x01".

⑧ Please transfer to PS0 status.
"Address 0x00" should be "Data 0x00".

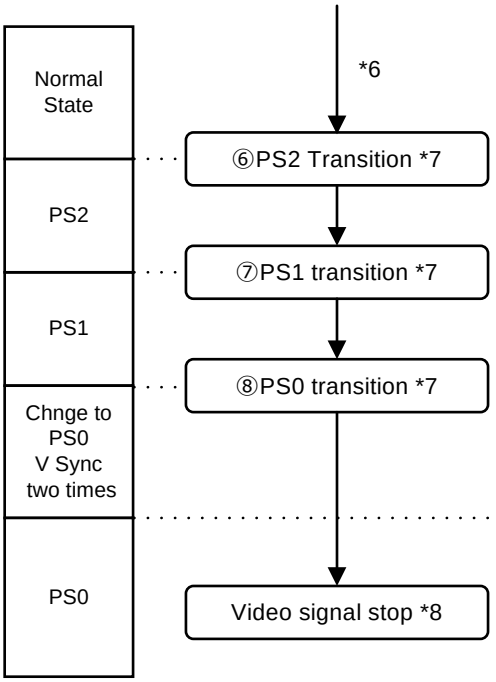
*7
Simultaneous implementation of ⑥⑦⑧ is available, but please make sure Address 0x00 should be Data0x00 in this case.

*8
Please surely send out V Synchronize signal two times.

*9
Order of 1.8V supply stop and 3.3V supply stop can be swapped.

Please surely turn off +3.3V after -6.6V completely turn off.
Please surely turn off 1.8V after XCLR setting with Low.

12.3 Power Save Transition



*6
The following data will be ignored except in Normal State.
・DE
・R[0]～[7]、G[0]～[7]、B[0]～[7]
・Y[0]～[7]、CB[0]～[7]、CR[0]～[7]

⑥ Please transfer to PS2 status.
"Address 0x00" should be "Data 0x03".

⑦ Please transfer to PS1 status.
"Address 0x00" should be "Data 0x01".

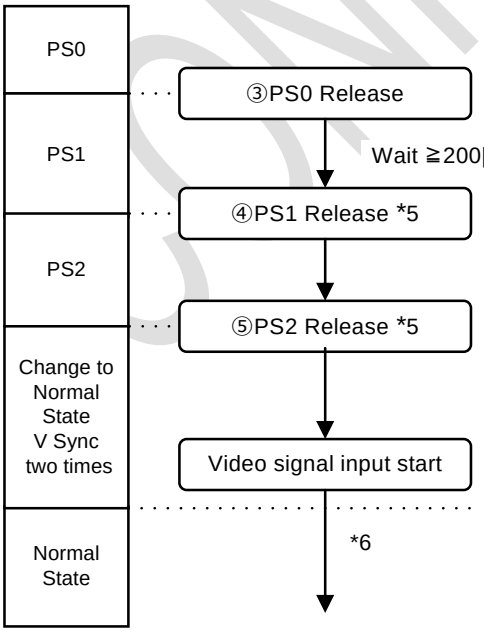
⑧ Please transfer to PS0 status.
"Address 0x00" should be "Data 0x00".

*7
Simultaneous implementation of ⑥⑦⑧ is available, but please make sure Address 0x00 should be Data0x00 in this case.

*8
Please surely send out V Synchronize signal two times.

Register value can stay even in PS status unless XCLR=L.

12.4 Power Save Release



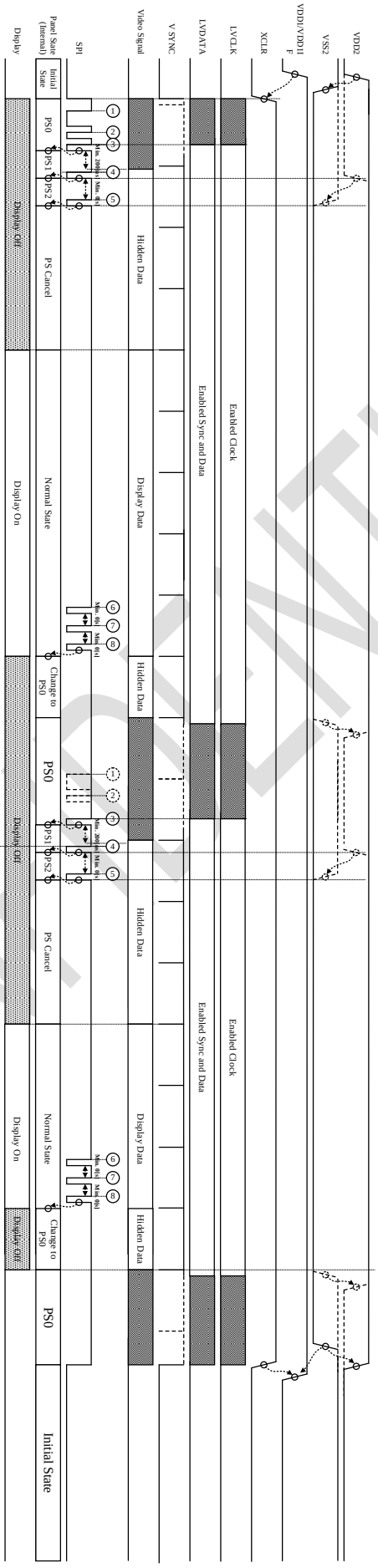
③ Please release PS0 status.
"Address 0x00" should be "Data 0x01".

④ Please release to PS1 status.
"Address 0x00" should be "Data 0x03".

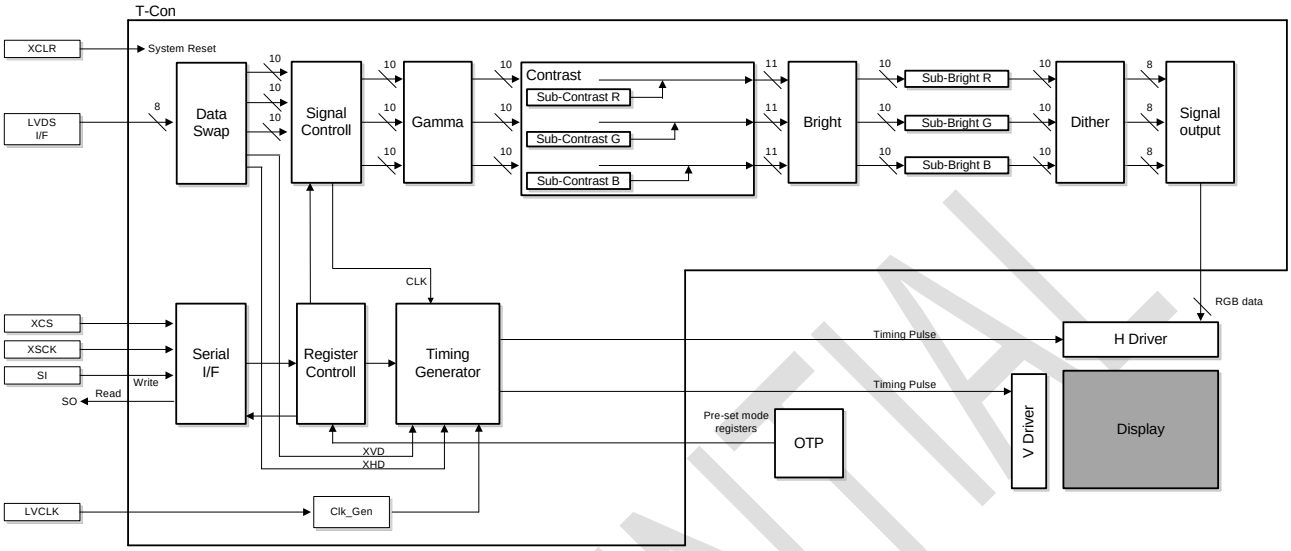
⑤ Please release to PS2 status.
"Address 0x00" should be "Data 0x07".

*5
Simultaneous implementation of ④⑤ is available, but please make sure Address 0x00 should be Data0x07 in this case.

*6
The following data will be ignored except in Normal State.
・DE
・R[0]～[7]、G[0]～[7]、B[0]～[7]
・Y[0]～[7]、CB[0]～[7]、CR[0]～[7]



13 T-CON Block Diagram



14 Functional Description and Settings

14.1 Swapping function

This function can swap input lanes and their polarity. There are three commands to swap, input port order and input lane order, their polarity.

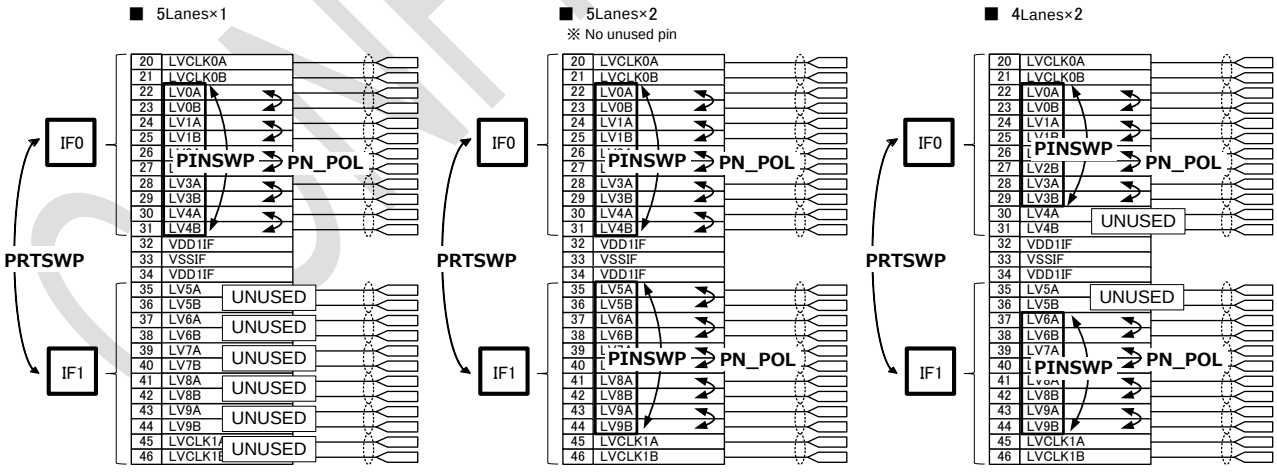
◆Register setting

Please execute this register setting only during PS0 state.

Address	DATA	Register	Function / Setting
0x04	[3]	PRTSWP	Selection of Input port order 0: Data input IF0 at first and then IF1 (Default) (*) 1: Data input IF1 at first and then IF0.
	[5:4]	PINSWP	Selection of Input lane order 00: IF0 Ascending order (LV0 to LV4) and IF1 Ascending order (LV5 to LV9) (Default) 01: IF0 Descending order (LV4 to LV0) and IF1 Ascending order (LV5 to LV9) 10: IF0 Ascending order (LV0 to LV4) and IF1 Descending order (LV9 to LV5) 11: IF0 Descending order (LV4 to LV0) and IF1 Descending order (LV9 to LV5)
	[7:6]	PN_POL	Selection of Input lane polarity 00: IF0 A=P B=N, IF1 A=P B=N (Default) 01: IF0 A=N B=P, IF1 A=P B=N 10: IF0 A=P B=N, IF1 A=N B=P 11: IF0 A=N B=P, IF1 A=N B=P

*IF0: (LV0～LV4)、IF1: (LV5～LV9)

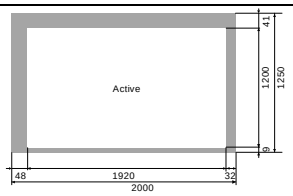
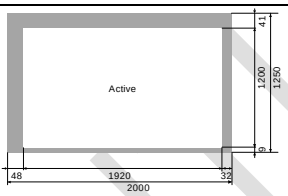
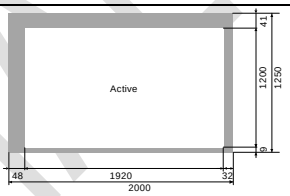
With this function usage, please pay attention about unused pin for each lane setting. And, please be noted that swapping function is invalid for unused pin, they are fixed.



14.2 Input Signal Data Format

Set the panel timing registers appropriately for the input signal data format.

◆Panel Display Modes, and Input Formats

		① WUXGA 120Hz Frame Rate	② WUXGA 60Hz Frame Rate	③ WUXGA 90Hz Frame Rate
Panel Display Modes		1920(H) x 1200(V)	1920(H) x 1200(V)	1920(H) x 1200(V)
Input Formats				
Active	H	1920	1920	1920
	V	1200	1200	1200
Total	H	2000	2000	2000
	V	1250	1250	1250
FP	H	32	32	32
	V	9	9	9
SYNC	H	16	16	16
	V	5	5	5
BP	H	32	32	32
	V	36	36	36
BP+SYNC	H	48	48	48
	V	41	41	41
fv	Hz	120.00	60.00	90.00
Pixel Clock	MHz	300	150	225
Lane*ch	-	5Lane*2	4Lane*2, 5Lane*1	5Lane*2

14.3 Dual line progressive drive

This ECX343E can achieve double refresh rate with the same power consumption by simultaneous drive of 2 vertical lines.

* In this mode, vertical direction resolution should be half because of 2 line simultaneous writing.

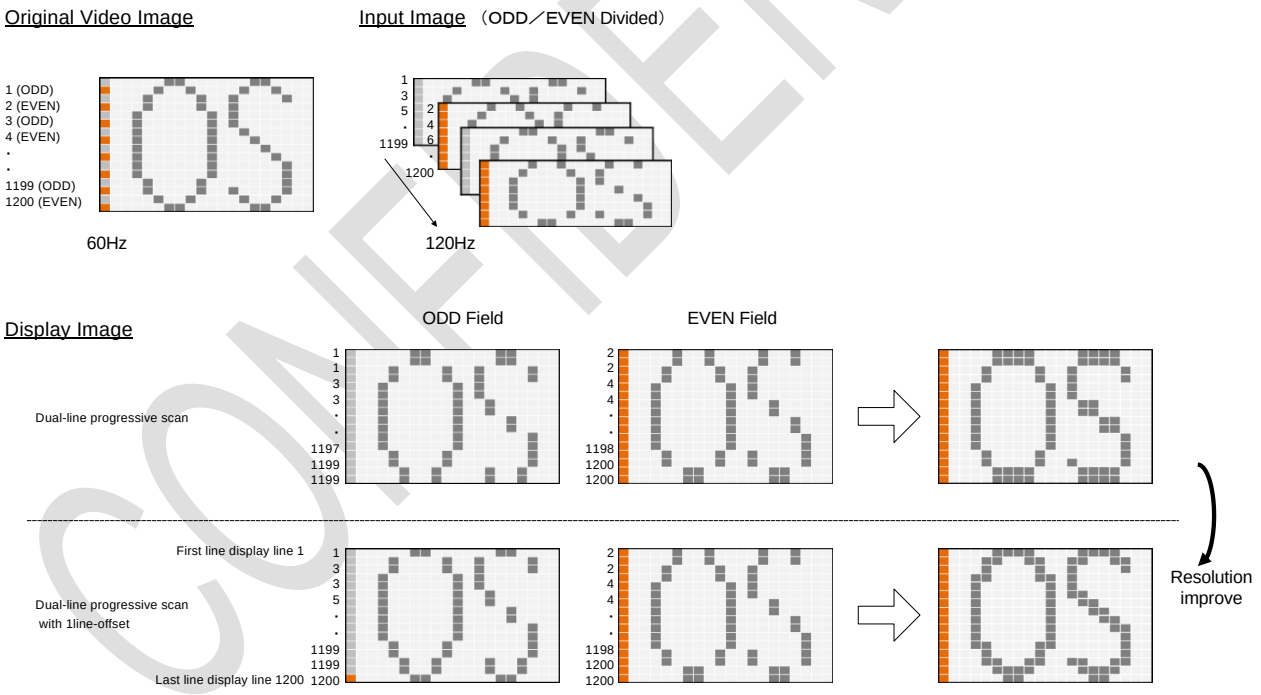
Dual-line progressive scan: Writing 2 vertical lines simultaneously and display “ODD” and “EVEN” field alternately.

Dual-line progressive scan with 1line-offset：Writing 2 vertical lines simultaneously and displaying “ODD” and “EVEN” field alternately. In this mode, vertical data of “ODD” filed is 1 line shifted from that of EVEN field. This driving method improves sacrifice of effective resolution in case of real progressive drive mode.

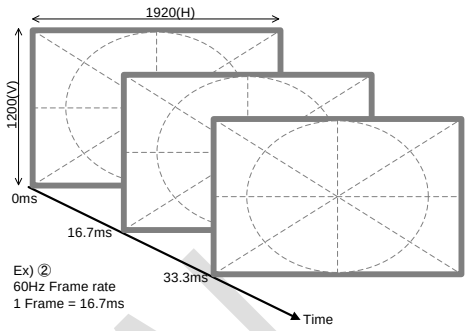
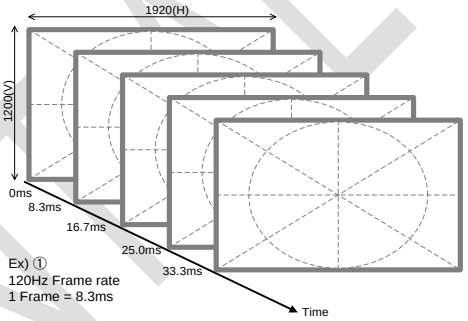
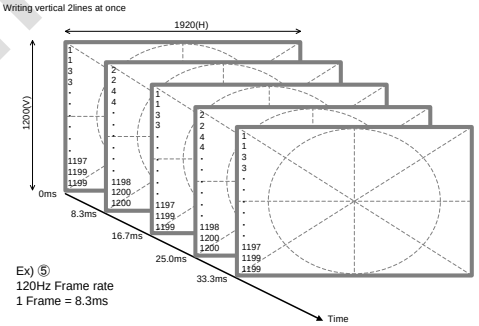
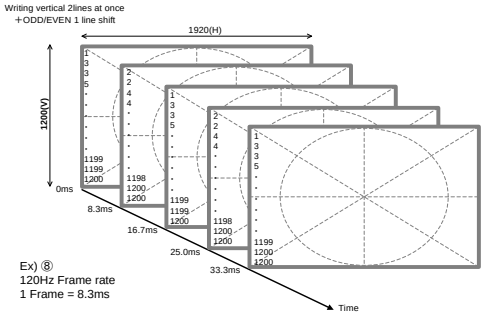
◆Register setting

Please execute this register setting only during PS0 state.

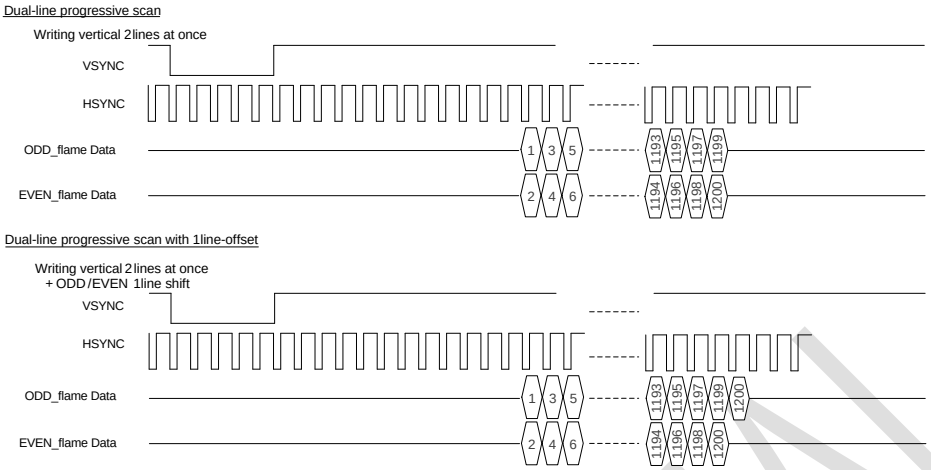
Address	DATA	Register	Function / Setting
0x3E	[7]	VDRMODE	Selection of VDR Mode or not 0: Invalid 1: Valid
	[6]	OESW	Selection of VDR Mode scan mode 0: Dual-line progressive scan 1: Dual-line progressive scan with 1line-offset



◆Input format and panel display image

Input format	VDRMODE	OESW	Panel display image
① 1920x1200 120Hz ② 1920x1200 60Hz ③ 1920x1200 90Hz 1920(H) x 1200(V)	0: Invalid	Don't care	
	0: Invalid	Don't care	
④ 1920x600 240Hz ⑤ 1920x600 120Hz ⑥ 1920x600 180Hz ODD 1920(H) x 600(V) EVEN 1920(H) x 600(V)	1: Valid	0: Dual-line progressive scan	
⑦ 1920x601,600 240Hz ⑧ 1920x601,600 120Hz ⑨ 1920x601,600 180Hz ODD 1920(H) x 601(V) EVEN 1920(H) x 600(V)	1: Valid	1: Dual-line progressive scan with 1line-offset	

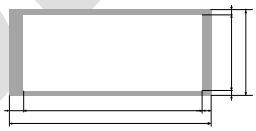
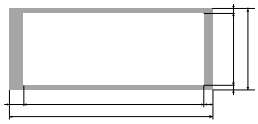
◆Input format



After setting PS2EN from 0 to 1, the first display will be XVD and the second will be the ODD field.

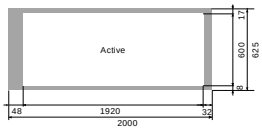
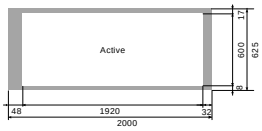
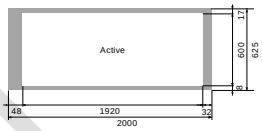
◆Panel Display Modes, and Input Formats

Dual-line progressive scan

Panel Display Modes		④ WUXGA 240Hz Frame Rate	⑤ WUXGA 120Hz Frame Rate	⑥ WUXGA 180Hz Frame Rate
Input Formats				
Active	H	1920	1920	1920
	V	600	600	600
Total	H	2000	2000	2000
	V	625	625	625
FP	H	32	32	32
	V	8	8	8
SYNC	H	16	16	16
	V	5	5	5
BP	H	32	32	32
	V	12	12	12
BP+SYNC	H	48	48	48
	V	17	17	17
fv	Hz	240.00	120.00	180.00
Pixel Clock	MHz	300.00	150.000	225.00
Lane*ch	-	5Lane*2	4Lane*2, 5Lane*1	5Lane*2

SONY

Dual-line progressive scan with 1line-offset

Panel Display Modes		⑦ WUXGA 240Hz Frame Rate 1920(H) x 600(V)	⑧ WUXGA 120Hz Frame Rate 1920(H) x 600(V)	⑨ WUXGA 180Hz Frame Rate 1920(H) x 600(V)
Input Formats				
Active	H	1920	1920	1920
	V	ODD/EVEN=601/600	ODD/EVEN=601/600	ODD/EVEN=601/600
Total	H	2000	2000	2000
	V	ODD/EVEN=626/625	ODD/EVEN=626/625	ODD/EVEN=626/625
FP	H	32	32	32
	V	8	8	8
SYNC	H	16	16	16
	V	5	5	5
BP	H	32	32	32
	V	12	12	12
BP+SYNC	H	48	48	48
	V	17	17	17
fv	Hz	240.00	120.00	180.00
Pixel Clock	MHz	300.00	150.00	225.00
Lane*ch	-	5Lane*2	4Lane*2, 5Lane*1	5Lane*2

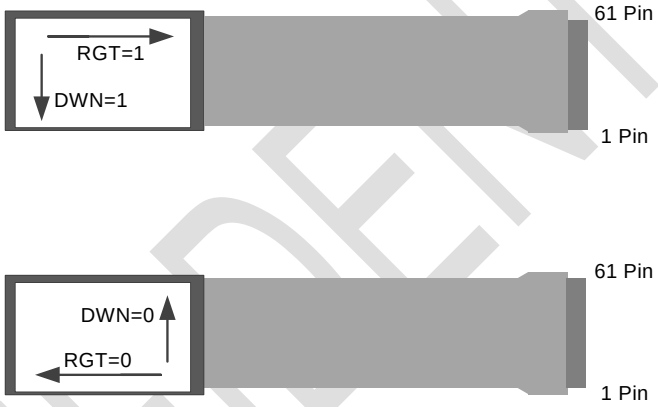
14.4 Up/down and Right/left Inversion Function

Up/down and right/left inverse display of the panel are set by the registers RGT and DWN, respectively.

◆Register setting

Please execute this register setting only during PS0 state.

Address	DATA	Register	Function / Setting
0x02	[2]	RGT	Selection of rightward / leftward scan 0: Leftward scan 1: Rightward scan (Default)
	[3]	DWN	Selection of upward / downward scan 0: Upward scan 1: Downward scan (Default)



14.5 Data trigger timing by Date Enable (DE)

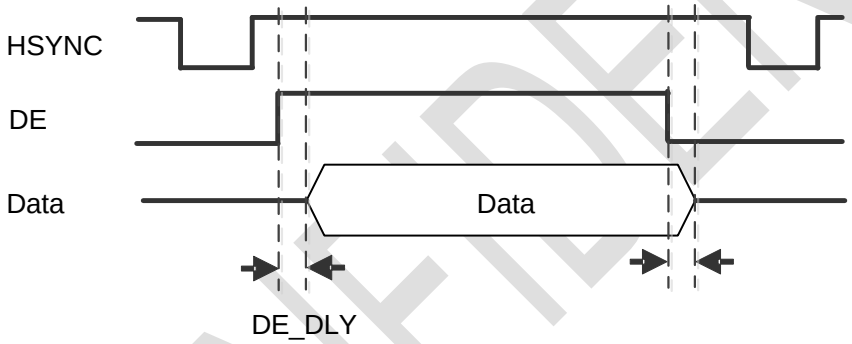
Data Enable (DE) signal can specify trigger timing to capture Display Data, instead of HSYNC signa trigger. The capture timing with DE can function based on following register setting.

◆Register setting

Please execute this register setting only during PS0 state.

Address	DATA	Register	Function / Setting
0x02	[4]	DE_SEL	Selecting valid trigger, DE or HSYNC signal. 0: DE (Default) 1: HSYNC
	[1:0]	DE_DLY	Delay time between DE trigger and Data capture, in case of DE function. 00: 0 (CLK) (Default) 01: 1 10: 2 11: 3

Data capturing scheme based on DE signal



14.6 Luminance setting function

This product has two options to specify luminance value. One is to directly specify arbitrary value (13.6.1 Arbitrary luminance value setting) and another is to select suitable luminance value from Pre-set modes (13.6.2 Preset luminance setting).
By reflecting all register values in 8. Register Map, luminance can be adjusted to 3,500cd/m2 based on Arbitrary luminance value setting.

◆Register Setting

Please execute this register setting in other than initial state. Latest register setting can be reflected at next coming V sync signal.

Address	DATA	Register	Function / Setting
0x10	[1]	L_AT_CALEN	Luminance setting 0: Preset Mode 1: REQUEST_LV (Default)
	[3]	WB_CALEN	Auto adjustment of white balance in case this function is valid. 0: Preset Mode 1: REQUEST_LV (Default)

14.6.1 Arbitrary luminance value setting

This product allows you to set the peak luminance.

◆Register Setting

Address	DATA	Register	Function / Setting
0x12 0x13	[1:0] [7:0]	REQUEST_LV	Luminance setting register 0001100100: 1000cd/m^2 | 0111110100: 5000cd/m^2 *Be sure to enter a value between 1000 and 5000cd/ m^2. (Default 0101011110: 3500cd/m^2)

14.6.2 Preset luminance setting

This product has 2 luminance preset modes.
By selecting the mode according to the register LUMINANCE, the luminance and the white chromaticity are adjusted to preset value

◆Register Settings

Address	Data	Register	Function / Setting
0x07	[0]	LUMINANCE	Luminance preset mode selection 0: 500cd/m^2 (Default) 1: 1000cd/m^2

14.7 Luminance changing speed

When luminance is changed by arbitrary luminance value setting command, dynamic changing speed (slope) is selectable, “slow” to “fast” with 7 slopes. Prompt luminance change can be noticeable. It is available to select adequate slope based on customer application and usage condition.

◆Register setting

Please execute this register setting in other than initial state. Latest register setting can be reflected at next coming V sync signal.

Address	DATA	Register	Function / Setting
0x10	[2]	L_SEAMLESSEN	Luminance change speed function 0: Invalid 1: Valid (Default)
0x0F	[6:4]	C_SLOPE	Luminance change speed synchronized with Vertical signal 000(0) : Prompt Transition (Default) 001(1) : Slow Speed | 111(7) : Fast Speed

14.8 Direct duty setting

ECX343EN display can adjust Duty ratio with specified value as you want. Duty ratio can be adjusted between more than 0% and less than 90%. (technically available to set 0%, however, not able to execute completed 0%.) And, this function is not valid with Global Illumination mode.

Luminance value set by “14.6 Luminance setting function” is defined with 90% duty ratio condition.
With Direct duty setting, it is possible to change Luminance value of 90% duty ratio by adjustment of duty ratio. For example, you can decrease luminance to 250cd/m2 (duty 45% setting) from 500cd/m2 (duty 90%, default condition).

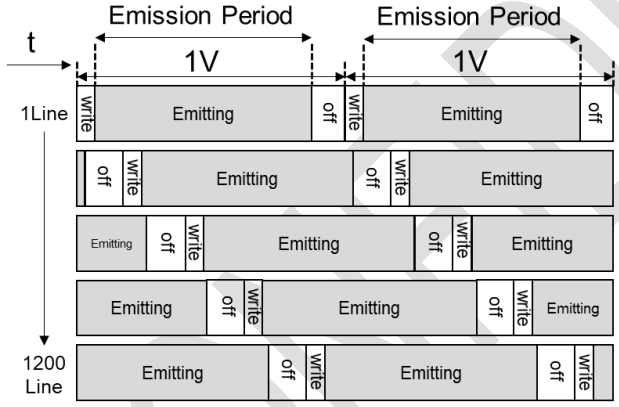
◆Register setting

Address	DATA	Register	Function
0x8B	[6:0]	DUTYCYCLE	Setting Duty ratio with Decimal value as percentage. (e.g. “0x5A” as Duty ration 90%) (Default 1011010:90%)
0x8B	[7]	DT_AT_CALEN	Activate(on) or Non-activate(off) Duty ratio calculation circuit. 0: off 1: on (Default)

Duty：Emission period ratio in 1 vertical scan period, can be defined with following formula.

Duty [%]= (Emission Period) / (1V Period)

Rolling illumination



14.9 Global Illumination

This function is emitting all lines at simultaneously instead one by one line emitting (Rolling Emitting).

Writing all data in one frame period and then emitting all lines simultaneously at next coming one frame.
Following figure in below is comparison between normal mode and the Global illumination mode.
Since video data writing is skipped for each frame, the real frame rate is halved.

Please set the register below additionally to "9 Register Map".

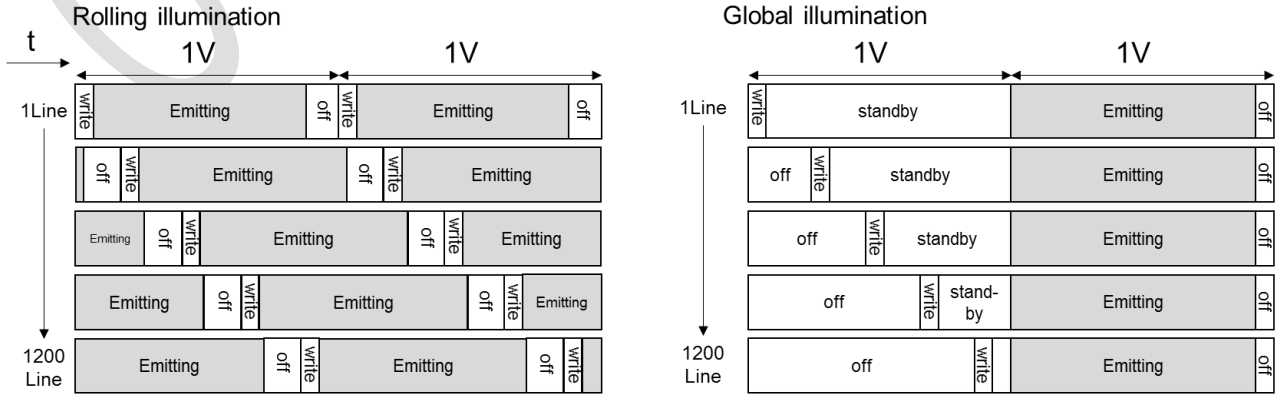
◆Register setting

Please execute this register setting only during PS0 state.

Address	DATA	Register	Function / Setting
0x77	[0]	FRAME_MD	Selection of Rolling illumination / Global illumination 0: Rolling illumination (Default) 1: Global illumination

◆Register settings for Global illumination
(The following register settings are 49% of the maximum duty.)

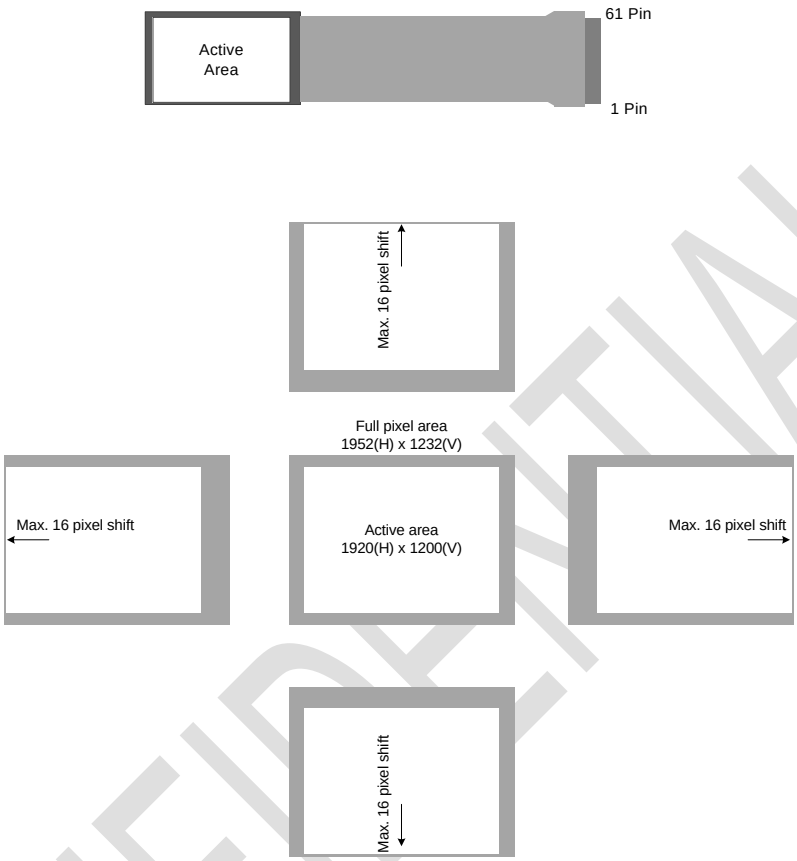
	Progressive				Dual-line progressive				Dual-line progressive with 1line offset			
Address	120Hz 5Lx2	60Hz 5Lx1	60Hz 4Lx2	90Hz 5Lx2	240Hz 5Lx2	120Hz 5Lx1	120Hz 4Lx2	180Hz 5Lx2	240Hz 5Lx2	120Hz 5Lx1	120Hz 4Lx2	180Hz 5Lx2
0x10	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F	1F
0x4E	00	00	00	00	00	00	00	00	00	00	00	00
0x4F	19	19	19	19	09	09	09	09	09	09	09	09
0x54	0F	0F	0F	0F	08	08	08	08	08	08	08	08
0x55	FF	FF	FF	FF	00	00	00	00	00	00	00	00
0x77	01	01	01	01	01	01	01	01	01	01	01	01
0x78	04	04	04	04	02	02	02	02	02	02	02	02
0x79	FB	FB	FB	FB	79	79	79	79	79	79	79	79
0x7A	09	09	09	09	04	04	04	04	04	04	04	04
0x7B	C3	C3	C3	C3	E1	E1	E1	E1	E1	E1	E1	E1
0x7D	FA	FA	FA	FA	FA	FA	FA	FA	FA	FA	FA	FA
0x8B	5A	5A	5A	5A	5A	5A	5A	5A	5A	5A	5A	5A
0xF2	01	01	01	01	00	00	00	00	00	00	00	00
0xF3	38	38	38	38	9C	9C	9C	9C	9C	9C	9C	9C



When global illumination is used, the luminance decreases due to the emitting time.

14.10 Orbit Function

Scanning start position of data image can be changed. This enables reducing of unwanted noticeability of local luminance drop, so called bun-in. As other wording, this function is called “Pixel Shifting” or “Pixel Orbit”. This approach is common technic to alleviate burn-in for self-emitting display.



◆Register Settings

Please execute this register setting in other than initial state. Latest register setting can be reflected at next coming V sync signal.

Address	DATA	Register	Function / Setting
0x05	[5:0]	ORBIT_H	Horizontal orbit adjustment 110000: -16 pixels | 000000: center(Default) | 010000: +16 pixels
0x06	[5:0]	ORBIT_V	Vertical orbit adjustment 110000: -16 pixels | 000000: center(Default) | 010000: +16 pixels

14.10.1 Horizontal Display Position Shift

The horizontal display start position can be changed by the register ORBIT_H. The variable range is ± 16 pixels.

ORBIT_H setting value	-16	…	-1	0 (Default)	1	…	16
Register input value (Two's compllement)	110000		111111	000000	000001		010000
Number of pixels shifted	Leftward 16-pixel	…	Leftward 1-pixel	Center	Rightward 1-pixel	…	Rightward 16-pixel

14.10.2 Vertical Display Position Shift

The vertical display start position can be changed by the register ORBIT_V. The variable range is ± 16 pixels.

ORBIT_V setting value	-16	…	-1	0 (Default)	1	…	16
Register input value (Two's compllement)	110000		111111	000000	000001		010000
Number of pixels shifted	Downward 16-pixel	…	Downward 1-pixel	Center	Upward 1-pixel	…	Upward 16-pixel

14.10.3 Number of shifted pixels in case Dual line progressive drive

Number of shifted pixels can be following in case implementing 2 line simultaneous writing.

ORBIT_V setting value	-16	-15	-14	-13	・・・	・・・	-4	-3	-2	-1	0	1	2	3	・・・	・・・	12	13	14	15	16
Number of shift pixels in case 1 line writing	-16	-15	-14	-13	・・・	・・・	-4	-3	-2	-1	0	1	2	3	・・・	・・・	12	13	14	15	16
Number of shift pixels in case 2 lines simultaneously writing	-16		-14		・・・		-4		-2		0		2		・・・		12		14		16

15 Optical Characteristics

15.1 Optical Characteristics

Item			Symbol	Min.	Typ.	Max.	Unit
Luminance tolerance (255Level)	Preset Mode :0		L0	-15		+15	%
	Preset Mode :1		L1	-15		+15	%
	REQUEST_LV=100 to 500		Lv	-15		+15	%
White Chromaticity tolerance (255 level)	White Preset Mode :0		WL0x,	0.298	0.313	0.328	CIE
			WL0y,	0.314	0.329	0.344	CIE
	White Preset Mode :1		WL1x	0.298	0.313	0.328	CIE
			WL1y	0.314	0.329	0.344	CIE
	White REQUEST_LV=100 to 500		Wx	0.298	0.313	0.328	CIE
			Wy	0.314	0.329	0.344	CIE
White Chromaticity tolerance (192, 128 level)	White REQUEST_LV=350		WGx	0.298	0.313	0.328	CIE
			WGy	0.314	0.329	0.344	CIE
Monochrome chromaticity	White REQUEST_LV =350	R	Rx	0.635	0.655	0.675	CIE
			Ry	0.310	0.330	0.350	CIE
		G	Gx	0.265	0.285	0.305	CIE
			Gy	0.580	0.600	0.620	CIE
		B	Bx	0.120	0.140	0.160	CIE
			By	0.045	0.065	0.085	CIE
Contrast Ratio	White REQUEST_LV=500		CR	100,000:1	—	—	

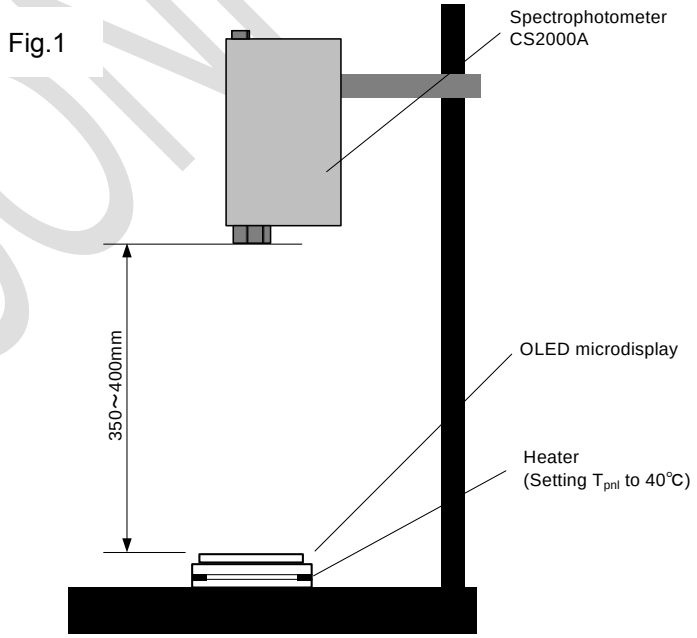
L : White Luminance

15.2 Measurement System and Measurement Condition

Measurement temperature: T_{pnl} = 40°C
Measurement point: One point on the screen center
Register setting: “OTPCALDAC_REGEN” = 0、”OTPDG_REGEN” = 0 (preset mode valid)

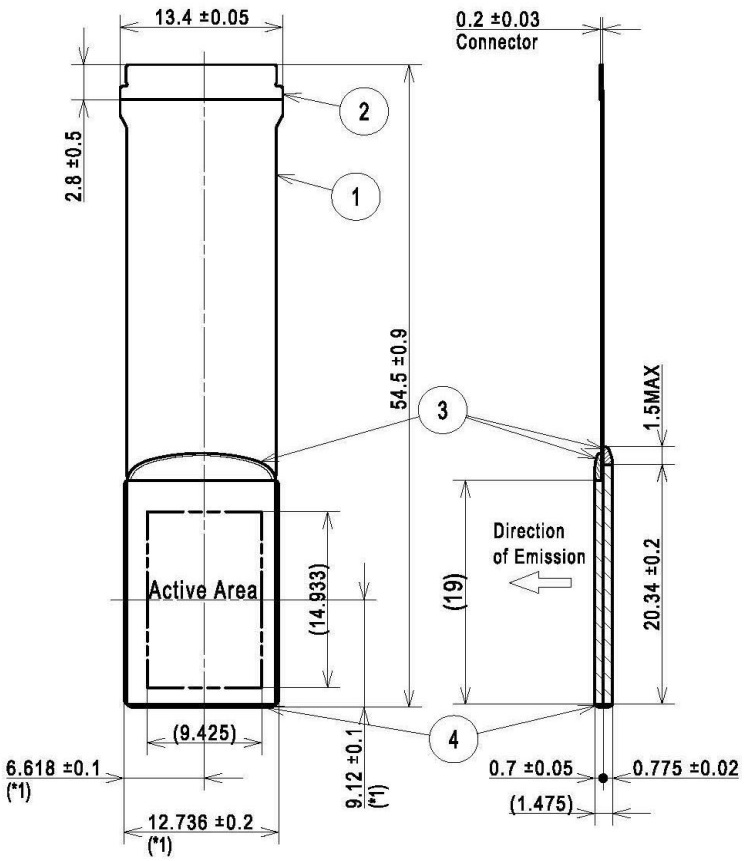
Item		Pattern	Luminance	Gray Level	Measurement Condition
Luminance / White chromaticity (255 level)	L0, L1, Lv / WL0x, WL0y WL1x, WL1y Wx, Wy	all white	L0, L1, REQUEST_LV=100 to 500	R=255 G=255 B=255	Fig.1
White chromaticity (192 level)	WGx, WGy	all white	REQUEST_LV=350	R=192 G=192 B=192	Fig.1
White chromaticity (128 level)				R=128 G=128 B=128	
Monochrome chromaticity	Rx,Ry	Monochrome (all red, all green, all blue)	REQUEST_LV=350	R=255	Fig.1
	Gx,Gy			G=255	
	Bx,By			B=255	
Contrast	CR	all white and all black	REQUEST_LV=500	White: R=255 G=255 B=255 Black: R=0 G=0 B=0	Fig.1

Fig.1

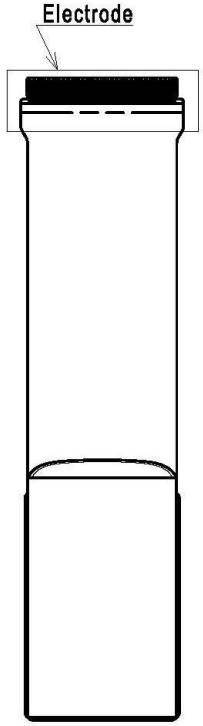


16 Module Outline

Unit : mm

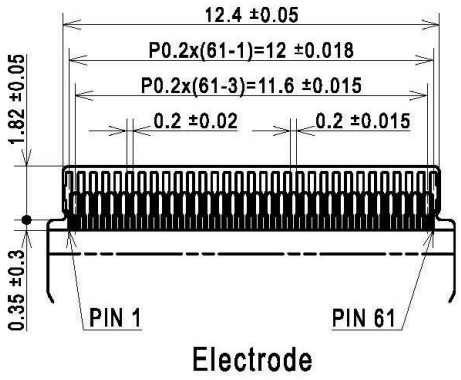


*1:including End-face coating



No	Description
1	FPC
2	Stiffener
3	Reinforcing Material
4	End-face coating

Mass 0.9g



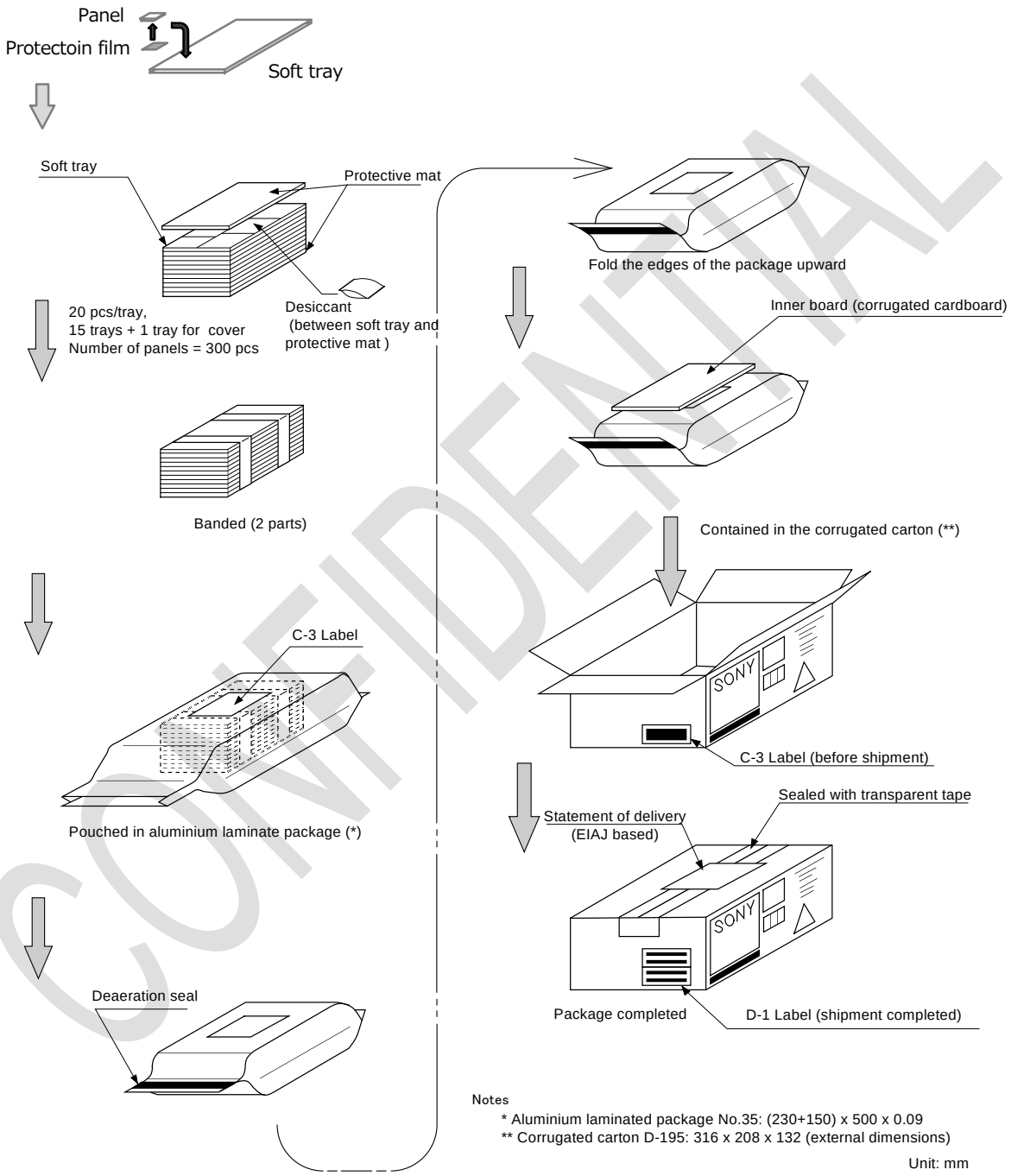
Electrode

Recommended Connector

Manufacturer	JST Connector
Part Number	61 FVXS - RSM1 - GAN - TF

17 Packing Specification

Forms : Soft tray（20 pieces）
Carton（20 pieces x 15 trays = 300 pieces



Notes
* Aluminium laminated package No.35: (230+150) x 500 x 0.09
** Corrugated carton D-195: 316 x 208 x 132 (external dimensions)

Unit: mm

18 Notes on Handling Module

18.1 Static charge prevention

Be sure to take the following protective measures. Organic EL panels are easily damaged by static charges.

(1) Use non-chargeable gloves or handle with bare hands.
(2) Use a wrist strap connecting ground when handling.
(3) Do not touch any electrodes on the panel.
(4) Wear non-chargeable clothes and conductive shoes.
(5) Install grounded conductive mats on the working floor and working table.
(6) Keep the panel away from any charged materials.

18.2 Protection from dust and dirt

(7) Operate in a clean environment.
(8) Do not touch the panel surface. The surface is easily scratched.
When cleaning on panel surface, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.
(9) Use ionized air to blow dust off the panel surface.

18.3 Others

(10) Not hold FPC (Flexible Printed Circuit), not twist the FPC, not bend FPC because connection area between the FPC and panel is easily broken by mechanical stress.
(11) The minimum fold radius of the FPC is 1.0 mm, So, do not fold the FPC less than 1.0mm radius.
(12) Do not drop the module.
(13) Do not twist or bend the module.
(14) Keep the module away from heat sources.
(15) Not be close the module to water or other solvents.
(16) Do not store or use the module at high temperatures or high humidity circumstance, as the circumstance may affect module specifications.
(17) When disposing of this, regard it as industrial waste and please comply with related regulations.
(18) Do not store or use the panel in reactive chemical substance (including alcohol) environments, as these may affect the specifications. .
(19) This module is supposed to be delivered in a degassed aluminum laminated bag.
When storing this panel again after once unsealing the bag, please take following action. Put it into the aluminum laminated bag again. Put in desiccant into the aluminum bag and the opening of the aluminum bag should be folded and seal the bag with tape.

19 Notice

19.1 Purpose of Use of ECX343EN:

Customer who use the Products (“Customer”) with the utmost concern for safety, and shall not use the Products for any purpose that may endanger life or physical wellbeing, or cause serious damage to property or the environment, either through normal use or malfunction.

Use of the Products for purposes other than those stipulated in this specification is strictly prohibited.

Furthermore, use of the Products for military purposes is strictly prohibited at all times.

19.2 Safe Design:

Customer is responsible for taking due care to ensure the product safety design of its products in which the Products are incorporated, such as by incorporating redundancy, anti-conflagration features, and features to prevent mis-operation, in order to prevent accidents resulting in injury, death, fire, or other social damage as a result of failure.

19.3 Product Information:

The product specifications, circuit examples, and any and all other technical information and content contained in this specification, as well as any other information and materials provided to Customer in connection with the Products (collectively, “Product Information”) have been provided to Customer for reference purpose only, and the availability and disclosure of such Product Information and its usage by Customer shall not be construed as giving any indication that Sony, its subsidiaries and/or its licensors will license any right, including intellectual property rights in such Product Information by any implication or otherwise.

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Ensure that you have read and reviewed the notices contained in our delivery specification as well as this specification when purchasing and using the Products.

20 Revision history

ECX343EN			
Ver.	Date	Page	Changes
0.1	2021.06.16	—	First edition created
1.0	2021.06.21	42	Global illumination Register settings correction (Address:0x4F,0x79)
	2021.06.25	15	Register Map Address:0x0F “C-SLOPE” addition
		41	Luminance changing speed “L_SEAMLESSEN” Address:0x10
	2021.09.02	6	Current Consumption Updated
		16	Register Map Address:0xF2 to :0xFE correction
		42	Global illumination Register settings correction (Address: :0x10, 0xF2 and 0xF3)
		45	Monochrome chromaticity Updated
		47	Module Outline Updated
	2021.09.10	17	Video Signal Transfer Format Addition of correspondence table between FR and IF mapping
1.1	2021.10.28	1,2	Built-in Sequence ~~Functions~~ → Features
		26,28,29	Sequence flow chart revised
		34	Correction of errors Register add : ~~0x38~~ → 0x3E
		2,42	Direct duty setting added
		43	Revised resister settings for global illumination
		58	Notes on handling module added
1.2	2021.11.10	15,16	Revised register map
		9	Delete ‘Clock duty’