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PRODUCT SPECIFICATION
产品规格书

PRODUCT **产品名称:**	**AMOLED MODULE**
MODEL NO. **模块型号：**	ET014WE01-GT
REVISON **文件版本：**	**1.0**
CUSTOMER **客户：**	**COMMON**
DATE **日期：**	**2022-11-24**

Proposed by			**Customer's Approval**
Designed	**Checked**	**Approved**	

■ REVISION RECORD
修改记录

REV NO. 版本号	REV DATE 修改日期	CONTENTS 内容	REMARKS 注释
1.0	2022-11-24	First release	

CONTENTS 内容

2 Features

2.1 Product Applications

Smart Watch(On-cell)

2.2 Product Features

1) Display color：16.7M (RGB x 24bits)
2) Display format：1.43”(466RGBx466)
3) Pixel arrangement：Real RGB arrangement
4) Interface：QSPI
5) Driver IC: ICNA3310B

3 Maximum rating

Parameter	Symbol	Spec			Unit	Note
		Min.	Typ.	Max.		
Analog/boost power voltage	VCI	-0.3	-	5.5	V	-
I/O voltage	VDDIO	-0.3	-	5.5	V	-
Operating temperature	Top	-20	-	70	℃	-
Storage temperature	Tstg	-40	-	80	℃	-

4 Mechanical Specifications

Item	Specification	unit
Dimension outline	42.62(V) x 42.70(W) x 2.43(T)	mm
LTPS Glass outline	39.34(V) x 39.55(W)	mm
Encapsulation Glass outline	38.65(V) x 39.55(W)	mm
Number of dots	466(W) x RGB x 466(H)	dots
Active area	φ36.35	mm
Diagonal size	1.43	inch
Pixel pitch	78 x 78	μm
Glass thickness	0.3 / 0.2	mm

5 Electrical Specifications

5.1 Electrical Characteristics

5.1.1 Power Characteristic：

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
AMOLED Power positive	ELVDD	3.25	3.3	3.35	V	-
AMOLED power Negative	ELVSS	-3.25	-3.3	-3.35	V	Ref
Digital Power supply	VDDIO	1.7	1.8	1.95	V	Ref
Analog Power supply	VCI	3.25	3.3	3.35	V	Ref

1) Normal Mode

Power Supply: IOVCC=1.8V VCI=3.3V ELVSS=-3.3V ELVDD=3.3V

Frame Frequency: F_{frame} =60HZ @ 25degC, Brightness 450 nits, Command Mode,

Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
100% Pixel On 450nits	IELVDD /ELVSS	-	33	38	mA	Ref
	IVCI	-	6	7.2	mA	Ref
	IVDDIO	-	3	3.6	mA	Ref

2) Idle Mode

Power Supply: IOVCC=1.8V VCI=2.8V

Frame Frequency: F_{frame} =15HZ @ 25degC, Brightness:100nits, OPR:10%,Command Mode(driver ic for power)

Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
10% Pixel On 100 nits	IELVDD /ELVSS	-	-	-	mA	Supplied by Driver IC
	IVCI	-	5	6	mA	Ref
	IVDDIO	-	1.2	1.5	mA	Ref

3) Deep Standby Mode

Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
Deep Standby(Vci Off)	Power Consumption	-	-	<50	uW	Ref

5.1.2 Driver IC：

ICNA3310 (refer to the datasheet)

5.1.3 Power IC：

1) BV6804/BV6802A(refer to the datasheet)

5.1.4 TP IC Recommended Operating Conditions (Suggestion):

FT3168(refer to the datasheet)

5.2 I/O Connection and Block Diagrams

5.2.1 Main FPC Bonding PAD Define

Pin No.	Symbol	I/O	Function Description
1	ELVSS1	Power	AMOLED power Negative
2	ELVSS2	Power	AMOLED power Negative
3	ELVDD1	Power	AMOLED power Positive
4	ELVDD2	Power	AMOLED power Positive
5	FOG	-	Test pin
6	FOG/FOF	-	Test pin
7	FOF	-	Test pin
8	VREFP5	Power	No connection
9	VREFN5	Power	OLED drive voltages
10	BVP3D	Power	AMOLED power Positive in idle mode
11	BVN3D	Power	AMOLED power Negative in idle mode
12	VCL	Power	Driver IC internal power
13	VREF	Power	Driver IC internal power
14	VCI	Power	Driver IC analog supply
15	VCI	Power	Driver IC analog supply
16	TE1	O	Tearing effect output pin
17	SWIRE	O	Swire protocol setting pin of Power IC
18	TE	O	Tearing effect output pin
19	RESX	I	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
20	SDO	O	Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal.
21	SDI_RDX	I	Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal.
22	DCX	I	Display data / command selection in 80-series MPU I/F and 4-wire SPI I/F.
			D/CX = ”0” : Command D/CX = ”1” : Display data or Parameter
23	WRX_SCL	I	A synchronous clock signal in SPI I/F.

24	**CSX**	I	Chip select input pin (“Low” enable)
25	**D0**	O	8-bit-directional data bus for 80-series MPU I/F and 8-bit input data bus for RGB I/F
26	**D1**	O	8-bit-directional data bus for 80-series MPU I/F and 8-bit input data bus for RGB I/F
27	**IM1**	I	Interface type selection.
28	**IM0**	I	Interface type selection.
29	**DSWAP**	I	Input pin to select HSSI_D0/D1 data lane sequence in high speed interface only
30	**PSWAP**	I	Input pin to select HSSI_D0/D1 data lane polarity in high speed interface only
31	**VDDIO**	Power	Driver IC digital I/O supply
32	**VDDIO**	Power	Driver IC digital I/O supply
33	**DVDD**	Power	Driver IC analog supply
34	**DGND**	Power	The power ground
35	**HSSI_D1_P**	I	These pins are DSI-D1+/- differential data signals
36	**HSSI_D1_N**	I	
37	**AGND1**	Power	The power ground
38	**HSSI_CLK_P**	I	These pins are DSI-CLK+/- differential clock signals
39	**HSSI_CLK_N**	**I**	
40	**AGND2**	Power	The power ground
41	**HSSI_D0_P**	I/O	These pins are DSI-D0+/- differential data signals
42	**HSSI_D0_N**	I/O	
43	**AGND3**	Power	The power ground
44	**C11P**	-	Capacitor connection pins for the step-up circuit which generate AVDD.
45	**C11N**	-	
46	**C12P**	-	
47	**C12N**	-	
48	**AVDD**	Power	Driver IC internal power
49	**C31P**	-	Capacitor connection pins for the step-up circuit which generate VCL.
50	**C31N**	-	
51	**C32P**	-	
52	**C32N**	-	
53	**C41P**	-	Capacitor connection pins for the step-up circuit which generate VGH.
54	**C41N**	-	
55	**C51N**	-	Capacitor connection pins for the step-up circuit which generate VGL.
56	**C51P**	-	
57	**VGH**	Power	Driver IC internal power

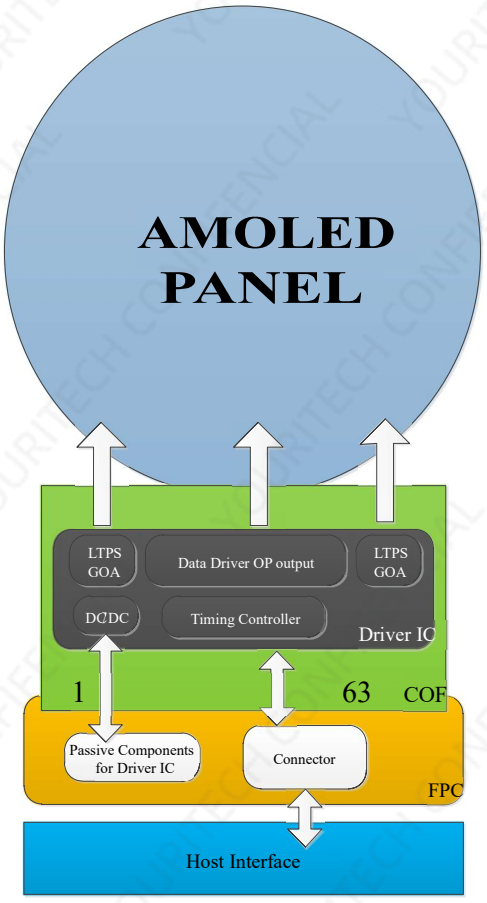
58	**VGHR**	Power	Driver IC internal power
59	**Dummy**	-	NC
60	**VGLR**	Power	Driver IC internal power
61	**VGL**	Power	Driver IC internal power
62	**AGND4**	Power	The power ground
63	**MTP_PWR**	Power	Power supply for OTP. Leave the pin to open when not in use.
64	**FOG**	-	Test pin
65	**FOG/FOF**	-	Test pin
66	**FOF**	-	Test pin
67	**ELVDD3**	Power	AMOLED power Positive
68	**ELVDD4**	Power	AMOLED power Positive
69	**ELVSS3**	Power	AMOLED power Negative
70	**ELVSS4**	Power	AMOLED power Negative

5.2.2 TP FPC Bonding PAD Define

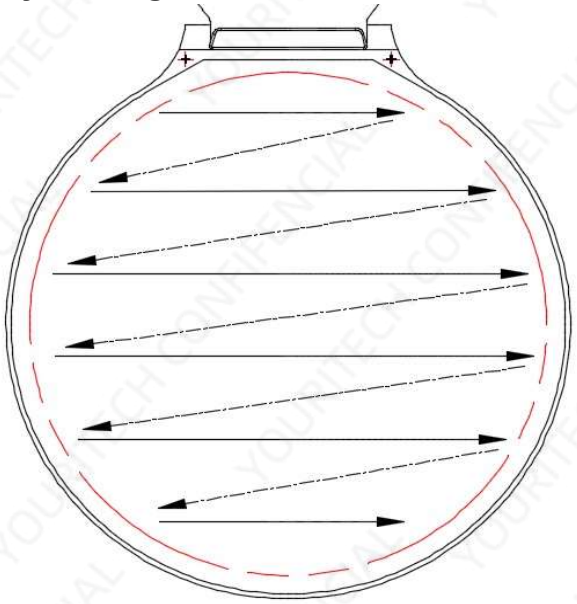
Pin No.	Symbol	I/O	Function Description	When not use
1	**FOG1**	-	FOG test pin	
2	**FOG2**	-	FOG test pin	
3	**GND1**	P	The power ground	
4	**GND2**	P	The power ground	
5	**Y07**	-	TP signal	
6	**Y06**	-	TP signal	
7	**GND3**	P	The power ground	
8	**X00**	-	TP signal	
9	**X01**	-	TP signal	
10	**X02**	-	TP signal	
11	**X03**	-	TP signal	
12	**X04**	-	TP signal	
13	**X05**	-	TP signal	
14	**GND4**	P	The power ground	
15	**Y00**	-	TP signal	
16	**Y01**	-	TP signal	
17	**Y02**	-	TP signal	
18	**Y03**	-	TP signal	
19	**Y04**	-	TP signal	
20	**Y05**	-	TP signal	

21	**GND5**	P	The power ground	
22	**X07**	-	TP signal	
23	**X06**	-	TP signal	
24	**GND6**	P	The power ground	
25	**GND7**	P	The power ground	
26	**FOG3**	-	FOG test pin	
27	**FOG4**	-	FOG test pin	

5.3 System Block Diagram

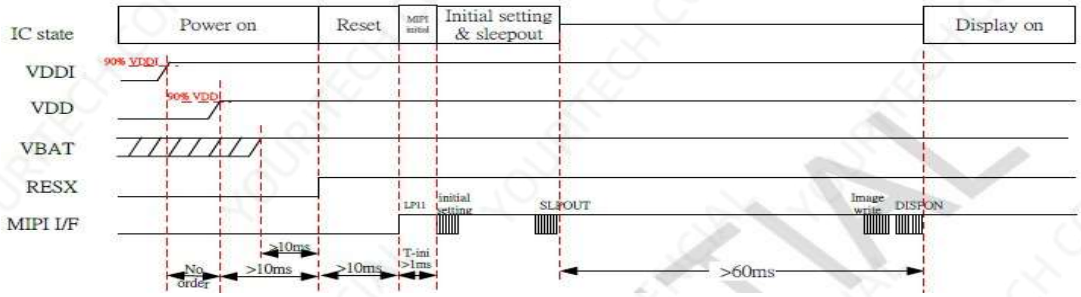


5.4 Graphic memory writing direction

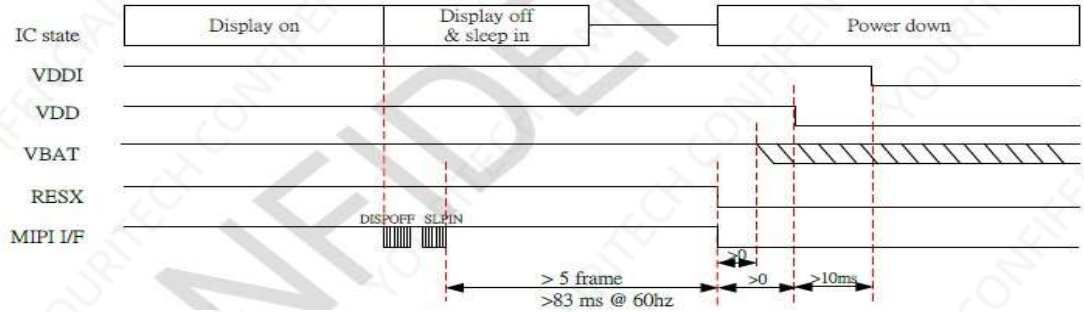


5.5 Recommended Operating Sequence

5.5.1 Power on sequence

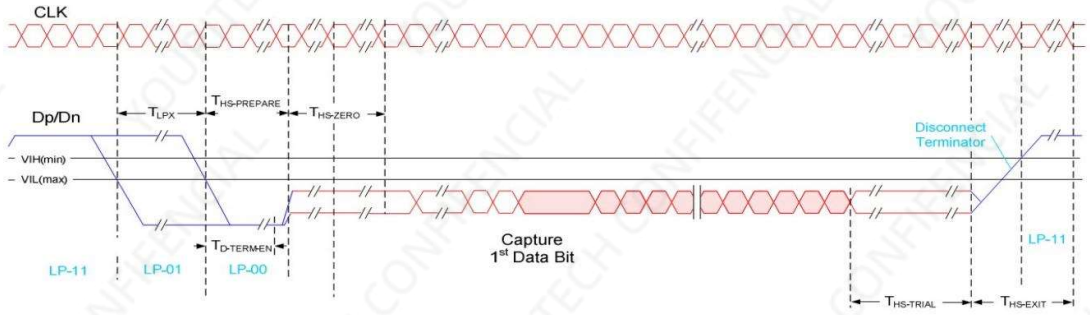


5.5.2 Power off sequence

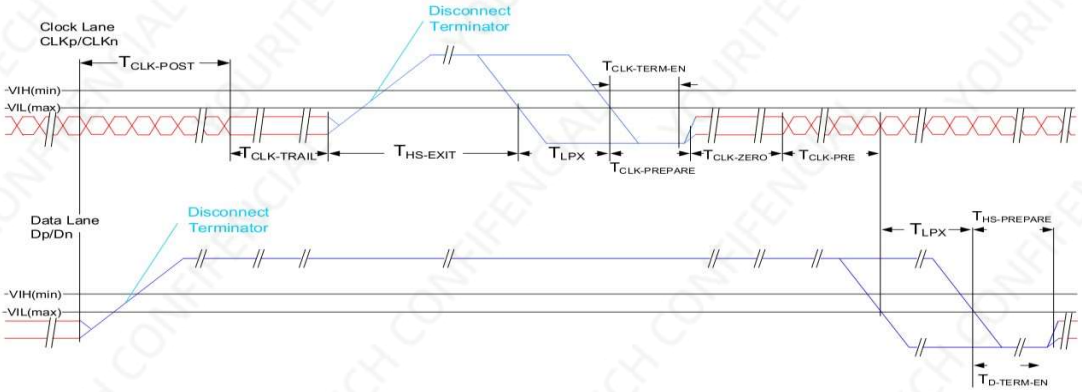


5.6 AC Characteristics（MIPI）

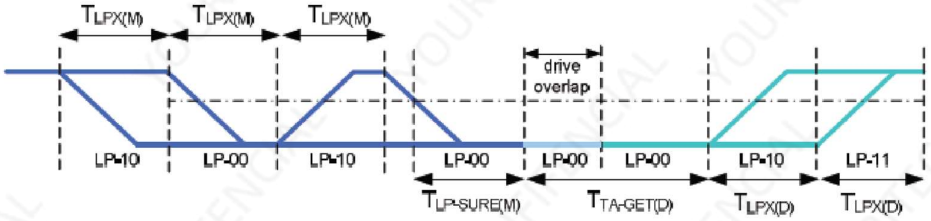
5.6.1 HS Data Transmission Burst



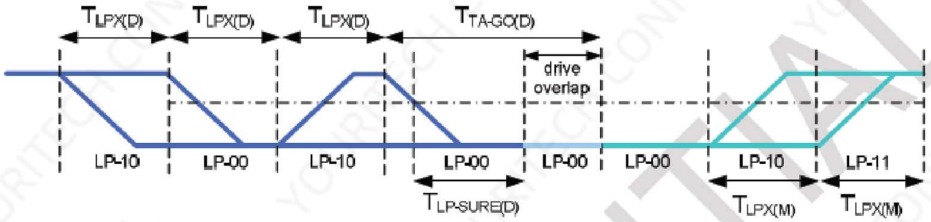
5.6.2 HS Clock Transmission



5.6.3 Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

5.6.4 Timing Parameters

Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	**300**			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	**$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.**	**145ns + 10*UI**			**ns**
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns

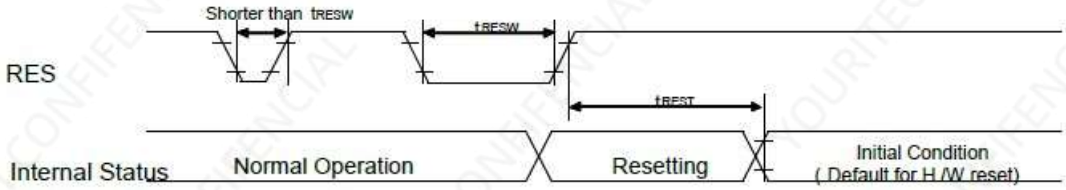
5.6.5 Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset.
When it is in the condition of reset, it will make the device recover the initial set.
However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.
The closed interval of Low can be shown as the following.

(Test condition: VDDIO=1.65V~3.3V, VSS=0V, T_A=-40℃~+85℃)

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	10	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

Table: Reset timing



Figure：Reset timing

6 Electro-Optical Specification

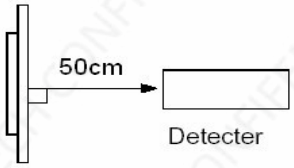
Test condition：VDDIO=1.8V , Vbat=3.7V ,Ta=25℃

Item		Symbol	Condition	Value			Unit	Note
				Min	Typ	Max		
Luminance		Bp	θ=0°	450	500	--	cd/m2	Note 1
Uniformity		△Bp	=0°	85		-	%	Note 2
Viewing Angle	Left	θ_L	Cr≥10	80	85	-	Deg.	Note 3
	Right	θ_R		80	85	-		
	Top	ψ_T		80	85	-		
	Bottom	ψ_B		80	85	-		
Contrast Ratio		CR	θ=0°	10000	100000	-	-	Note 4
Response Time		Tr+Tf	=0°	-	2	3	ms	Note 5
Color Coordinate of CIE1931	Red	X	θ=0° =0°	0.656	0.686	0.716	-	-
		Y		0.283	0.313	0.343		
	Green	X		0.195	0.235	0.275		
		Y		0.685	0.725	0.765		
	Blue	X		0.113	0.143	0.173		
		Y		0.014	0.044	0.074		
	White	X		0.28	0.30	0.32		
		Y		0.29	0.31	0.33		
NTSC Ratio		NTSC	CIE1931		100	-	%	-
Flicker		-	-	-	-	-30	dB	-
Gamma		-	-	1.9	2.2	2.5		Note 6
Crosstalk		ΔCT	-	-	-	1.1		Note 7

Note 1: Luminance measurement

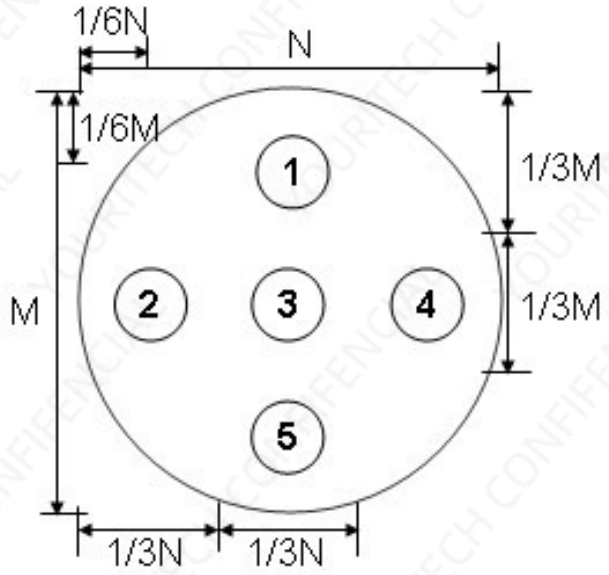
The test condition is at 25℃ and measured on the surface of OLED module.

- The data are measured after OLEDs are lighted on for more than 5 minutes and displays
- equipment CS2000 or similar equipments (Field of view:1deg,Distance:50cm)
- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.
- Measured value at the center point of panel must be after more than 5 minutes while backlight turning on.



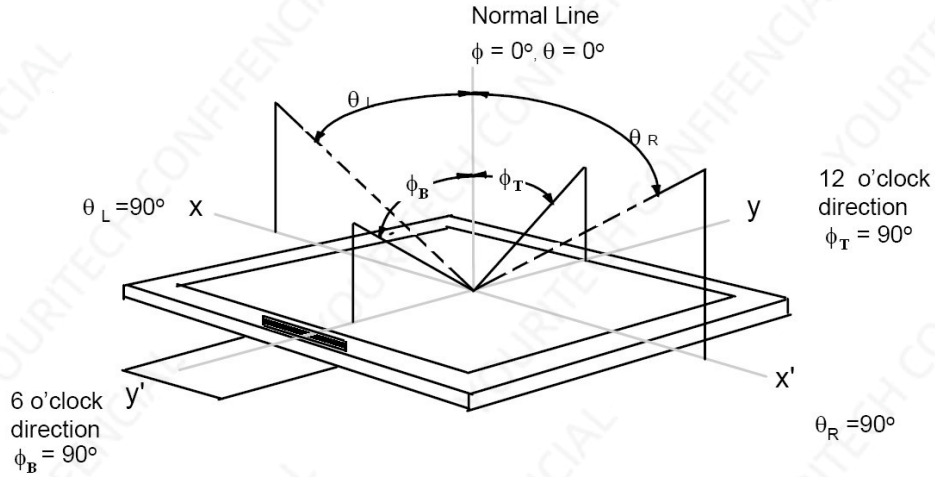
Note 2: Uniformity

- The test condition is at 25℃ and measured on the surface of display module.
- Measurement equipment: CS2000 or similar equipments.
- The luminance uniformity is calculated by using following formula:
- △ Bp = Bp (Min.) / Bp (Max.)×100 (%)
- Bp (Max.) = Maximum brightness in 5 measured spots • Bp (Min.) = Minimum brightness in 5 measured spots.



Note 3: **The definition of Viewing Angle**

Refer to the graph below marked by *θ* and *Φ*

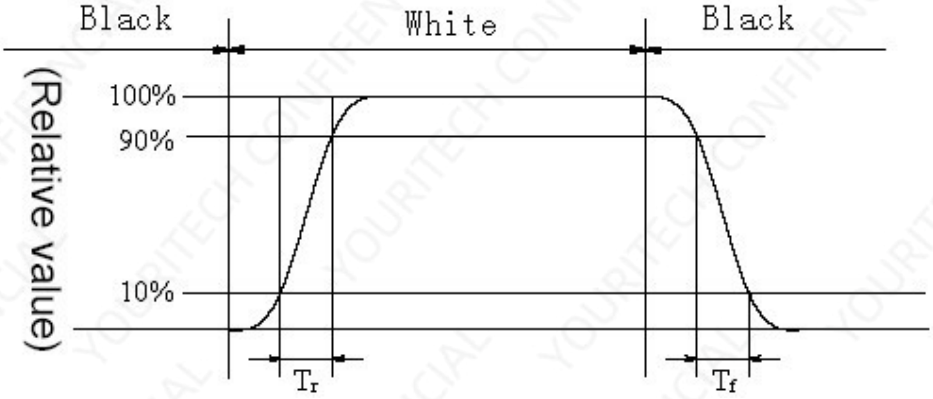


Note 4: **The definition of Contrast Ratio**:

$$\text{Contrast Ratio (CR)} = \frac{\text{Luminance When AMOLED is at "White" state}}{\text{Luminance When AMOLED is at "Black" state}}$$

Note 5: **Definition of Response time.**

The output signals of photo detector are measured when the input signals are changed from “black” to “white” (Voltage falling time) and from “white” to “black” (Voltage rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



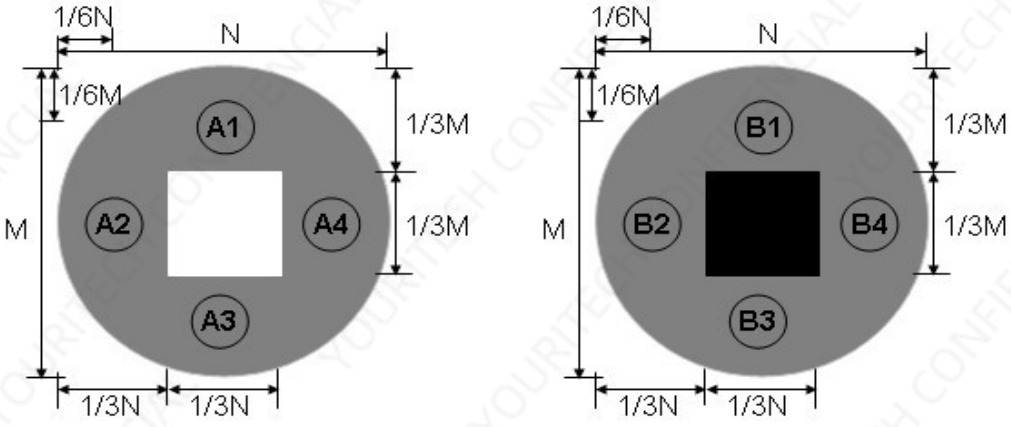
Note 6: Gamma curve

The whole curve’s tolerance must control within +/-0.3, test the gray scale below:
8, 16, 25, 33, 41, 49, 58, 66, 74, 82, 90, 99, 107, 115, 123, 132, 140, 148, 156, 165, 173, 181, 189, 197,206, 214, 222, 230, 239, 255

Note 7: **Crosstalk**

There should be no visible cross-talk in normal direction of the display when the two “Cross-talk Test Patterns” below are loaded.

ΔBp (Max.) = Maximum value in ΔBp1~ΔBp4.
ΔBp (Min.) = Minimum value in ΔBp1~ΔBp4. ΔCT=
ΔBp (Max.)/ ΔBp(Min.).
ΔCT must be less than 1.10



Cross-talk Test Pattern

7 Reliability

7.1 Environmental Test

Item	Main spec	No. of failures / No. of examinations
High Temperature Operation	70℃/ 128hours	0/ 5
Low Temperature Operation	-20℃/ 128hours	0/ 5
High Temperature Storage	80℃/ 128hours	0/ 5
Low Temperature Storage	-30℃/ 128hours	0/ 5
High Temperature Humidity Operation	60℃/ 90%RH 128hours	0/ 5
Thermal Shock	-40℃~80℃ 0.5hr, 30 cycles	0/ 5

7.2 Electrical Test

Item(Display)	Main spec	Note
Air Discharge	±4kV , 150pF/330Ω （Module level）	5Points, Each 2times. No degradation of OLED performance after this test.
Contact Discharge	±4kV, 150pF/330Ω （Module level）	

7.3 Mechanical Test

Item	Main spec	Note
Drop Test	Drop the packing from 75cm height, 3 times for 6-faces, 3-edges and 1-corner	Package
Vibration-proof test	2g, f=10->55->10Hz apply in each of X, Y, and Z direction for 30 min	Package

8 Packing Specification

	包装作业规范 Packaging Operation Procedure	编 号：3MT-EN-POP 版 本： 01 页 数： 1 OF 1 发行日期：22-11-21

一、基本信息

客户：Common	)1
品名：1.43AMOLED显示屏总成	包装方式：真空包

二、作业规范

1、包装数量

☑ 吸塑盒，每盒25 pcs；真空袋，每包12 盒；纸箱，每箱2 包，每箱600PCS

☐ 其他

2、真空袋规格 单位：**MM**

☑ 455*515 ☐ 400*450 ☐ 120*160

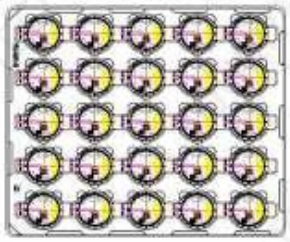
3、纸箱规格

☑ 415mm*320mm*250mm ☐ 270mm*270mm*350mm ☐ 290mm*265mm*125mm ☐ 300mm*300mm*250mm

4、标签

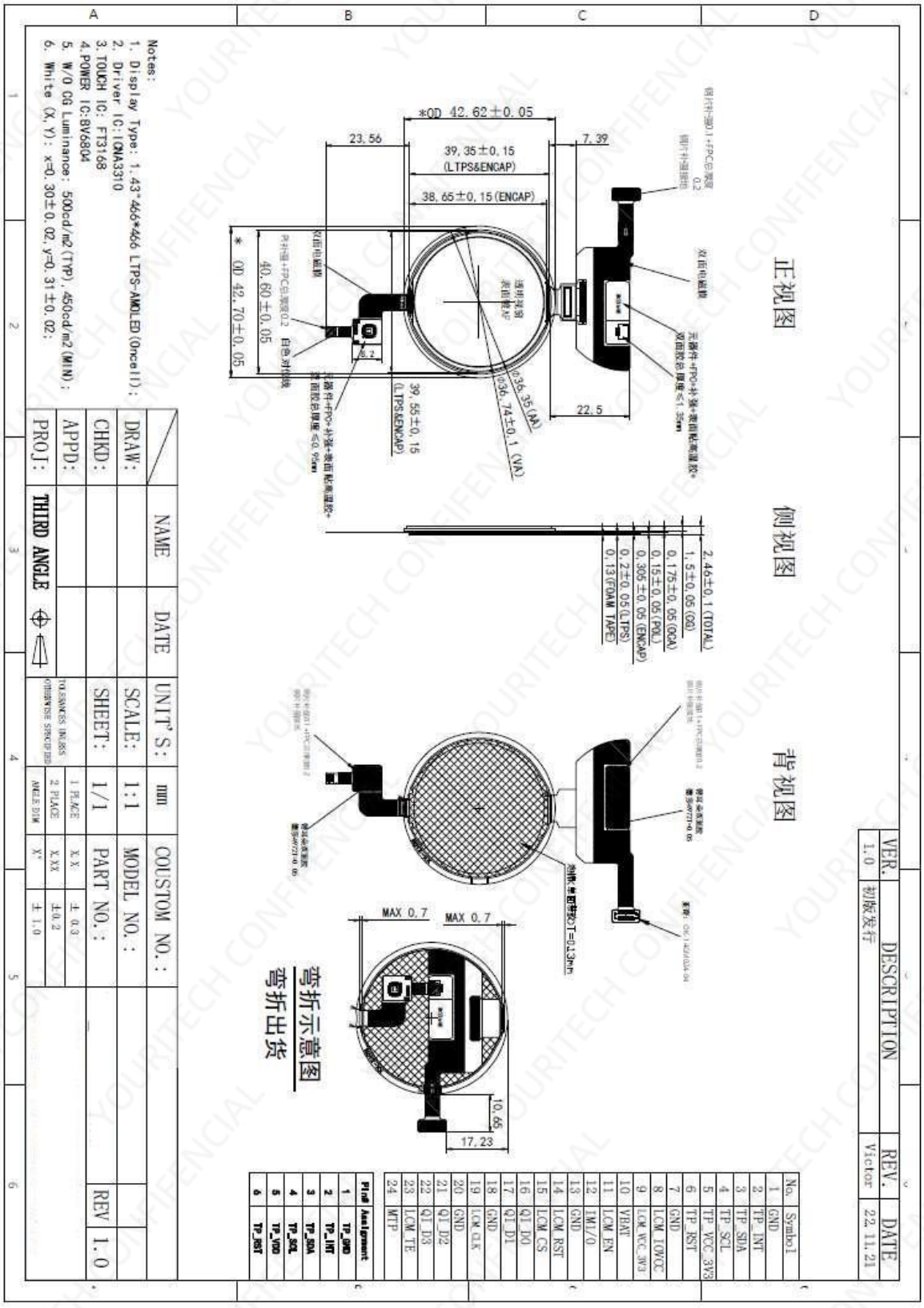
☑ 合格标签 ☑ RoHS标签 ☑ 月份标签 ☐ 产品标签

三、作业步骤

作业示意图	说明和注意事项
	1、按产品形状，盖板面向下摆放在吸塑盒定位形状槽内 2、每盘摆放25个 3、注意摆放方向一致 4、注意排线放入对应槽内，不可再弯折
 	1、12盘一扎，最上面放一个空盘 2、用胶带十字交叉固定好 3、贴上RoHS、合格、月份标签 4、按每袋一扎，放入真空袋，真空包装
 	1、每箱两包 2、在纸箱空隙放气泡袋防护 3、胶带固定好 4、注意纸箱不可有破损、脏污

编制/日期：Victor/22.11.21　　核准/日期：

9 Outline Dimension Drawing



10 Handling Precautions

1. When cleaning ITO pad, avoid using hard and abrasive material or corrosive solution
2. Keep module away from direct sunlight or fluorescent light, and keep it at room temperature and humidity
3. Strong impact & pressure on module and packing is prohibited
4. Following normal power on/off sequence is necessary for preventing abnormal display or permanent damage to display
5. Optimal contrast ratio under ideal voltage is AMOLED module's characteristic, hence it is recommended a voltage control function available
6. Image sticking may occur if an image displays for an extended period of time
7. When interfered by system's overall mechanical design, an abnormal display may occur
8. After considering emitting energy, you should plan your design to satisfy EMI standards.
9. Host side should place a surge-prevent circuit at power trace (ie: VCI, Vddi) to protect AMOLED module.