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Project No. 项目编号	ET016CR03-TT
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	**Standard LCD Module** **TFT：400*RGBx400Dots** **1.6”TFT LCD+CG**

客户确认Customer Approval	
项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	

PREPARED BY	CHECKED BY	APPROVED BY

1. Introduction

1.1 Scope of application

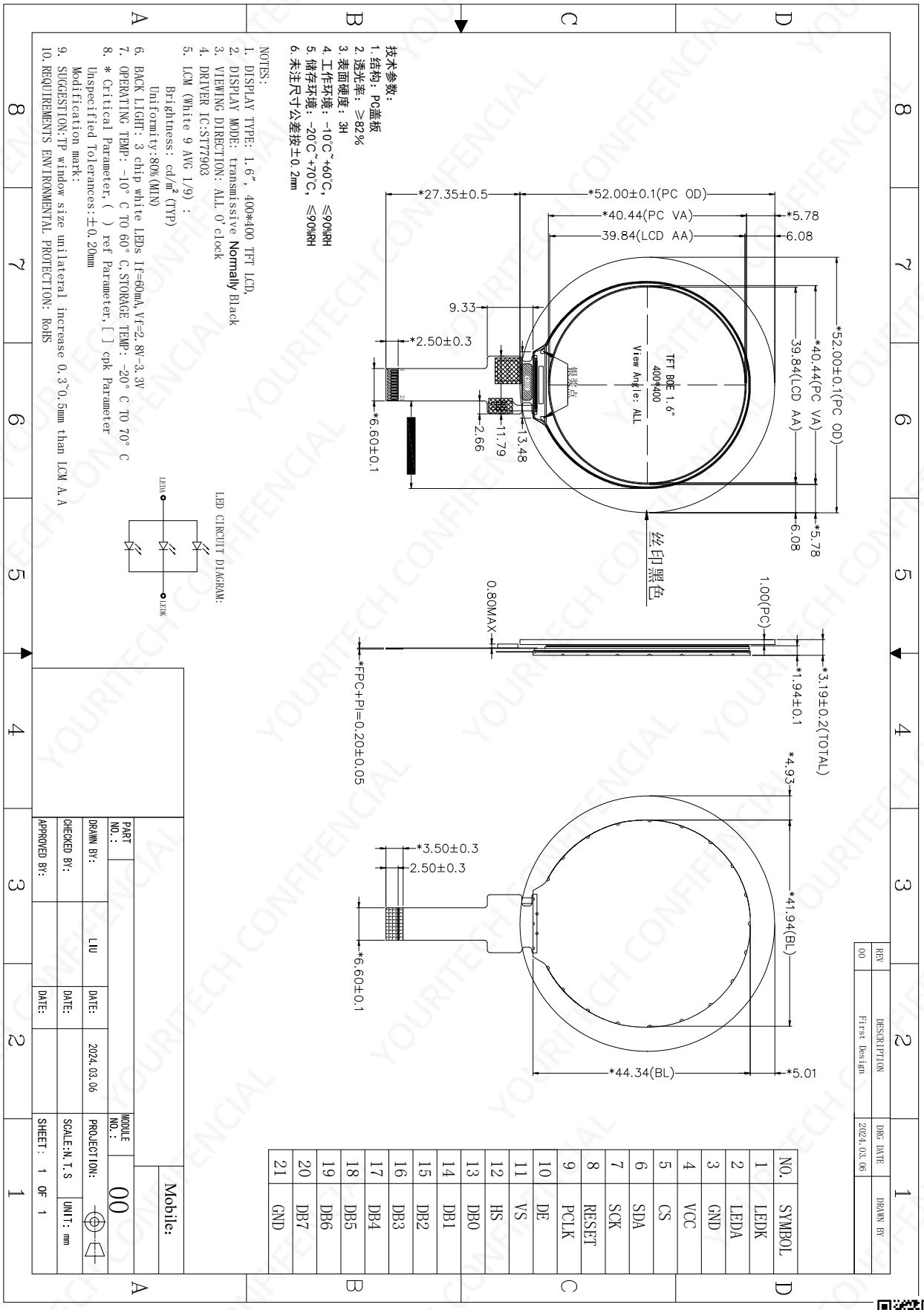
This specification applies to the LCD module that is supplied by YOURITECH Technology CO., LTD.
LCD specification: Dots 400xRGBx400.
As to basic specification of the driver IC, refer to the IC (ST77903) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL+CG;
IPS Type LCD
400 dot-segment and 400 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
8bit RGB interface

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	400*3RGB(H)X400(V)	Dots
Pixel arrangement	RGB Vertical stripe	--
Pixel Pitch (W*H)	0.0996(H) x0.0996 (V)	mm
Active area	39.84(H) x39.84(V)	mm
Viewing direction	IPS Type LCD	mm
TFT Driver IC	ST77903	--
TFT interface	8bit RGB interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	41.94(W)x 44.34(H) x 1.94(T)	mm
LCM+CG Size(W*H*T)	52.00(W)x 52.00(H) x 3.19(T)	mm
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--


技术参数：
1.结构：PC盖板
2.透光率：≥82%
3.表面硬度：3H
4.工作环境：-10℃~+60℃，≤90%RH
5.储存环境：-20℃~+70℃，≤90%RH
6.未注尺寸公差按±0.2mm
NOTES:
1. DISPLAY TYPE: 1.6", 400*400 TFT LCD,
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL O'clock
4. DRIVER IC:ST77903
5. LCM (White 9 AVG 1/9) :
Brightness: cd/㎡ (TYP)
Uniformity:80%(MIN)
6. BACK LIGHT: 3 chip white LEDs If=60mA,Vf=2.8V~3.3V
7. OPERATING TEMP: -10° C TO 60° C,STORAGE TEMP: -20° C TO 70° C
8. * Critical Parameter, ( ) ref Parameter, [ ] cpk Parameter
Unspecified Tolerances:±0.20mm
Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS
LED CIRCUIT DIAGRAM:
LEDA
LEDK
*27.35±0.5
*52.00±0.1(PC OD)
*40.44(PC VA)
39.84(LCD AA)
*5.78
6.08
9.33
*2.50±0.3
TFT BOE 1.6"
400*400
View Angle: ALL
银浆点
*52.00±0.1(PC OD)
*40.44(PC VA)
39.84(LCD AA)
*5.78
6.08
*6.60±0.1
11.79
2.66
13.48
丝印黑色
0.80MAX
1.00(PC)
*FPC+PI=0.20±0.05
*1.94±0.1
*3.19±0.2(TOTAL)
*4.93
*3.50±0.3
2.50±0.3
*41.94(BL)
*6.60±0.1
*44.34(BL)
*5.01
REV
DESCRIPTION
DRC DATE
DRAWN BY
00
First Design
2024.03.06
NO.
SYMBOL
1 LEDK
2 LEDA
3 GND
4 VCC
5 CS
6 SDA
7 SCK
8 RESET
9 PCLK
10 DE
11 VS
12 HS
13 DB0
14 DB1
15 DB2
16 DB3
17 DB4
18 DB5
19 DB6
20 DB7
21 GND
PART NO.:
DRAWN BY:
LIU
DATE:
2024.03.06
MODULE NO.:
00
CHECKED BY:
DATE:
PROJECTION:
APPROVED BY:
DATE:
SCALE:N.T.S
UNIT: mm
SHEET: 1 OF 1
Mobile:

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
CG Operating Temperature & Humidity (20% ~ 90%RH)	T_{OPR}	-20	+70	°C
CG SStorage Temperature & Humidity (20% ~ 90%RH)	T_{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	I/O	--	--	--	V
Supply Voltage for(DC/DC)	VDD	2.5	2.8	3.3	V

4.2 Back-Light Unit Characeristics

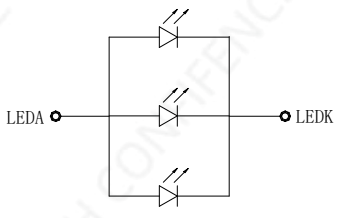
The back-light system is an edge-lighting type with 3 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	2.8	--	3.3	V	V
Forward current	I_F	--	60	--	mA	V
Luminance(With LCD)	Lv	--	TBD	--	cd/m^2	V
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	LCM Functional	Notes
1	LEDK	Power supply for backlight cathode input terminal.	
2	LEDA	Power supply for backlight anode input terminal.	
3	GND	Power Ground	
4	VCC	Power Supply For LCD.	
5	CS	Chip selection signal pin.	
6	SDA	Serial data input/output pin.	
7	SCK	Serial clock signal pin.	
8	RESET	Reset Signal input pin.	
9	PCLK	Dot clock signal for RGB interface operation.	
10	DE	Data enable signal for RGB interface operation.	
11	VS	Vertical (Frame) synchronizing input signal for RGB interface operation.	
12	HS	Horizontal (Line) synchronizing input signal for RGB interface operation.	
13	DB0	RGB interface data bus.	
14	DB1	RGB interface data bus.	
15	DB2	RGB interface data bus.	
16	DB3	RGB interface data bus.	
17	DB4	RGB interface data bus.	
18	DB5	RGB interface data bus.	
19	DB6	RGB interface data bus.	
20	DB7	RGB interface data bus.	
21	GND	Power Ground	

6.Power ON/OFF Sequence

VDDI and VCI can be applied in any order.

VCI and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.

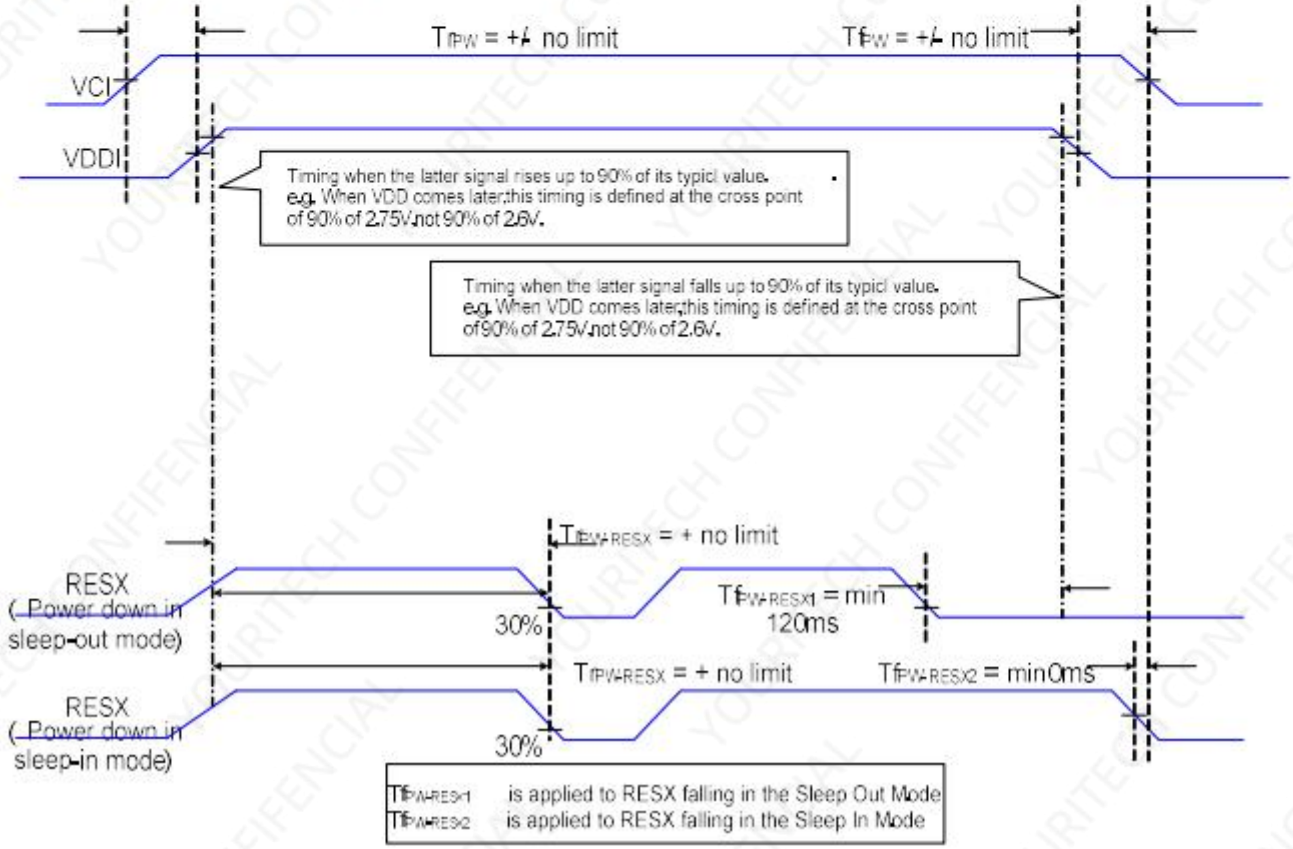
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.

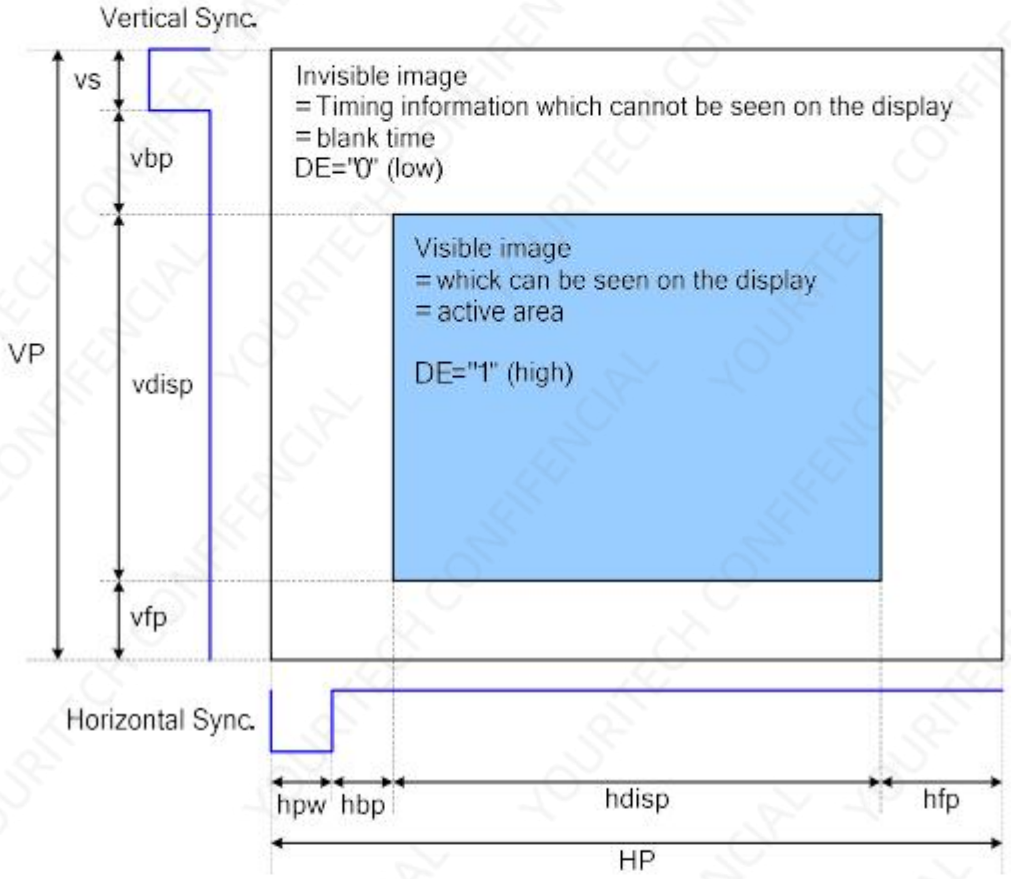


Figure 3 DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

6bit RGB interface:

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	TBD	TBD	TBD	Clock
Horizontal Sync. Back Porch	hbp	TBD	TBD		Clock
Horizontal Sync. Front Porch	hfp	TBD	TBD	TBD	Clock
Vertical Sync. Width	vs	TBD	TBD	TBD	Line
Vertical Sync. Back Porch	vbp	TBD	TBD		Line
Vertical Sync. Front Porch	vfp	TBD	TBD	TBD	Line

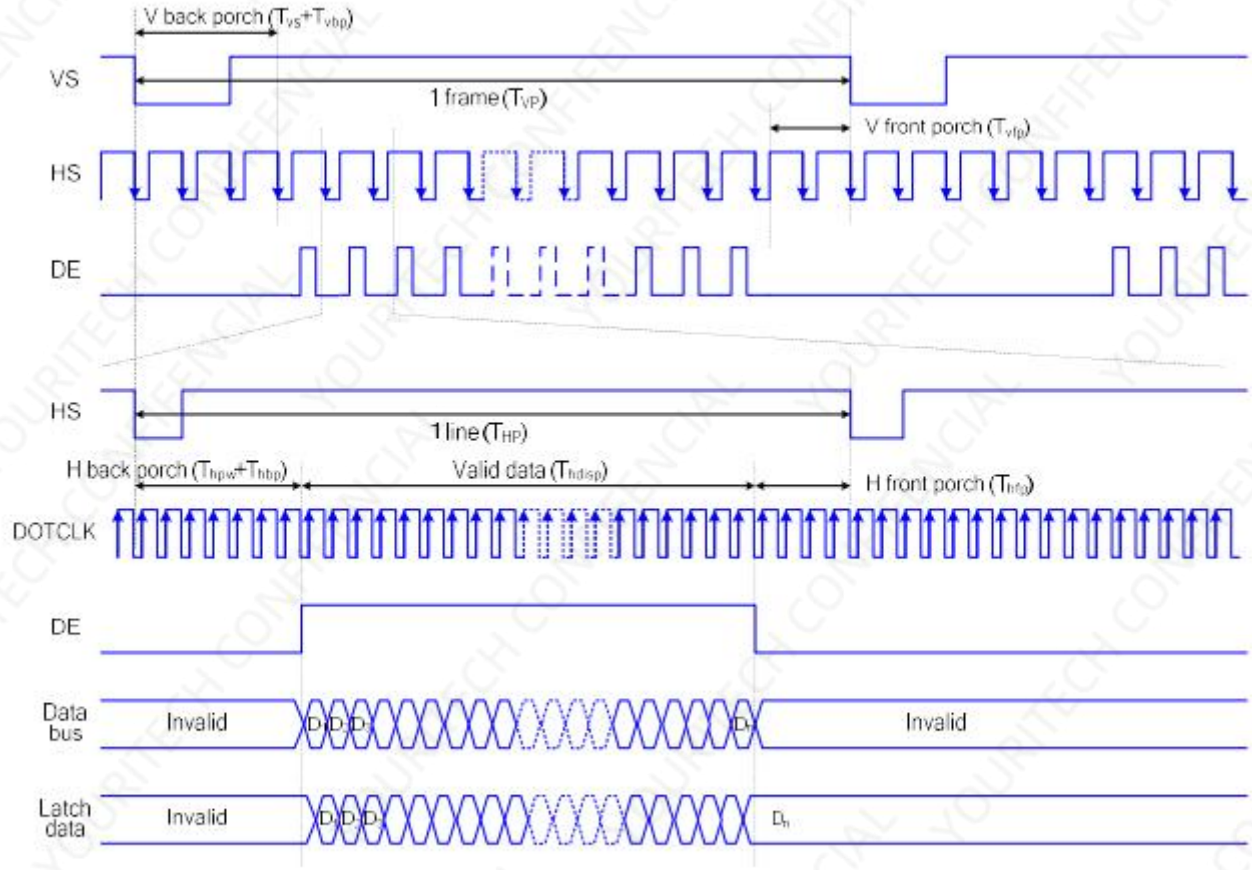
Note:

Typical value are related to the setting of dot clock is 17MHz and frame rate is 60Hz..

In without ram mode, hpw+hbp≧60

RGB Interface Timing

The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Figure 4 Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.

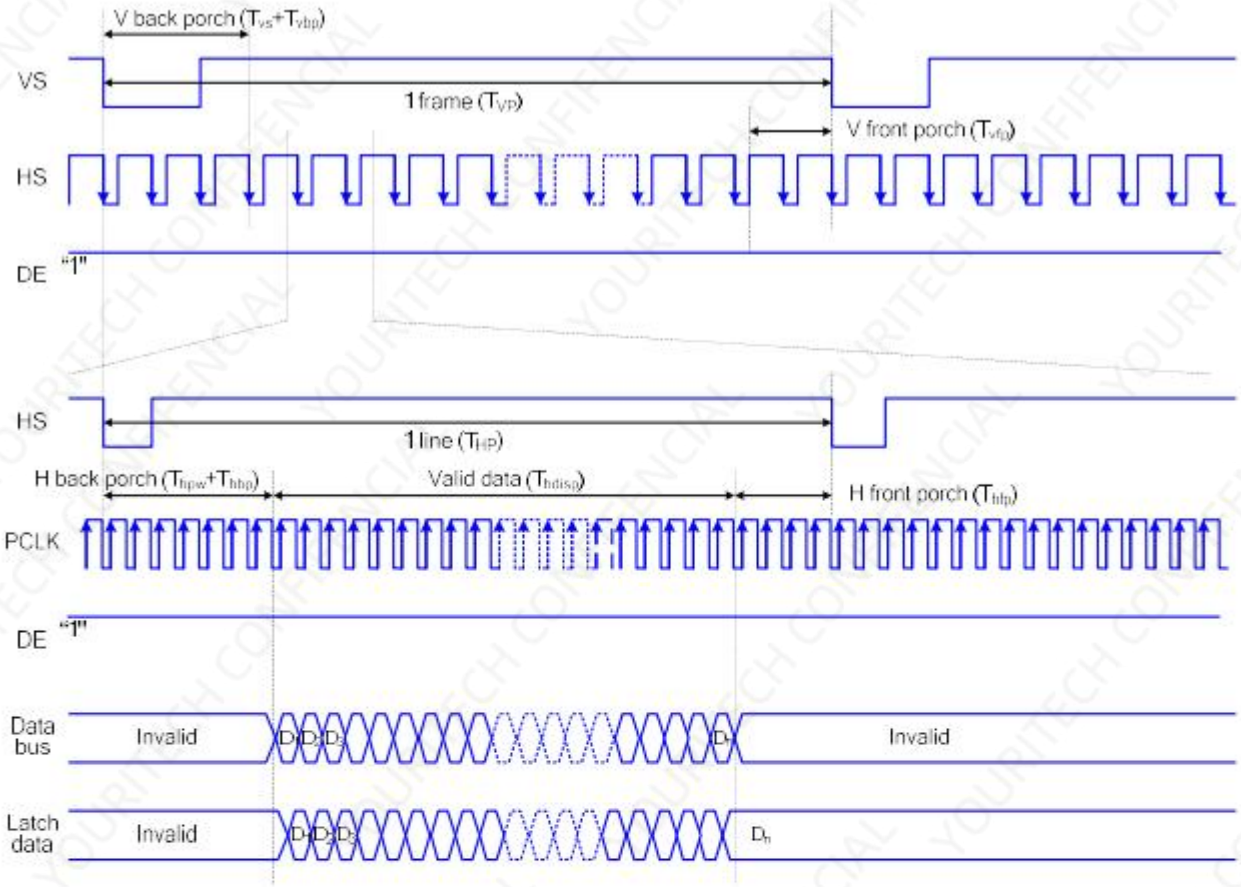


Figure 5 Timing chart of RGB interface HV mod

VSYNC, HSYNC, and DOTCLK signals must be supplied during a display operation period.

In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

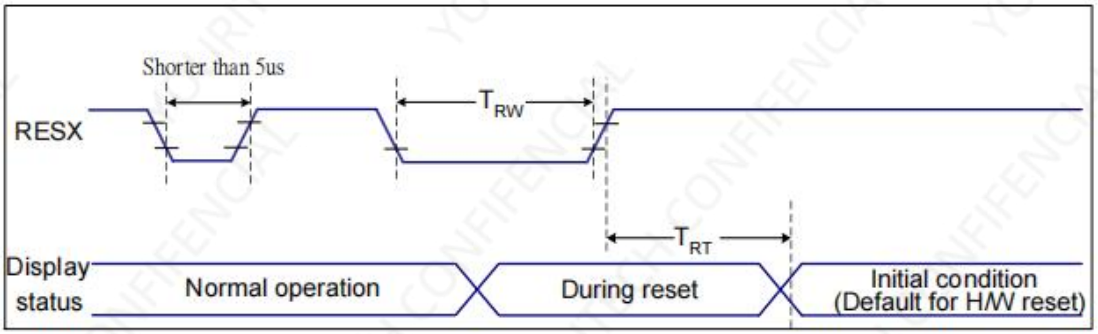
In RGB interface mode, each of RGB dots are transferred in synchronization with DOTCLK signals. In other words, one pixel data needs to take three DOTCLKs to transfer.

In RGB interface mode, the cycles of VSYNC, HSYNC, ENABLE, DOTCLK signals must be set correctly so that the data transfer is completed in units of pixels.

When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

Reset Timing



VDDI=1.8V, VCI=2.8V, AGND=DGND=AGNDR=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
			-	120 (Note 1, 6, 7)	ms

Notes:

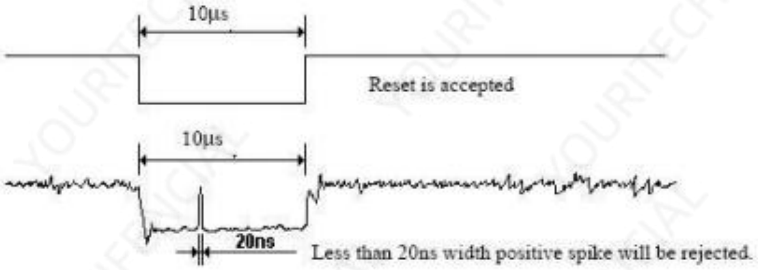
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

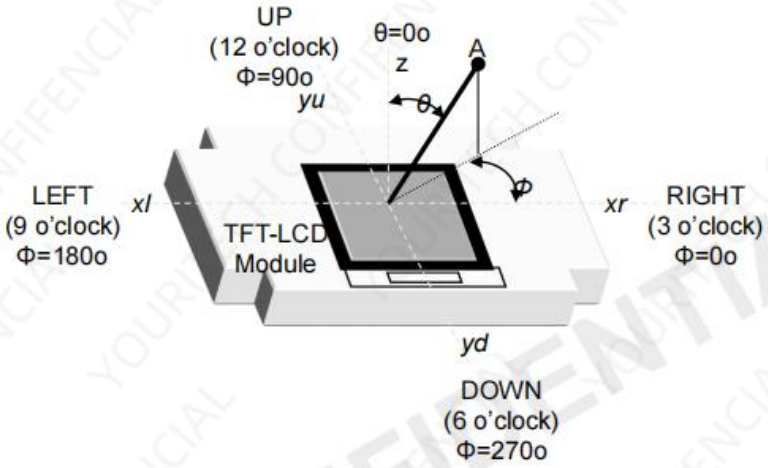
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	Note5
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Contrast ratio		CR	Θ = 0°	900	1200	-	-	HC+Clear @silicate BLU Note 5.2/5.3
Cell Transmittance		Tr	-	3.4	4.0	-	%	
Color Gamut	NTSC	CIE1931	Θ = 0°	60	65	-	%	CF@C Light Note 5.4
Chroma@CIE 1931	Red	(Rx,Ry)	Θ = 0°	Typ± 0.02	(0.660,0.323)	Typ± 0.02	-	
	Green	(Gx,Gy)	Θ = 0°		(0.280,0.571)		-	
	Blue	(Bx,By)	Θ = 0°		(0.134,0.132)		-	
	White	(Wx,Wy)	Θ = 0°		(0.294,0.335)		-	
Response Time		Tr+Tf	Ta= 25° C Θ = 0°	-	25	35	ms	Note 5.5

Note 1: Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 5).

<Figure 5. Viewing Angle Range Is Defined As Follows>



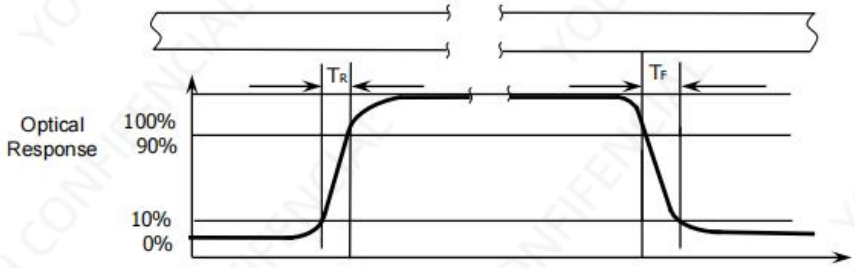
Note 2: Contrast measurements shall be made at viewing angle of Θ=0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 3 : The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

Note 4 : The electro-optical response time measurements shall be made as Figure 6 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

<Figure 6. Response Time Testing>



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	60°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~70℃（30min），10 cycles	

9. Packing Method----TBD

- END -