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Product Specifications

Customer	**Standard**
Description	1.69 ” E-PAPER DISPLAY
Model Name	ET017EPCR01-J
Date	2025/08/04
Revision	1.0

	Design Engineering		
	Approval	**Check**	**Design**

CONTENTS

1. Over View

ET017EPCR01-J is a reflective electrophoretic E Ink® Spectra 6 technology display modulebased on active matrix TFT substrate. It has 1.69” active area with 400 x 400 pixels . Thedisplay is capable to display images at Black/White/ Red/Yellow/Blue/Green depending onthe display controller and the associated waveform file it used.

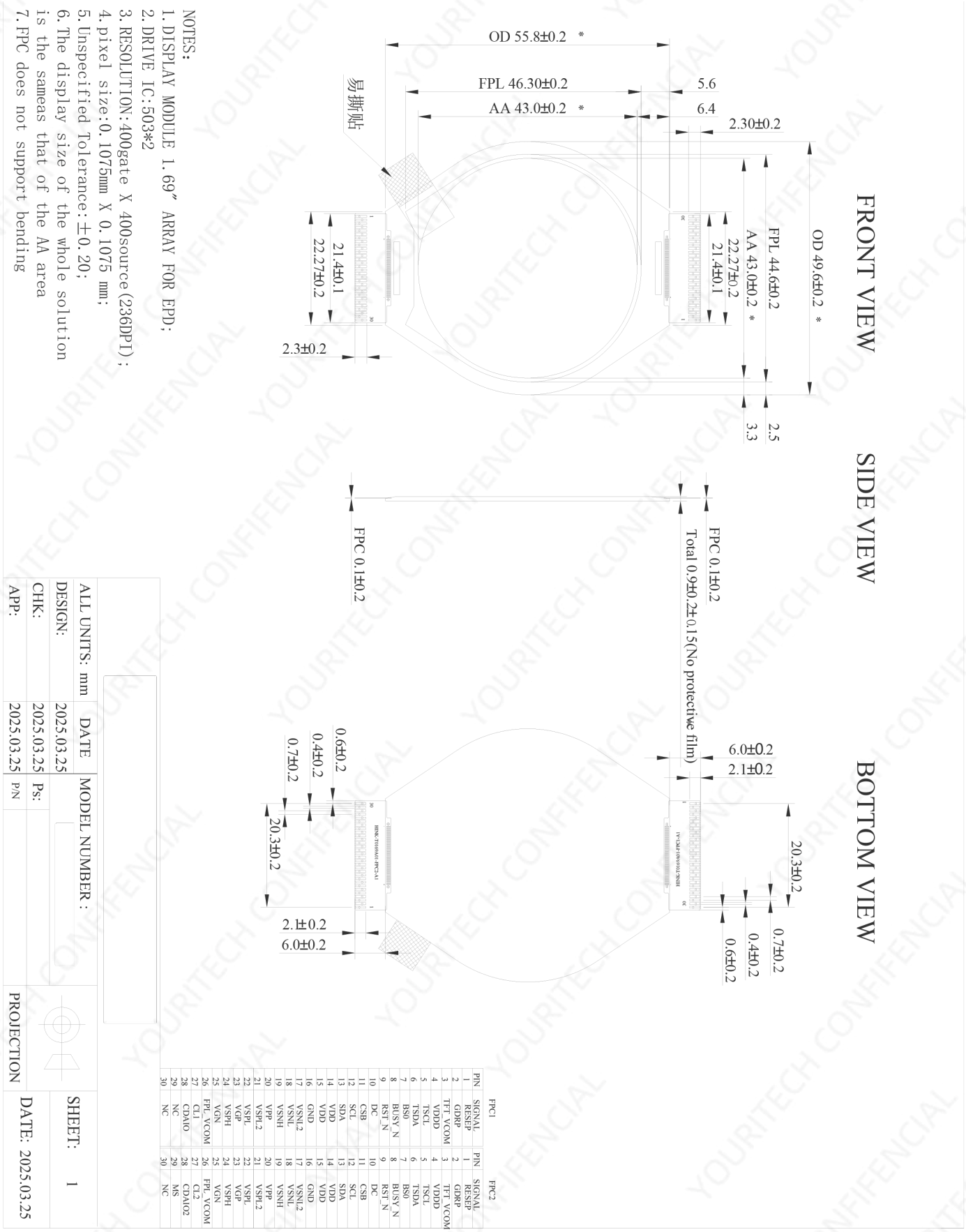
2.Features

- 400*400 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Low voltage detect for supply voltage
- High voltage ready detect for driving voltage
- Internal temperature sensor
- Waveform stored in On-chip OTP
- 10-byte OTP space for module identification
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- I2C signal master interface to read external temperature sensor/ built-in temperature sensor

3.Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	1.69	Inch	
Display Resolution	400(H)x400(V)	Pixel	Dpi:236
Active Area	43(H)x43(V)	mm	
Pixel Pitch	0.169x0.169	mm	
Pixel Configuration	Square		
Outline Dimension	55.8(H)x49.6(V)x0.95(D)	mm	
Weight	10±3	g	

4. Mechanical Drawing of EPD module



NOTES:
1. DISPLAY MODULE 1.69" ARRAY FOR EPD;
2. DRIVE IC:SS03*2
3. RESOLUTION:400gate X 400source(236DPI);
4. pixel size:0.1075mm X 0.1075 mm;
5. Unspecified Tolerance:±0.20;
6. The display size of the whole solution is the sameas that of the AA area
7. FPC does not support bending

FPC1		FPC2	
PIN	SIGNAL	PIN	SIGNAL
1	RESP	1	RESP
2	GDRP	2	GDRP
3	TFT_VCOM	3	TFT_VCOM
4	VDDD	4	VDDD
5	TSCL	5	TSCL
6	TSDA	6	TSDA
7	BS0	7	BS0
8	BUSY_N	8	BUSY_N
9	RST_N	9	RST_N
10	DC	10	DC
11	CSB	11	CSB
12	SCL	12	SCL
13	SDA	13	SDA
14	VDD	14	VDD
15	VDD	15	VDD
16	GND	16	GND
17	VSNL2	17	VSNL2
18	VSNL	18	VSNL
19	VSNH	19	VSNH
20	VPP	20	VPP
21	VSPL2	21	VSPL2
22	VSPL	22	VSPL
23	VGP	23	VGP
24	VSPH	24	VSPH
25	VGN	25	VGN
26	FPL_VCOM	26	FPL_VCOM
27	CL1	27	CL2
28	GDAIO	28	GDAIO2
29	NC	29	MS
30	NC	30	NC

ALL UNITS: mm	DATE	MODEL NUMBER :	
DESIGN:	2025.03.25		
CHK:	2025.03.25	Ps:	
APP:	2025.03.25	P/N	
PROJECTION		SHEET: 1	DATE: 2025.03.25

5. Input /Output Pin Assignment

Pin Assignment_**FPC1**			
Pin #	**Type**	**Single**	**Description**
1	I	RESEP	Current sense input for control loop for VGP Boost.
2	O	GDRP	N-MOS gate control for VGP Boost.
3	O	TFT_VCOM	a. VCOMDC. b. 0V.
4	P	VDDD	Digital Power input. (1.2v)
5	I/O	TSCL	I2C Interface to digital temperature sensor Clock pin
6	I/O	TSDA	I2C Interface to digital temperature sensor Data pin
7	I	BS0	Input interface setting. Select 3 wire/ 4 wire/ Quad SPI interface.(Default :H)
8	O	BUSY_N	IC busy flag. H: Host side can send command/data to driver. L: IC is busy, SD/VCOM is transforming
9	I	RST_N	Global reset pin. Low: Active. (Default=H) When RST_N becomes low, driver will reset. All register will reset to default value. Driver all function will disable. SD output and VCOM will base on previous condition. It may have two conditions: 0V or floating. The minimal width of RST_N=Low is 100μs.
10	I	DC	Command/Data input. (4-wire SPI) H: Data. L: Command. Connect to GND in 3-wire or Standard 4-wire mode.
11	I	CSB	Serial communication chip selects.
12	I	SCL	Serial communication clock input.
13	I/O (I)	SDA	Serial communication data input/output. (3-wire/4-wire SPI) (Serial communication data input.) (Standard 4-wire SPI)
14	I	VDD	Digital Power input.

15	I	VDD	Digital Power input.
16	P	GND	Ground
17	P	VSNL2	2nd Color Negative source driver voltage
18	P	VSNL	1st Color Negative source driver voltage
19	P	VSNH	Negative source driver voltage.
20	I	VPP	VPP for OTP programing. (7.25V)
21	P	VSPL2	2nd Color Positive source driver voltage.
22	P	VSPL	1st Color Positive source driver voltage.
23	I	VGP	Positive Gate voltage. (VGP)
24	P	VSPH	Positive source driver voltage.
25	I	VGN	Negative Gate voltage. (VGN)
26	O	FPL_VCOM	a. (VSPH+VCOMDC) or (VSNH+VCOMDC). b. VCOMDC. c. (VSPL+VCOMDC) or (VSNL+VCOMDC). d. Floating.
27	I/O	CL1	Connect to CL1 with a 2K resistor.
28	I/O	CDAIO1	Connect to CDAIO1 with a 2K resistor.
29		NC	No connection and do not connect with other NC pins
30		NC	No connection and do not connect with other NC pins

Pin Assignment_**FPC2**			
Pin #	**Type**	**Single**	**Description**
1	I	RESEP	Current sense input for control loop for VGP Boost.
2	O	GDRP	N-MOS gate control for VGP Boost.
3	O	TFT_VCOM	a. VCOMDC. b. 0V.
4	P	VDDD	Digital Power input. (1.2v)
5	I/O	TSCL	I2C Interface to digital temperature sensor Clock pin
6	I/O	TSDA	I2C Interface to digital temperature sensor Data pin
7	I	BS0	Input interface setting. Select 3 wire/ 4 wire/ Quad SPI interface.(Default :H)
8	O	BUSY_N	IC busy flag. H: Host side can send command/data to driver. L: IC is busy, SD/VCOM is transforming
9	I	RST_N	Global reset pin. Low: Active. (Default=H) When RST_N becomes low, driver will reset. All register will reset to default value. Driver all function will disable. SD output and VCOM will base on previous condition. It may have two conditions: 0V or floating. The minimal width of RST_N=Low is 100μs.
10	I	DC	Command/Data input. (4-wire SPI) H: Data. L: Command. Connect to GND in 3-wire or Standard 4-wire mode.
11	I	CSB	Serial communication chip selects.
12	I	SCL	Serial communication clock input.
13	I/O (I)	SDA	Serial communication data input/output. (3-wire/4-wire SPI) (Serial communication data input.) (Standard 4-wire SPI)
14	I	VDD	Digital Power input.
15	I		

16	P	GND	Ground
17	P	VSNL2	2nd Color Negative source driver voltage
18	P	VSNL	1st Color Negative source driver voltage
19	P	VSNH	Negative source driver voltage.
20	I	VPP	VPP for OTP programing. (7.25V)
21	P	VSPL2	2nd Color Positive source driver voltage.
22	P	VSPL	1st Color Positive source driver voltage.
23	I	VGP	Positive Gate voltage. (VGP)
24	P	VSPH	Positive source buffer output.
25	I	VGN	Negative Gate voltage. (VGN)
26	O	FPL_VCOM	a. (VSPH+VCOMDC) or (VSNH+VCOMDC). b. VCOMDC. c. (VSPL+VCOMDC) or (VSNL+VCOMDC). d. Floating
27	I/O	CL2	Connect to CL2with a 2K resistor.
28	I/O	CDAIO2	Connect to CDAIO2 with a 2K resistor.
29	I	MS	Cascade setting pin. Remark：Connect to the system GPIO H: Master chip. L: Slave chip
30		NC	No connection and do not connect with other NC pins

6.Reference Circuit

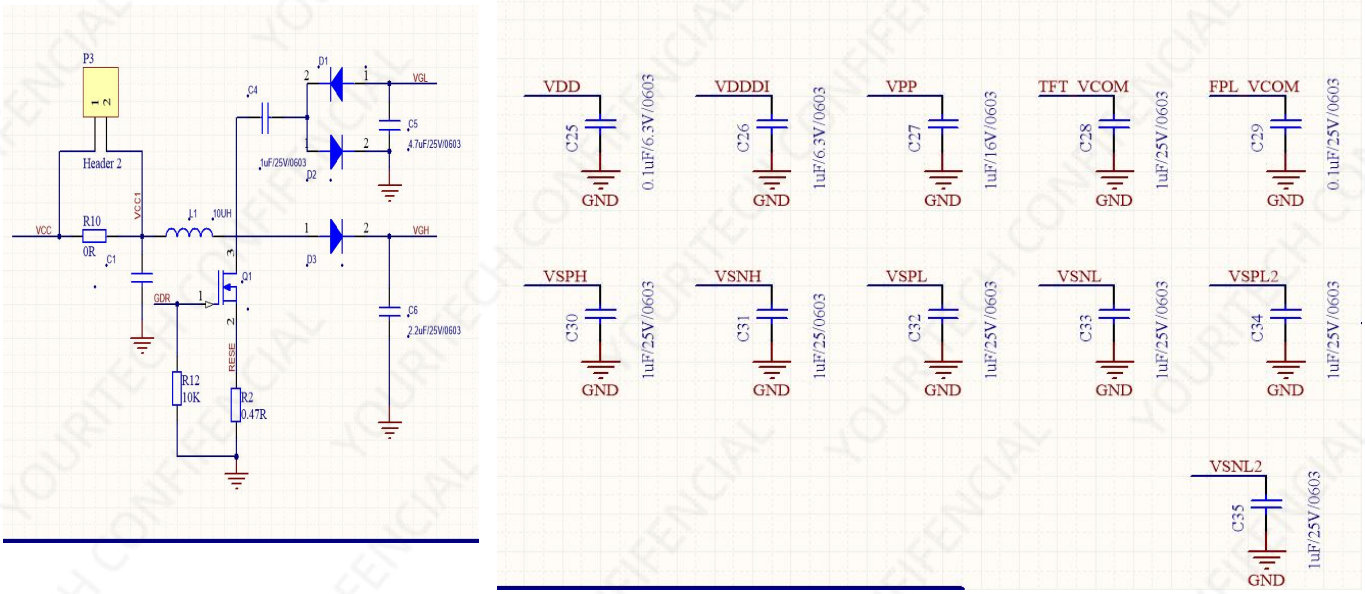
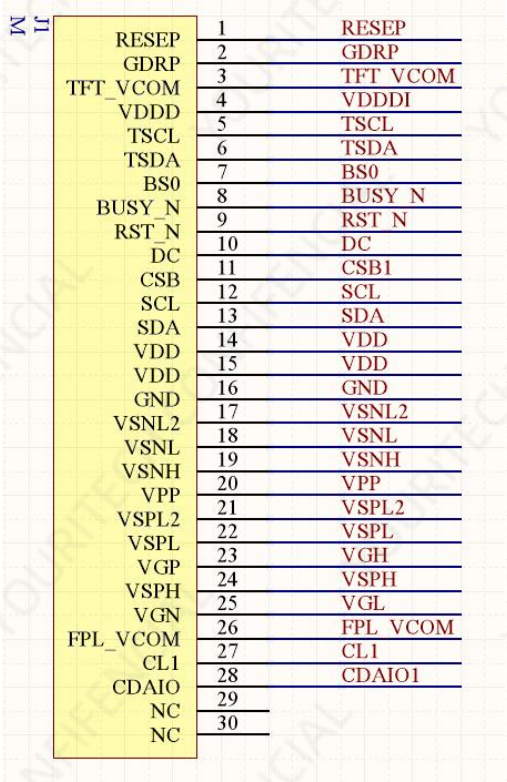
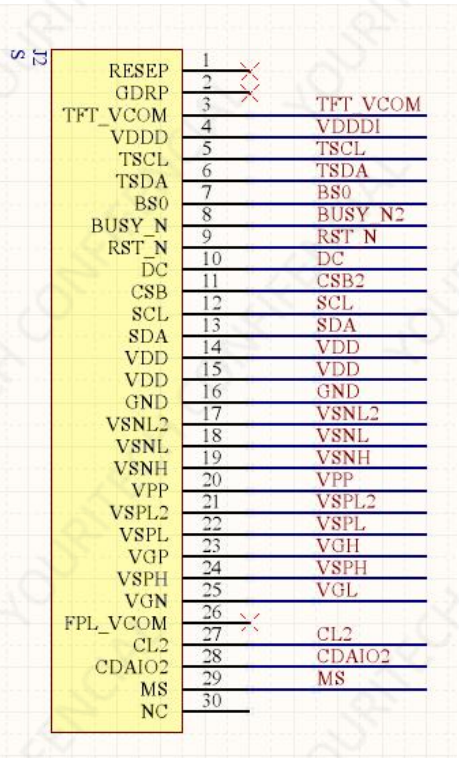


Figure. 6 - 1

FPC1



FPC2



Plugged sample circuit diagram

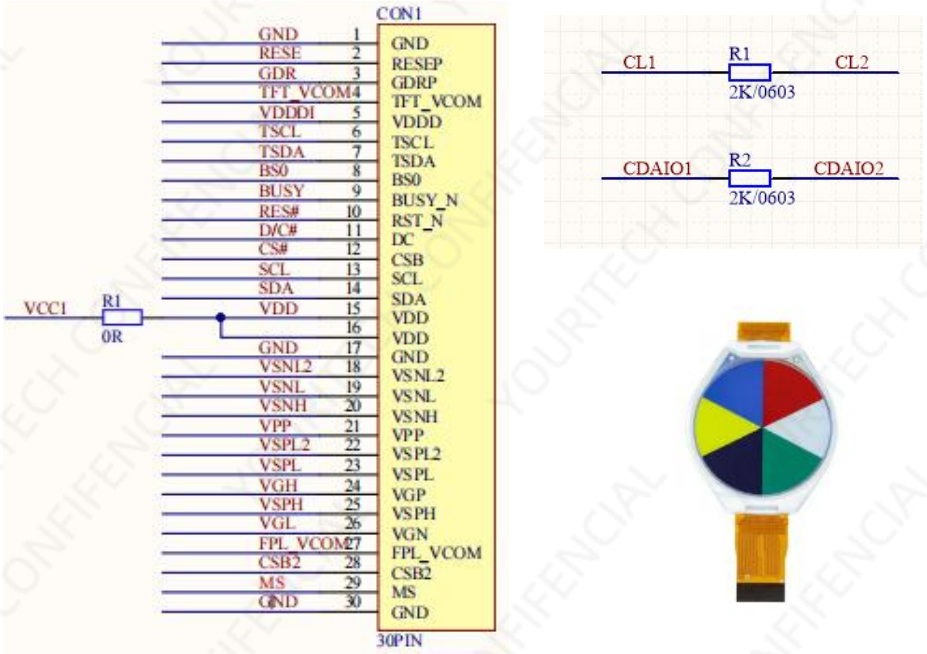


Figure. 6 - 2

Part Name	**Value/Type**	Value /requirement/Reference Part
C25，C29	0.1 uF	0603, X5R/X7R, Voltage Rating:16V
C4,C26,C27,C28,C30 C31,C32,C33,C34,C35	1uF	0603, X5R/X7R, Voltage Rating:25V
C6	2.2UF	0603, X5R/X7R, Voltage Rating:25V
C5	4.7UF	0603, X5R/X7R, Voltage Rating:25V
C1	10uF	0603, X5R/X7R, Voltage Rating:50V
R2	0.47 ohm	0603; 1% variation
D1-D3	Diode	MBR0530 1. Reverse DC voltage ≧ 30V 2. Forward current ≧ 500mA 3. Forward voltage ≦ 430mV
Q1	NMOS	Si1308EDL / Si1304BDL NTR4170NT1G1. Drain-source break voltage ≧ 30V 2. Gate-source threshold voltage ≦ 1.5V 3. Drain-source on-state resistance < 400mΩ
L1	10uH	NR4018T100M DCR<0.5ohm≥1.2A@25° C 10UI/NRH3010T100IMN
CON30Pin	0.5mm ZIF Socket	30Pins,0.5mm pitch

7. ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit	Humidity	Unit	Note
Logic Supply voltage	VCC,VDDIO	-0.5~6.0	V	45~70	%RH	Note 8-1
Operation temperature range	TOPR	0~50	℃	45~70	%RH	
Storage temperature range	TSTG	-25~60	℃	45~70	%RH	Note 8-2
Transportation temperature range	TTTG	-25~60	℃	45~70	%RH	Note 8-3
GND	Ground	-	-		-	Connect to Ground

Note 7 -1:

Maximum ratings are those values beyond which damages to the devicemay occur. VCC: Digital power, VDDIO:

IO power. Functional operation should berestricted to the limits in the Electric al Characteristics chapter.

Note 7 -2:

The display effect may be affected if the product is stored for more than10day s under the environment of 40-60 degree.

Note 7 -3:

TTTG is the transportation condition, the transport time is within 10 days for -25℃~0℃ or 40℃~60℃

Note 7 -4: The single pixel effect under the condition of above 40℃cannot be guaranteed

Note 7 - 5：

In order to ensure that NFC can complete the screen imaging, the timerequir ement is very short, so it is guaranteed that the imaging can be done below 2 0degrees Celsius, and the effect cannot be guaranteed

Note 7 -6：

At present, the power consumption standard and brush map support iPhone and Bluetooth transmission schemes, and other mobile phone systems are synchronized internally for internal verification.

8. DC Characteristics

Absolute maximum rating (GND=0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD, VDDIO, VDDA VPP,	Logic supply voltage	-0.3	-	+ 5.0	V
Vpp	OTP programming voltage	-0.3	-	-	V
VI	Digital input range	-	-	VDDIO+0.3	V
VGP-VGN	Supply range	-0.3	-	+42.0	V
Source					
VSPH	Analog supply voltage – Positive	-0.3	-	VGP	V
VSPL	Analog supply voltage – 1st color P	-0.3	-	VGP	V
VSPL2		-0.3	-	VGP	V
VSNH		VGN	-	+0.3	V
VSNL		VGN	-	+0.3	V
VNL2		VGN	-	+0.3	V
Gate					
VGP		-0.3	-	+22	V
VGN		-22	-	+0.3	V
TSTG		-55	-	+125	℃

Note: (1) If ICs are stressed beyond those listed above “ absolute maximum ratings ”,they may be permanently destroyed. These are stress ratings only, and functional operation of the device at theseor any other condition beyond those indicated under “ recommended operating conditions ” is notimplied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.1 Recommended operating conditions(GND=0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD，VDDIO, VDDA	Logic supply voltage	+2.3	-	+ 3.6	V
Vpp	OTP programming voltage	+7.25	-	+7.45	V
VI	Digital input range	0	-	VDDIO	V
VGP-VGN	Supply range	0	-	+40.0	V
Source					
VSPH	Analog supply voltage – Positive	0	-	VGP	V
VSPL	Analog supply voltage – 1st color P	0	-	VGP	V
VSPL2	Analog supply voltage – 2nd color P	0	-	VGP	V
VSNH	Analog supply voltage – Negative	-15	-	0	V
VSNL	Analog supply voltage – 1st color N	-15	-	0	V
VNL2	Analog supply voltage – 2nd color N	-15	-	0	V
Gate					
VGP	Analog supply voltage – positive	0	-	+20	V
VGN	Analog supply voltage – negative	-20	-	0	V
TOP	Operation temperature	-30	-	+85	℃

9. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃		140	mAs	-

MAs=update Average current ×update time

The Typical power consumption is measured using associated 25℃wavef orm withfollowing pattern:

10. Optical characteristics

10.1 Optical Measurement Conditions

Item	Symbol	Value	Unit	Note
Ambient Temperature	Ta	25±2	℃	Indoor testing
Ambient Humidity	Ha	50±5	%RH	-
Supply Voltage	VCC, VDDIO	3.0	V	-
illuminance	-	800~1300	Lux	

Note 10-1: Image is updated with above condition

10.2 Optical Measurement

WS: White state, BS: Black state, RS: Red state

Note 10-2: Luminance meter: Eye - One Spectrophotometer

Note 10-3:

We don't guarantee 3 years pixels display quality for humidity below 45%RH or above 70%RH; Suggest Updated once a day;

Symbol	Parameter	Conditions	Temperature	Min	Typ.	Max	Unit	Note
R	Reflectance	White	25° C	-	34	-	%	Note 7 -1
CR	Contrast Ratio	-	25° C	-	22	-	-	-
T_{update}	Update time	-	25° C	-	18	-	sec	-

Symbol	Parameter	Conditions	Temperature	L* Typ.	a* Typ.	b* Typ.	△E2000 Max.	Note
WS	White State L*/a*/b* value	White	25°C	66.5	-4	0	6	Note7-1
DS	Dark State L*/a*/b* value	Dark	25°C	12	7	-11	6	Note7-1
RS	Red State L*/a*/b* value	Red	25°C	26.5	41	30	6	Note7-1
YS	Yellow State L*/a*/b* value	Yellow	25°C	62	-11	65	6	Note 7-1
BS	Blue State L*/a*/b* value	Blue	25°C	34	3.5	-37	6	Note 7-1
GS	Green State L*/a*/b* value	Green	25°C	35	-22	15	8	Note 7-1

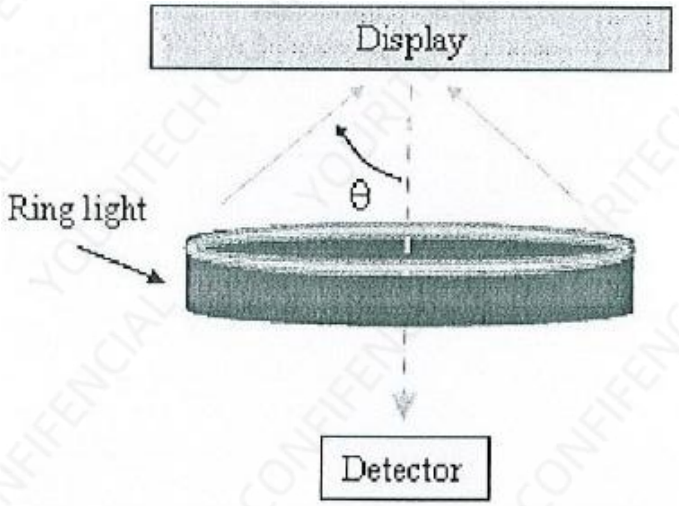
WS: White state, DS: Dark state, RS: Red state, YS: Yellow state, BS: Blue state, GS:Green state

Note 7-1 ： Luminance meter ： Eye - One Pro3 Spectrophotometer

10.3 Definition of contrast ratio

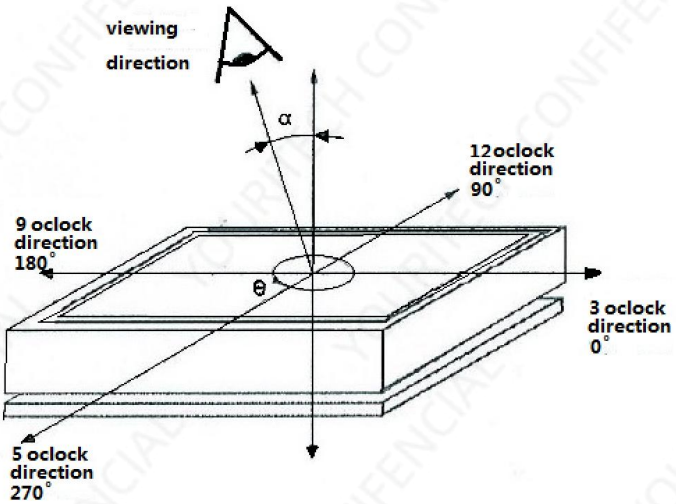
The contrast ratio (CR)
is the ratio between the reflectance in a full white area (Rl)
and the reflectance in a dark area (Rd)：R1: white reflectance
Rd: dark reflectance

CR = Rl/Rd



10.4 Reflection Ratio

The reflection ratio is expressed as:
R = Reflectance Factor white board x (L center / L white board)
L center is the luminance measured at center in a white area
(R=G =B=1). L whiteboard is the luminance of a standard white board. Bot
h are measured with equivalentillumination source. The viewing angle shal
l be no more than 2 degrees.



11. Handling Safety and Environmental Requirements

WARNING
The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.
Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	The data sheet contains final product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification
ROHS
REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

12. Reliability test

12.1 Reliability test items

	TEST	CONDITION	REMARK
1	High Temperature Storage	T = 60℃35% RH, 240Hrs Test in White pattern	ongoing
2	Low Temperature Storage	T = -25℃, 240Hrs Test in White pattern	ongoing
3	High Temperature Operation	T = 50℃30% RH, 240Hrs 150s interval between updates	ongoing
4	Low Temperature Operation	T = 0℃, 240Hrs 150s interval between updates	ongoing
5	High-Temperature, High-Humidity Operation	T = +40℃, RH = 90%, 240Hrs 150s interval between updates	ongoing
6	High Temperature, High-Humidity Storage	T = 60℃ 80% RH, 240Hrs Test in White pattern	ongoing
7	Heat Shock	-25℃(30 min) ~60℃(30 min) 50 cycle, 1Hr/cycle Test in White pattern	ongoing
8	Electrostatic Discharge	(Machine model) +/- 200V ; 0Ω, 200pF	ongoing

Actual EMC level to be measured on customer application.

Note1： Stay white pattern for storage and non-operation test.

Note2： Power off duration time is 30s

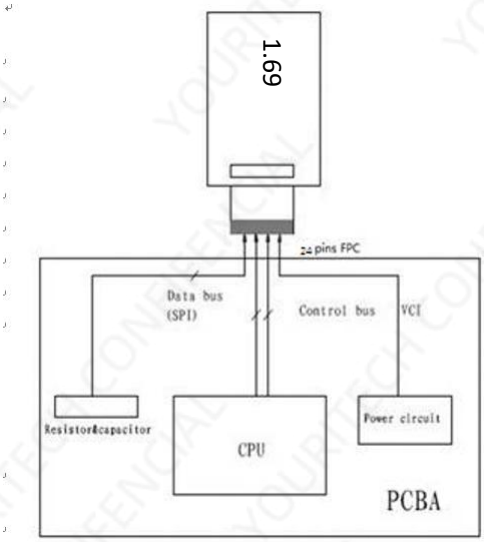
Note3： Continue testing after 2 hours at 20C~25C℃

Note4： Reliability verification of new products is ongoing, and this reliability condition is not considered as a final reliability result

12.2 Product life time

The EPD Module is designed for a 2-year life-time with 25 ℃/60%RH operation assumption. Reliability estimation testing with accelerated life-time theory would be demonstrated to provide confidence of EPD lifetime.

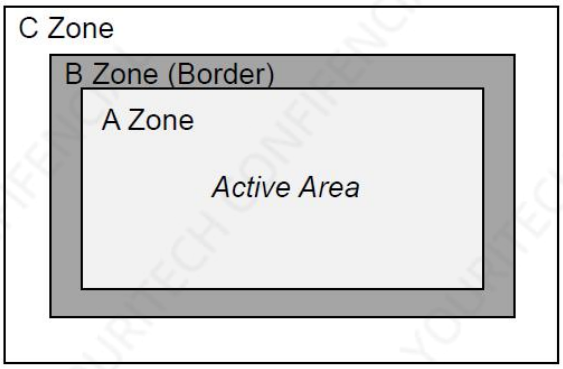
13. Block Diagram



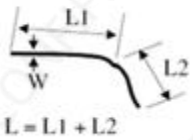
14. Shipment inspection specification

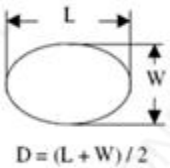
14.1 Zone Definition

A Zone: Active Area
B Zone: Border Area
C Zone:
From B Zone edge to panel edge

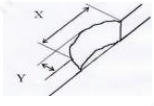
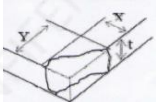


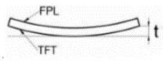
14.2 Line/Spot defect size





14.3 Point and line standard

Shipment Inspection Standard						
Equipment：Electrical test fixture, Point gauge						
Outline dimension	55.8 (H) x 49.6 (V) x 0.95(D)	**Unit：** ㎜	**Part-A**	Active area	**Part-B**	Border area
Environment	**Temperature**	**Humidity**	**illuminance**	**Distance**	**Time**	**Angle**
	19℃～25℃	50±5%RH	800~1300Lux	300 ㎜	35Sec	45°
Defect type	**Inspection method**	**Standard**		**Part-A**		**Part-B**
Spot	Electric Display	D≤0.25 ㎜		Ignore		Ignore
		0.25 ㎜＜D≤0.4 ㎜		N≤4		Ignore
		D＞0.4 ㎜		Not Allow		Ignore
Display malfunction	Electric Display	Not Allow		Not Allow		Ignore
Display error	Electric Display	Not Allow		Not Allow		Ignore
Scratch or line defect(include dirt)	Visual/Film card	L≤2 ㎜,W≤0.2mm		Ignore		Ignore
		2.0mm＜L≤5/0mm,0.2＜W≤0.3mm		N≤2		Ignore
		L＞5mm，W＞03mm		Not Allow		Ignore
PS Bubble	Visual/Film card	D≤0.2mm		Ignore		Ignore
		0.2mm≤D≤0.3mm，DS＞10mm		N≤3		Ignore
		D＞0.3 mm		Not Allow		Ignore
Corner /Edge chipping	Visual/Film card	Back edge breaking: length X≤6mm, width, Y≤0.1mm, negligible, not allowed Xu Intensive; 0.1mm＜Y≤0.4mm，N≤5；0.4＜Y≤0.6mm，N≤5， No cracks, non-acute angles and no impact on the electrode line Front edge: length X≤6mm, width, Y≤0.1mm, negligible, not allowed Xu Intensive; 0.1mm＜Y≤0.2mm，N≤5；0.2＜Y≤0.3mm，N≤5， No cracks, non-acute angles and does not affect the electrode line; Chipping angle: length X≤1mm, width Y≤1mm no cracks, non-acute angles and no impact on electricity Only 1 is allowed on each side of the pole line.				
		 				

TFT warping	T≤2mm 
Remark	1.Cannot be defect & failure cause by appearance defect;
	2.Cannot be larger size cause by appearance defect;
	L=long W=wide D=point size N=Defects NO
Mura	Refer to limit samples defined by E-INK