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MODEL NO : ET018QC01-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-07-05

□Preliminary Specification

■Final Product Specification

Customer :_____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 128xRGBx160
As to basic specification of the driver IC, refer to the IC (Sitronix:ST7735S) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;
12 O'clock Type LCD
128 dot-segment and 160 dot-common outputs;
65K Color can be selected by software;
White LED back light;
8lane MCU interface

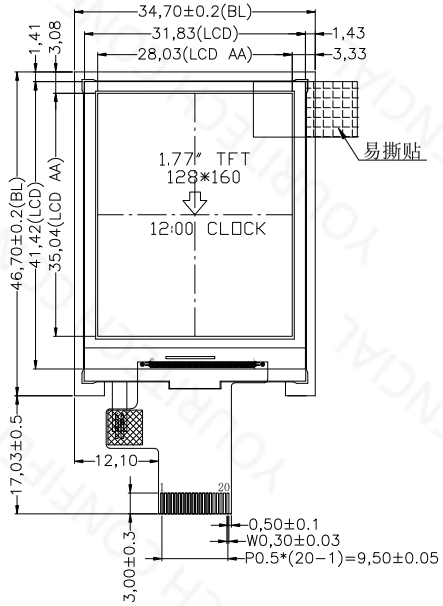
1.3 Applications:

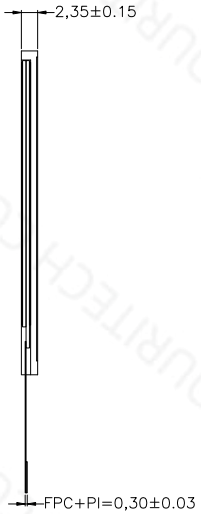
*

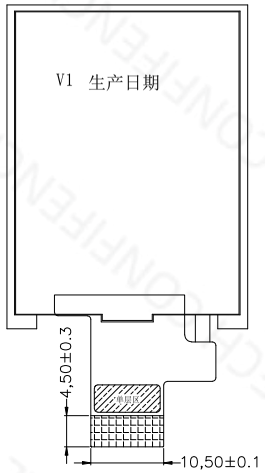
2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally White	--
Drive element	TFT active matrix	--
Number of pixels	128*3RGB(H)X160 (V)	Dots
Pixel arrangement	RGB stripe	--
Pixel Pitch (H*V)	0.219(H) x0.219 (V)	mm
Active area	28.03(H) x 35.04(V)	mm
Module Size(W*H*T)	34.70(W)x46.70(H)x2.35(T)	mm
Viewing direction	12 O'CLOCK	
TFT Driver IC	ST7735S	-
TFT interface	8lane MCU Interface	-
Approx. Weight	TBD	g
Touch structure		
Touch Driver IC		-
Touch Interface		

REV	DESCRIPTION	DRG DATE	DRAWN BY
	First Desing	2022.01.15	

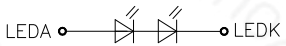






展开出货

PIN	DESCRIPTION
1	BL_K
2	BL_A
3	GND
4	VDD(2.8V)
5	VDD(2.8V)
6	NC
7	/CS
8	/RSTB
9	RS
10	WRB
11	RDB
12	DB7
13	DB6
14	DB5
15	DB4
16	DB3
17	DB2
18	DB1
19	DB0
20	GND



NOTES:
1. DISPLAY TYPE: 1.77″, 128*160 TFT LCD
2. DISPLAY MODE: transmissive Normally White
3. VIEWING DIRECTION: 12 O'clock
4. DRIVER IC:ST7735S
5. LCM (White 9 AVG 1/9) :
   Brightness: 350cd/m^2 (TYP)
   Uniformity:80%(MIN)
6. OPERATING TEMP: -20° C TO 60° C,STORAGE TEMP: -30° C TO 70° C
7. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
8. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS

深圳市优瑞泰克科技有限公司					
PART NO.:	ET018QC01-T			MODULE NO.:	00
DRAWN BY:	LIU	DATE:		PROJECTION:	
CHECKED BY:		DATE:		SCALE: N.T.S	UNIT: mm
APPROVED BY:		DATE:		SHEET: 1 OF 1	

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+60	°C
LCM Storage Temperature	T_{STG}	-30	+70	°C
Humidity	RH	-	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO				V
Supply Voltage for(DC/DC)	VDD	2.7	2.8	3.3	V
Supply Voltage for(DC/DC)	AVDD				V
Supply Voltage for(DC/DC)	AVEE				V

4.2Back-Light Unit Characeristics

The back-light system is an edge-lighting type with 2 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	5.6	-	6.4	V	-
Forward current	I_F	--	20	-	mA	-
Luminance(With LCD)	Lv		350	--	cd/m^2	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:

5. Module Function Description

LCM Pin Descriptions

1	K	Power supply for backlight cathode input terminal.
2	A	Power supply for backlight anode input terminal.
3	GND	Gound
4~5	VDD(2.8v)	PINPOWER SUPPLY（2.7-3.3V）
6	NC	NC
7	CS	Chip select signal input pin
8	RESET	Reset signal input terminal. Active at ‘L’.
9	RS	Register select input pin
10	WR	This serves as a write strobe signal
11	RD	Read data at the rising edge.
12	DB7	Data bus
13	DB6	Data bus
14	DB5	Data bus
15	DB4	Data bus
16	DB3	Data bus
17	DB2	Data bus
18	DB1	Data bus
19	DB0	Data bus
20	GND	Gound

6. Timing Characteristics

VDDI and VDD can be applied in any order

VDD and VDDI can be powered down in any order

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

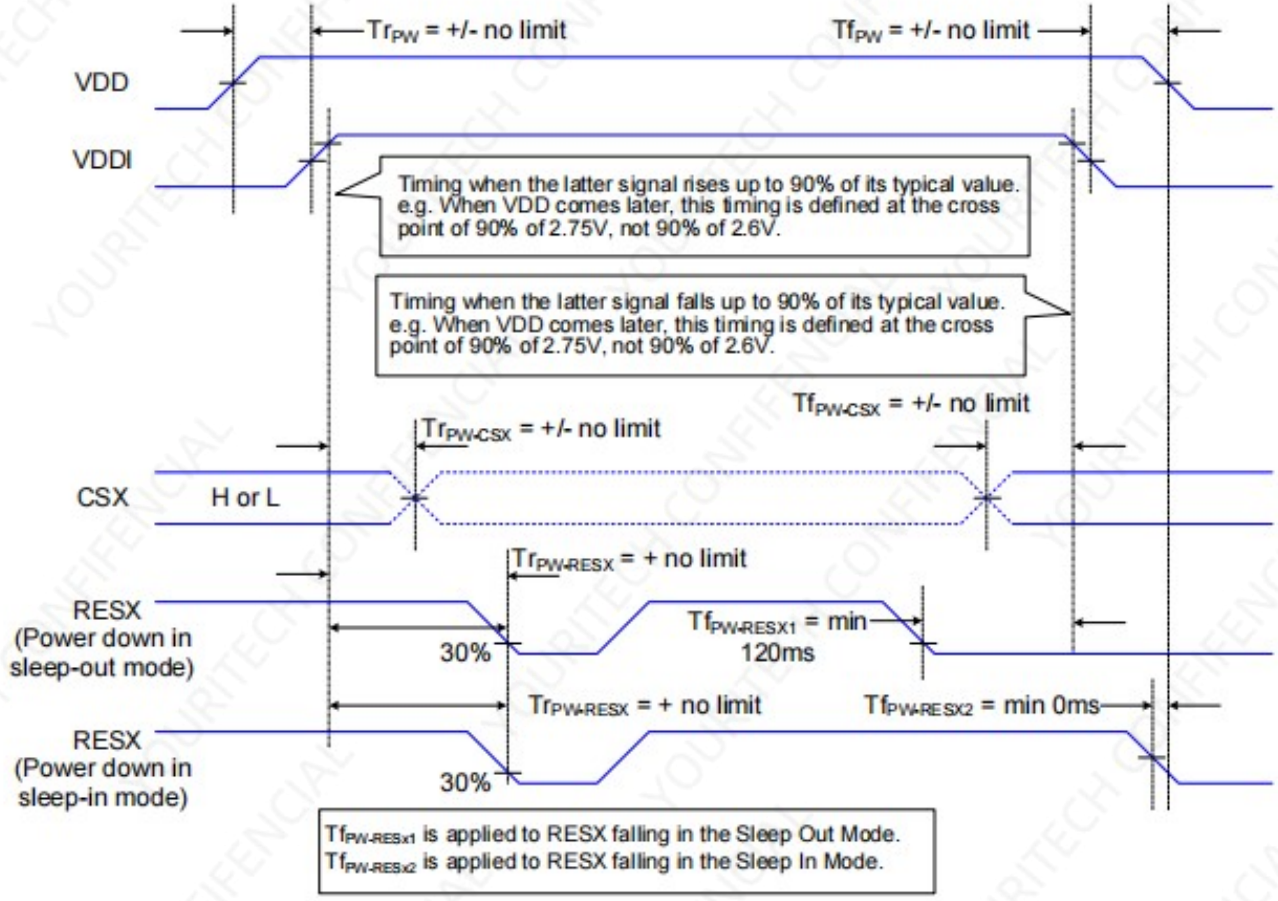
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

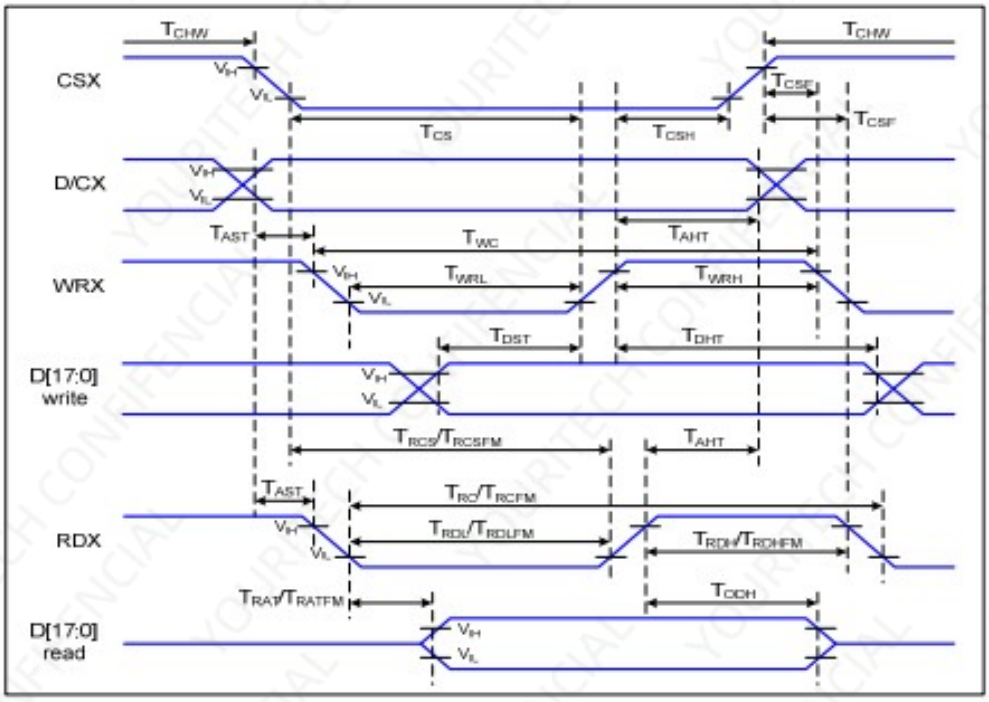


Figure 1 Parallel Interface Timing Characteristics (8080 Ceries MCU Interface)

Ta=25 ℃, VDDI=1.65~3.7V, VDD=2.5~4.8V

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	TAST	Address Setup Ttime	0		ns	-
	TAHT	Address Hold Time (Write/Read)	10		ns	
CSX	TCHW	Chip Select "H" Pulse Width	0		ns	-
	TCS	Chip Select Setup Time (Write)	15		ns	
	TRCS	Chip Select Setup Time (Read ID)	45		ns	
	TRCSFM	Chip Select Setup time (Read FM)	355		ns	
	TCSF	Chip Select Wait Time (Write/Read)	10		ns	
	TCSH	Chip Select Hold Time	10		ns	
WRX	TWC	Write Cycle	66		ns	
	TWRH	Control Pulse "H" Duration	15		ns	
	TWRL	Control Pulse "L" Duration	15		ns	
RDX (ID)	TRC	Read Cycle (ID)	160		ns	When Read ID Data
	TRDH	Control Pulse "H" Duration (ID)	90		ns	
	TRDL	Control Pulse "L" Duration (ID)	45		ns	

RDX (FM)	TRCFM	Read Cycle (FM)	450		ns	When Read from Frame Memory
	TRDHFM	Control Pulse "H" Duration (FM)	90		ns	
	TRDLFM	Control Pulse "L" Duration (FM)	355		ns	
D[17:0]	TDST	Data Setup Time	10		ns	For CL=30pF
	TDHT	Data Hold Time	10		ns	
	TRAT	Read Access Time (ID)		40	ns	
	TRATFM	Read Access Time (FM)		340	ns	
	TODH	Output Disable Time	20	80	ns	

Table 4 8080 Parallel Interface Characteristics

Figure 2 Rising And Falling Timing for Input And Output Signal

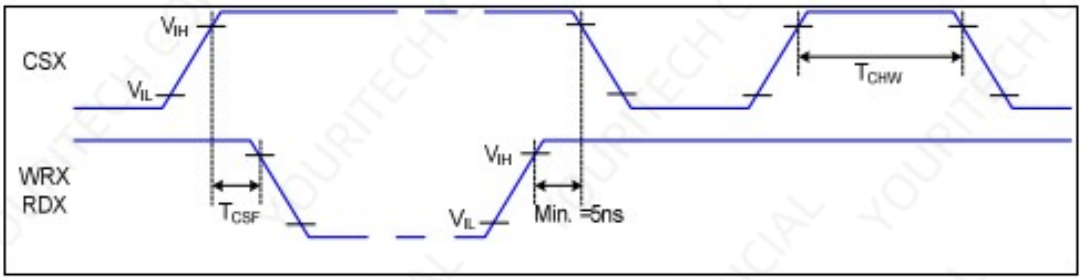


Figure 3 Chip Selection (CSX) Timing

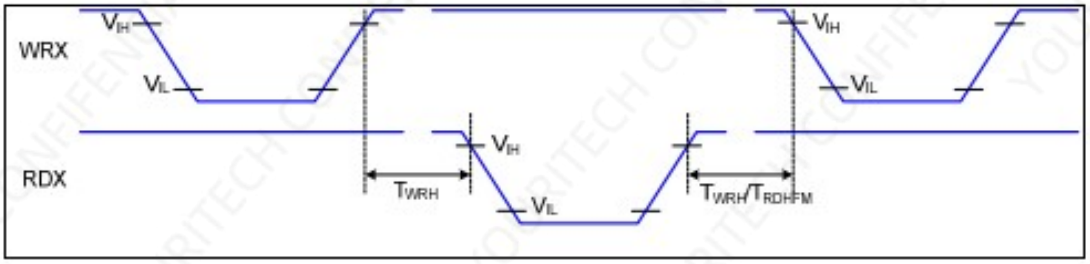
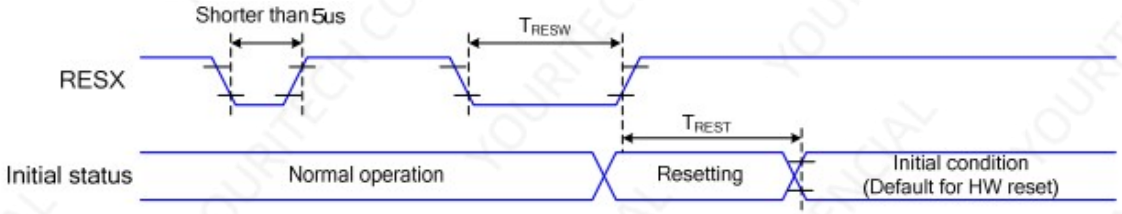


Figure 4 Write-to-Read And Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Reset Timing:



Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	tRESW	Reset Pulse Duration	10	-	us
	tREST	Reset Cancel	-	5	ms
				120	ms

Table 14 Reset Timing

Notes:

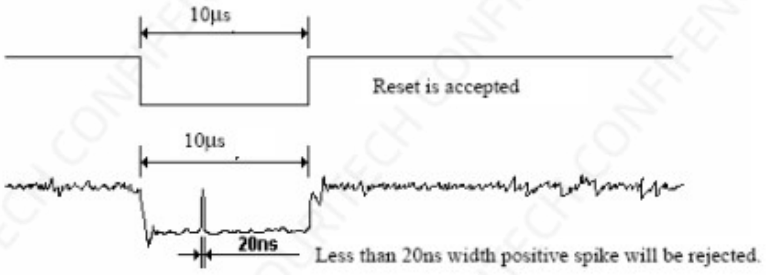
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset Starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Item		Symbol	Conditions	Specifications			Unit	Note
				Min.	Typ.	Max.		
Transmittance		T%	Viewing normal angle $\theta_X = \theta_Y = 0°$	6.21	6.9	-	%	All left side data are based on CMI's following condition – 1.LC : TN 2.Light Source :CMI LED BLU 3.Film : 日東 NPF TEG 1465DU 4.Machine : DMS 803 5.EWV Pol
Contrast Ratio		CR		200	300	-		
Response Time (by Quick)		$T_{on}+T_{off}$		-	30	60	ms	
Viewing Angle	Hor.	θ_{X+}	Center CR>10	60	70	-	deg.	
		θ_{X-}		60	70	-		
	Ver.	θ_{Y+}		60	70	-		
		θ_{Y-}		45	50	-		
CF only Color Chromaticity (CIE 1931)	Red	X_R	Viewing normal angle $\theta_X = \theta_Y = 0°$	0.590	0.610	0.630		1.Under C light Simulation 2.NTSC 55%
		Y_R		0.309	0.329	0.349		
	Green	X_G		0.279	0.299	0.319		
		Y_G		0.547	0.567	0.587		
	Blue	X_B		0.123	0.143	0.163		
		Y_B		0.091	0.111	0.131		
	White	X_W		0.288	0.308	0.328		
		Y_W		0.307	0.327	0.347		

Note 1: Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

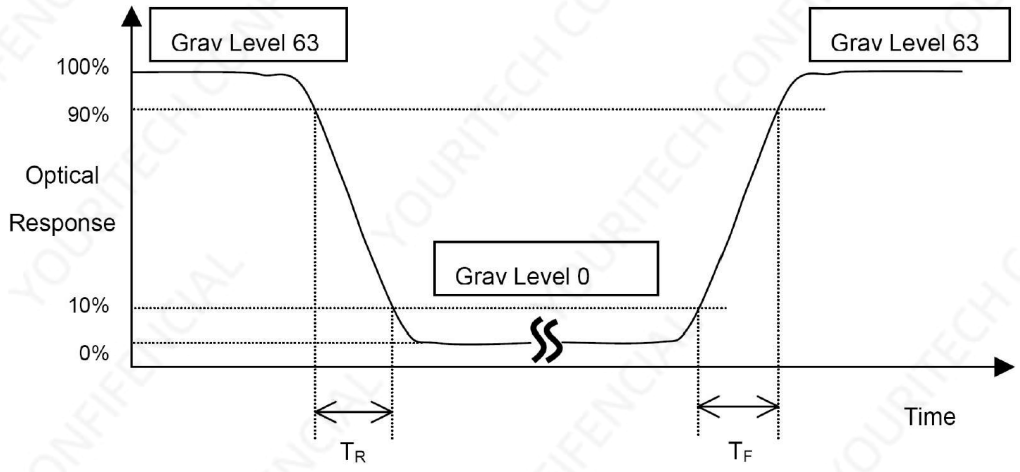
L63: Luminance of gray level 63

L0: Luminance of gray level 0

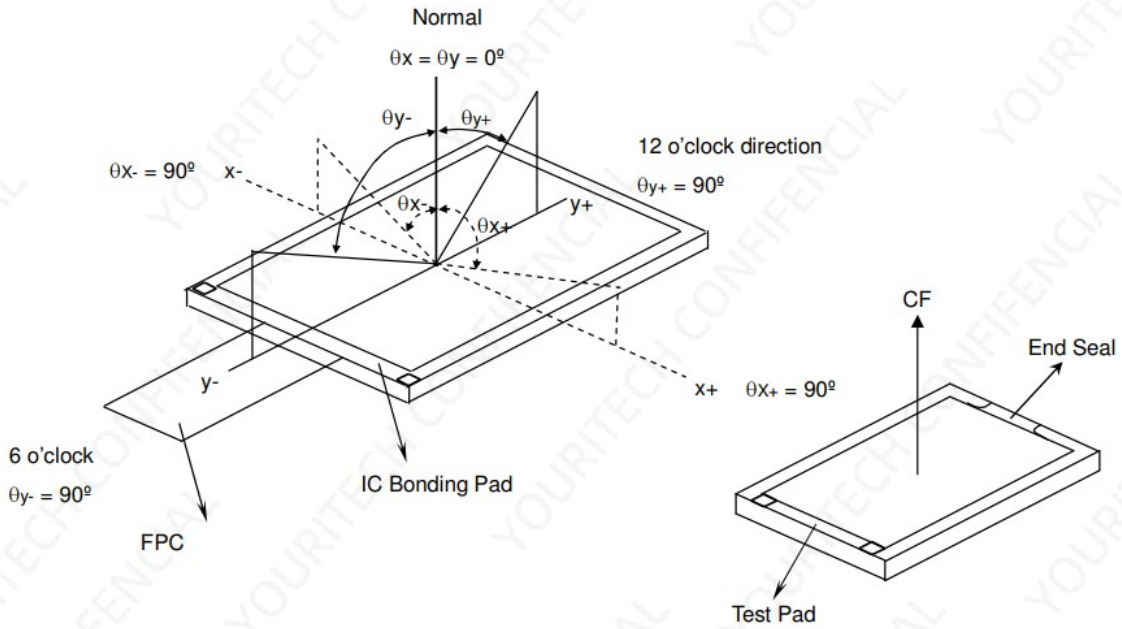
CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note 5.

Note 2: Definition of Response Time (TR, TF):



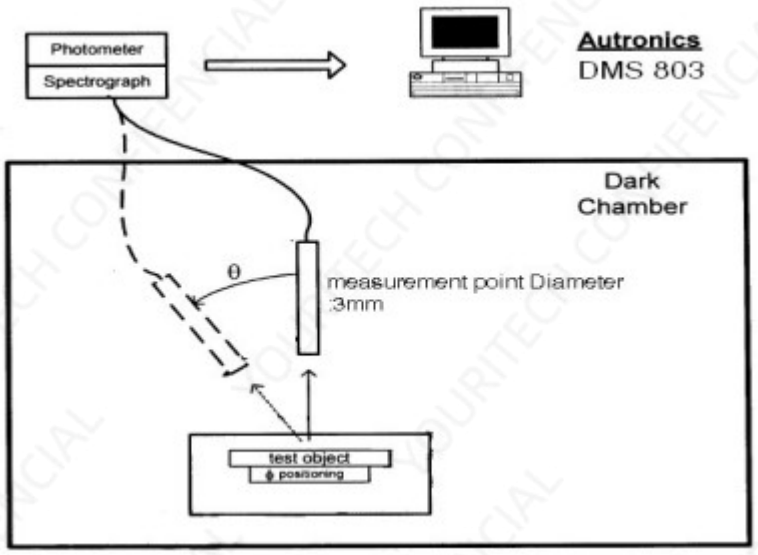
Note 3: Viewing Angle



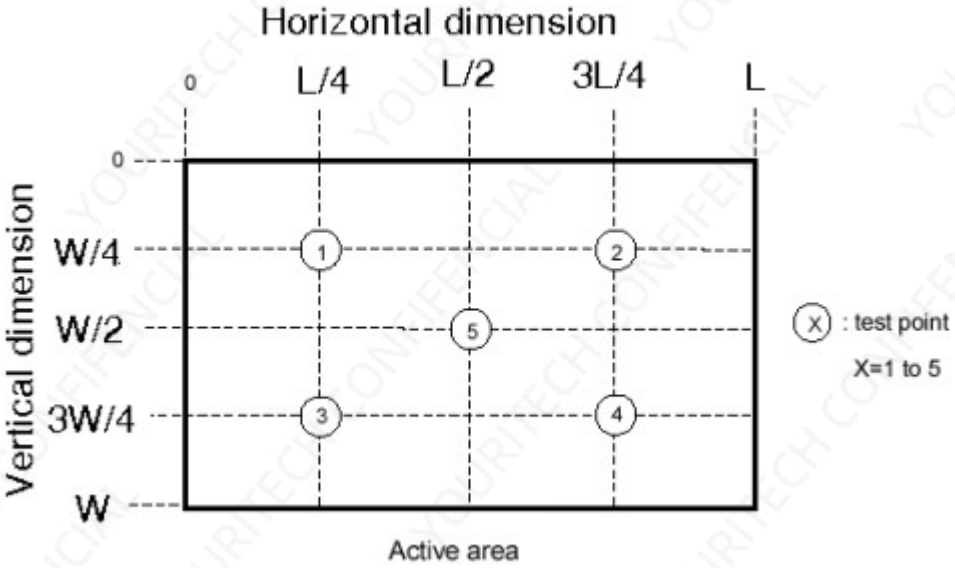
The above "Viewing Angle" is the measuring position with Largest Contrast Ratio; not for good image quality. View Direction for good image quality is 6 O'clock. Module maker can increase the "Viewing Angle" by applying Wide View Film.

Note 4: Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note 5:



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+70°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+60°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~70℃（30min），50 cycles	

9. Packing Method----TBD

- END -