

INDUSTRIAL STRENGTH... Start Your Application From **YOURITECH**

Integration support

Obsolescence Management

PCAP

Embedded Systems

Human Machine Interface

Touch Solutions

Software

Quality Management

Open Frame Monitors

LCD Controller

Research & Development

Firmware

EMC tests

on-site service

In-house Manufacturing

Optical Bonding

Cover glass

System solutions

OEM Solutions

Custom Display

Production
Custom designs
Installation

Mechanical design



MODEL NO : ET020HV05-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-12-29

☐ Preliminary Specification

☒ Final Product Specification

Customer : _____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

This LCD module should be designed for mobile phone use.

LCD specification: Dots 240xRGBx320.

As to basic specification of the driver IC, refer to the IC (Orise:ST7789V2) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;

ALL O'CLOCK Type LCD

240 dot-segment and 320 dot-common outputs;

65K/262K Color can be selected by software;

White LED back light;

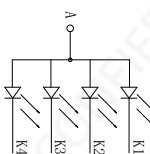
8bit MCU interface

1.3 Applications:

2. LCM General specification

ITEM	Standard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	240*3RGB(H)X320(V)	Dots
Pixel arrangement	RGB stripe	--
Pixel Pitch (W*H)	0.1275(W)x 0.1275(H)	mm
Active area	30.60(W) x40.80(H)	mm
Module Size(W*H*T)	35.70(W) x51.20(H) x2.30(T)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	ST7789V2	--
TFT interface	8bit MCU interface	--
Approx. Weight	TBD	g

NO.	SYMBOL
1	GND
2	VCI
3	IM2
4	IM1
5	RESET
6	CS
7	DC(SP1-SCL)
8	WR(SP1-RS)
9	RD
10	SDA
11	DB0
12	DB1
13	DB2
14	DB3
15	DB4
16	DB5
17	DB6
18	DB7
19	SD0
20	LED-A
21	LED-K1
22	LED-K2
23	LED-K3
24	LED-K4
25	GND
26	TP_RST(NC)
27	TP_SCL(NC)
28	TP_SDA(NC)
29	TP_INT(NC)
30	GND



- NOTES:
1. DISPLAY TYPE: 2.0", 240*320 TFT LCD
 2. DISPLAY MODE: transmissive **Normally Black**
 3. VIEWING DIRECTION: **ALL**
 4. DRIVER IC: S1789V
 5. LCM (White 9 AVG 1/9) :
Brightness: 400cd/m² (TYP)
Uniformity: 80% (MIN)
 6. BACK LIGHT: 4 chip white LEDs If=80mA Vf=2.8V~3.3V
 7. OPERATING TEMP: -20° C to 70° C, STORAGE TEMP: -30° C to 80° C
 8. * Critical Parameters, () ref Parameter, [] cpk Parameter
Unspecified Tolerances: ±0.20mm
 9. Modification mark:
SUGGESTION: TP window size unilateral increase 0.3~0.5mm than LCM A.A.
 10. RECOMMENDS ENVIRONMENTAL PROTECTION: RoHS

PART NO. : EIT020HV05-T		MOQ/LOT NO. : 00	
DRAWN BY :	LIT	DATE :	
CHECKED BY :		DATE :	
APPROVED BY :		DATE :	
		PROJECTION :	
		SCALE: N.T.S	UNIT: mm
		SHEET: 1	OF 1

3. Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T _{OPR}	-20	+70	°C
LCM Storage Temperature	T _{STG}	-30	+80	°C
Humidity	RH	10	90	%

4. Electrical Characteristics

4.1 TFT DC Characteristics

(Ta=25±2°C)

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage 1	VDDIO	--	--	--	V	--
Power Supply Voltage 2	VDD	2.6	2.8	3.3	V	--
Power Supply Voltage 3	VDD3	--	--	--	V	--
Power Supply for MTP	VPP	--	--	--	V	--

4.2 Back-Light Unit Characteristics

The back-light system is an edge-lighting type with 3 white LEDs. The characteristics of the back-light are shown in the following tables.

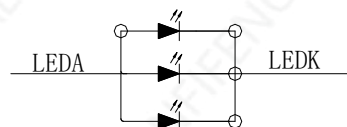
(Ta=25±2°C)

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V _F	2.8	--	3.2	V	--
Forward current	I _F	--	80	--	mA	--
Luminance(With LCD)	L _v	--	400	--	cd/m ²	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

- (1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:

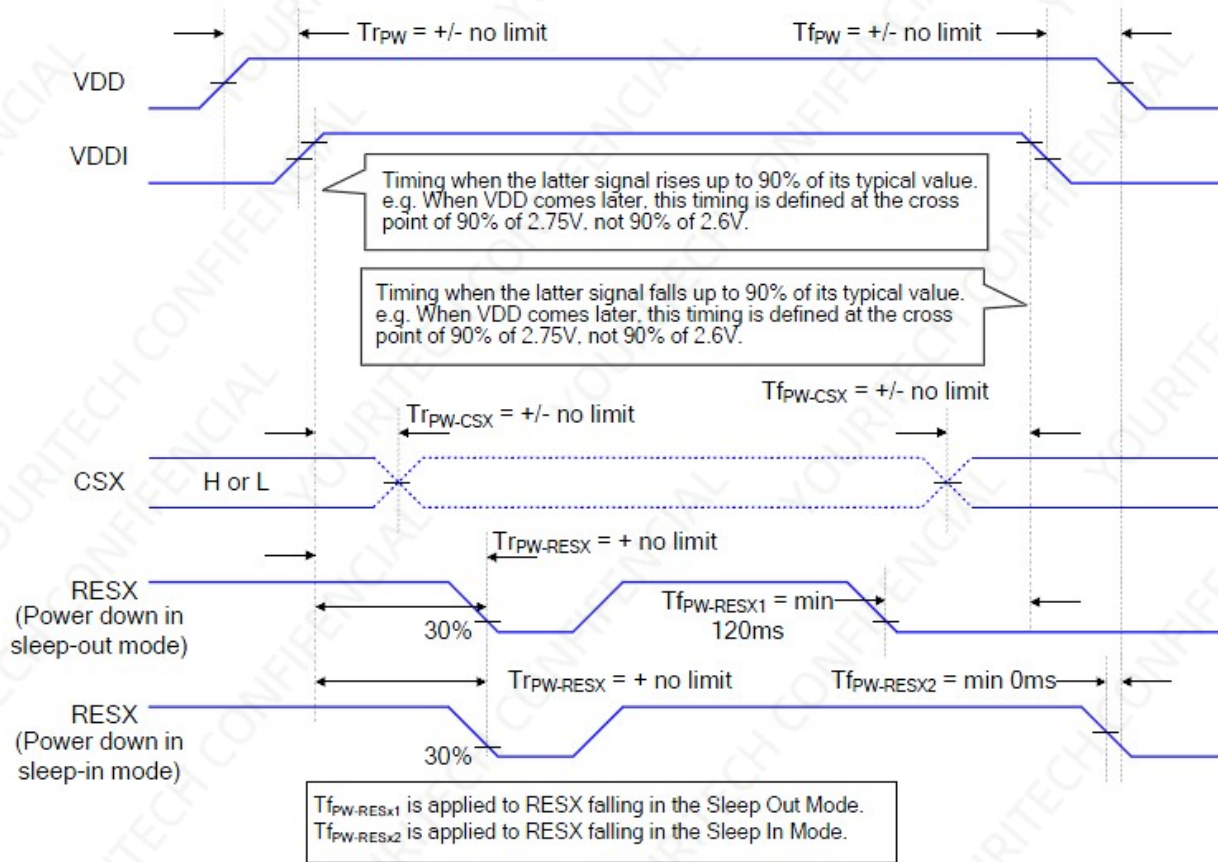


5. Module Function Description

Pin No.	Symbol	Functional	Notes																	
1	GND	Power Ground																		
2	VCI	power supply for DC/DC circuit(2.8V)																		
3-4	IM2-IM1	<table><tr><td>IM3</td><td>IM2</td><td>IM1</td><td>IM0</td><td>MPU Interface Mode</td><td>Data pin</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80-8bit parallel I/F</td><td>DB[7:0]</td></tr></table> <table><tr><td>0</td><td>1</td><td>0</td><td>4-line 8bit serial I/F</td><td>SDA: in/out</td></tr></table>	IM3	IM2	IM1	IM0	MPU Interface Mode	Data pin	0	0	0	0	80-8bit parallel I/F	DB[7:0]	0	1	0	4-line 8bit serial I/F	SDA: in/out	
IM3	IM2	IM1	IM0	MPU Interface Mode	Data pin															
0	0	0	0	80-8bit parallel I/F	DB[7:0]															
0	1	0	4-line 8bit serial I/F	SDA: in/out																
5	RESET	Reset signal input terminal. Active at ‘L’.																		
6	CS	Chip select signal input pin																		
7	RS	Display data/command selection pin																		
8	WR	Write enable in MCU parallel interface.																		
9	RD	Read data at the rising edge.																		
10	SDA	Serial data input/output pin.																		
11-18	DB0~DB7	DB[15:0] are used as MCU parallel interface data bus.																		
19	SDO	Serial data output pin.																		
20	LEDA	Power supply for backlight anode input terminal.																		
21	LEDK1	Power supply for backlight cathode input terminal.																		
22	LEDK2	Power supply for backlight cathode input terminal.																		
23	LEDK3	Power supply for backlight cathode input terminal.																		
24	LEDK4	Power supply for backlight cathode input terminal.																		
25	GND	Power Ground																		
26	CTP-RST(NC)	NC																		
27	CTP-SCL(NC)	NC																		
28	CTP-SDA(NC)	NC																		
29	CTP-INT(NC)	NC																		
30	GND	Power Ground																		

6. Timing Characteristics

The power on/off sequence is illustrated below



8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

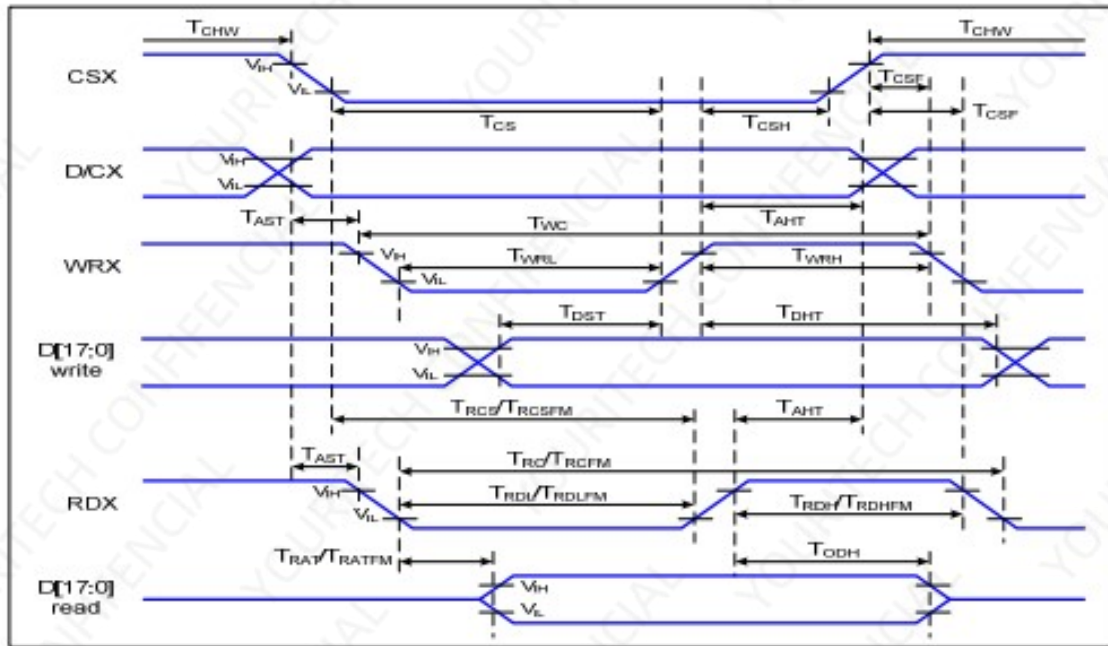


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25°C

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T _{AST}	Address setup time	0		ns	-
	T _{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T _{CHW}	Chip select "H" pulse width	0		ns	-
	T _{CS}	Chip select setup time (Write)	15		ns	
	T _{RC}	Chip select setup time (Read ID)	45		ns	
	T _{RCF}	Chip select setup time (Read FM)	355		ns	
	T _{CSF}	Chip select wait time (Write/Read)	10		ns	
	T _{CSH}	Chip select hold time	10		ns	
WRX	T _{WC}	Write cycle	66		ns	
	T _{WRH}	Control pulse "H" duration	15		ns	
	T _{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T _{RC}	Read cycle (ID)	160		ns	When read ID data
	T _{RDH}	Control pulse "H" duration (ID)	90		ns	
	T _{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T _{RCF}	Read cycle (FM)	450		ns	When read from frame memory
	T _{RDHF}	Control pulse "H" duration (FM)	90		ns	
	T _{RDLF}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T _{DST}	Data setup time	10		ns	For CL=30pF

T_{DHT}	Data hold time	10		ns
T_{RAT}	Read access time (ID)		40	ns
T_{RATFM}	Read access time (FM)		340	ns
T_{ODH}	Output disable time	20	80	ns

Table 4 8080 Parallel Interface Characteristics

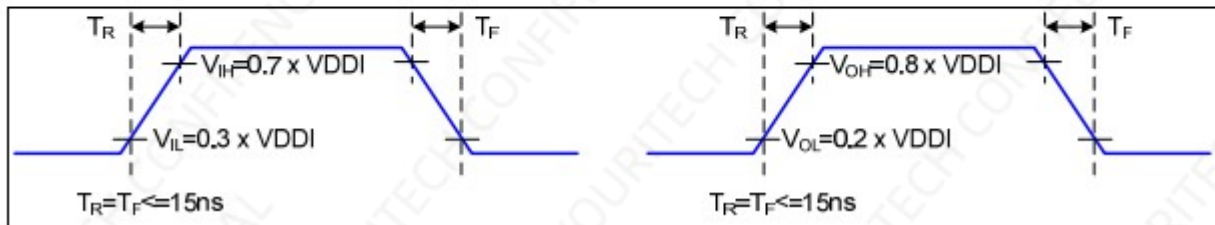


Figure 2 Rising and Falling Timing for I/O Signal

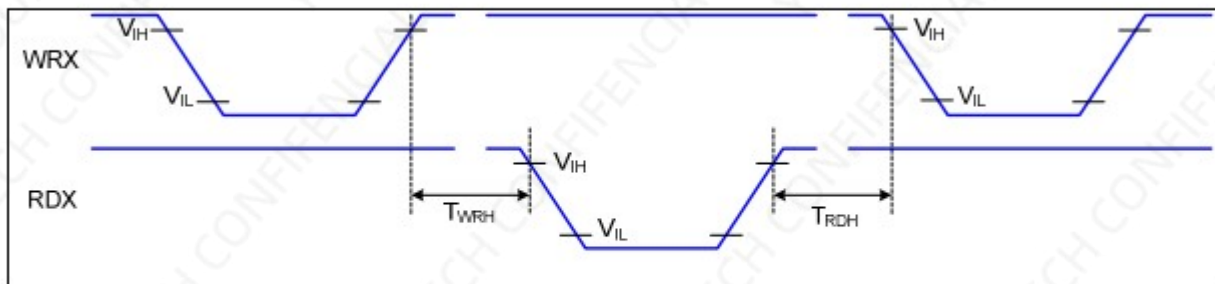


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (T_R , T_F) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Reset Timing:

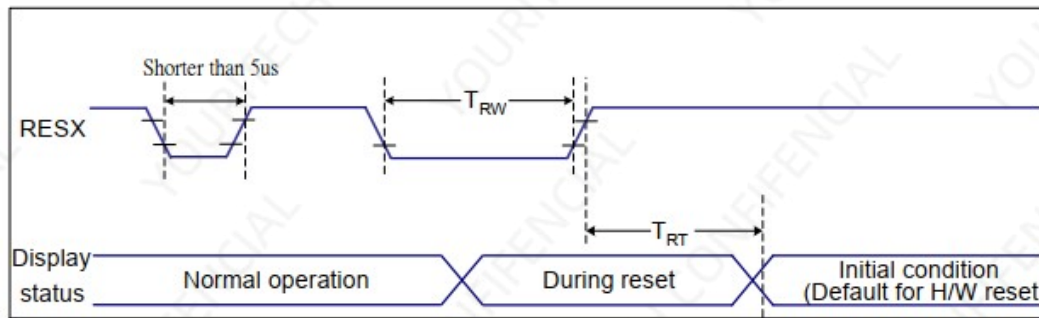


Figure 7 Reset Timing

$V_{DDI}=1.65$ to $3.3V$, $V_{DD}=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a=25^{\circ}C$

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

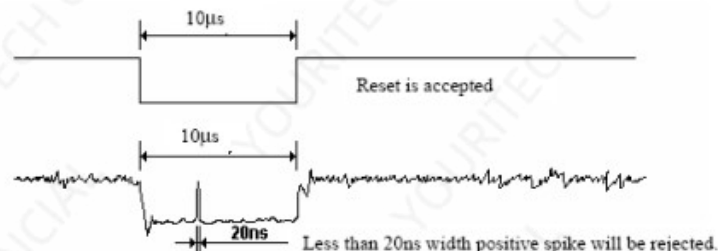
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Optical Specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T(%)	—	—	(4.50)	—	%	Normal POL
Transmittance (without Polarizer)		T(%)	—	—	(12.20)	—	%	
Contrast Ratio		CR	$\Theta=0$ Normal viewing angle	640	800	—	—	(1)(2)
Response Time		$T_R + T_F$		—	30	40	msec	(1)(3)
Color Gamut		S(%)		54	60	—	%	
Color Chromaticity (CIE1931)	White	W_x		± 0.02	(0.296)	± 0.02		(1)(4) CF glass
		W_y			(0.325)			
	Red	R_x			(0.647)			
		R_y			(0.329)			
	Green	G_x			(0.279)			
		G_y			(0.550)			
	Blue	B_x			(0.134)			
		B_y			(0.123)			
Viewing Angle	Hor.	Θ_L	CR>10	—	80	—		Viewing Angle base on using Normal Polarizer , Reference Only
		Θ_R		—	80	—		
	Ver.	Θ_U		—	80	—		
		Θ_D		—	80	—		
Optima View Direction		ALL						(5)

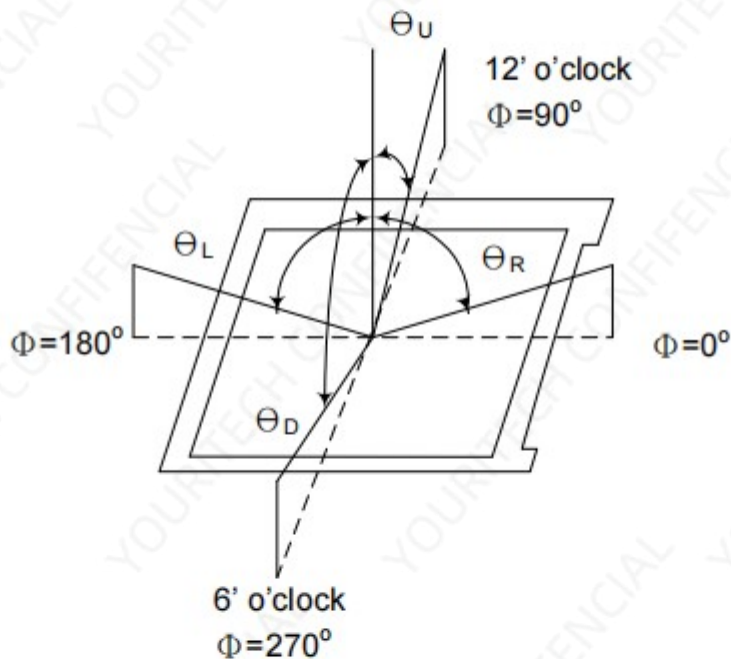
Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : $25 \pm 2^\circ\text{C}$
- 15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1) Definition of Viewing Angle:

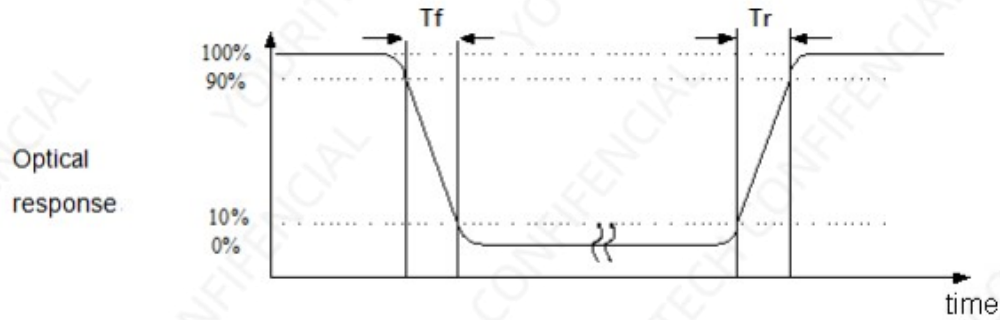


Note (2) Definition of Contrast Ratio (CR):

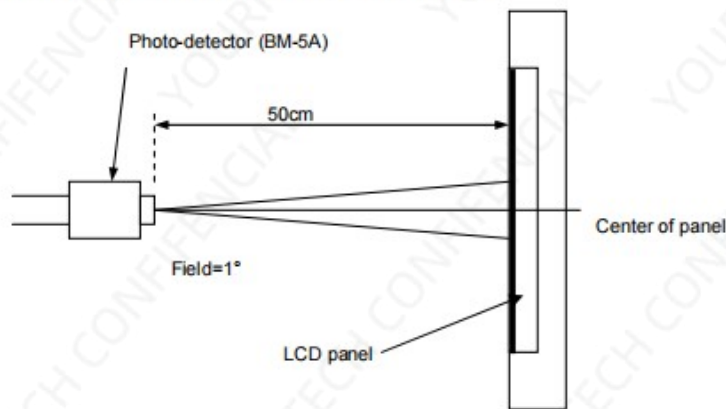
measured at the center point of panel

$$\text{CR} = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

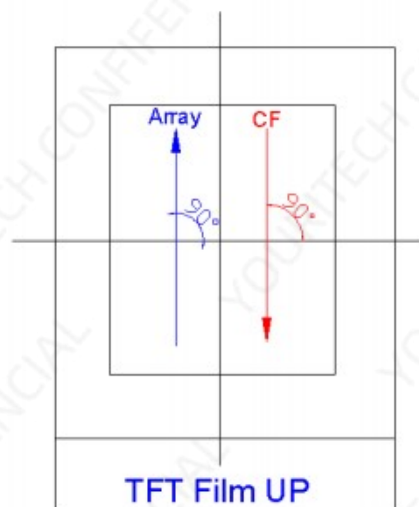
Note (3) Definition of Response Time: Sum of T_R and T_F



Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.)



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state, -20°C (30min) ~60°C (30min) , 50 cycles	

9. Packing Method----TBD

- END -