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MODEL NO : ET020HV08-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2021-09-02

□Preliminary Specification

■Final Product Specification

Customer :_____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 480xRGBx360.
As to basic specification of the driver IC, refer to the IC (Sitronix:ST7701S) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

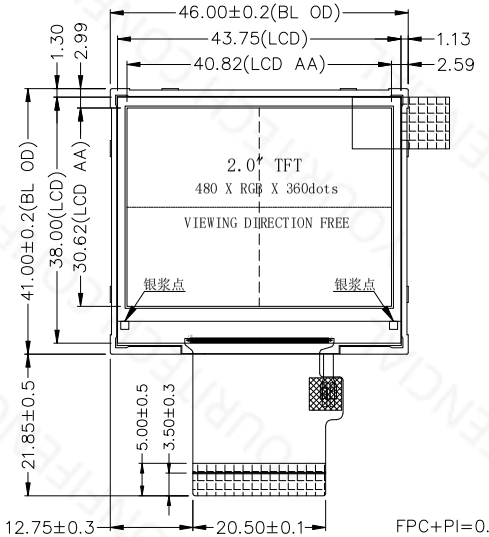
Structure: TFT PANNEL+IC +FPC+BL;
IPS Type LCD
480dot-segment and 360 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
3SPI+16bit RGB or 2lane MIPI interface

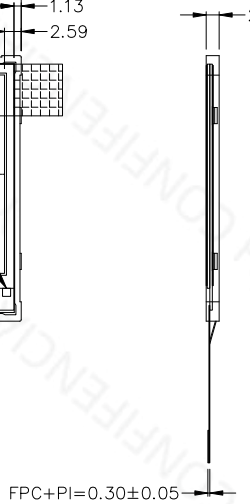
1.3 Applications:

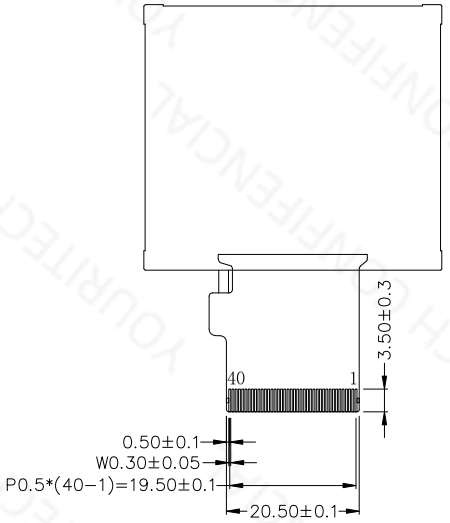
2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally black	--
Drive element	TFT active matrix	--
Number of pixels	480*3RGB(H)X360(V)	Dots
Pixel arrangement	RGB Vertical stripe	--
Pixel Pitch (W*H)	0.08505x0.08505	mm
Active area	40.824(H) x 30.618(V)	mm
Viewing direction	ALL O'CLOCK	-
TFT Driver IC	ST7701S	
TFT interface	3SPI+16bit RGB or 2lane MIPI interface	-
Module Size(W*H*T)	46.00(H) x 41.00(V) x2.00(T)	mm
Approx. Weight	TBD	g
Touch structure	--	
Touch Driver IC	--	-
Touch Interface	--	

REV	DESCRIPTION	DRG DATE	DRAWN BY
	First Desing	2021.04.14	

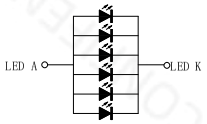






PIN	SYMBOL	PIN	SYMBOL
1	LEDK	1	LEDK
2	LEDA	2	LEDA
3	GND	3	GND
4	VDD	4	VDD
5	D0N	5	GND
6	D0P	6	GND
7	GND	7	GND
8	CKN	8	GND
9	CKP	9	GND
10	GND	10	GND
11	D1N	11	GND
12	D1P	12	GND
13	GND	13	GND
14	GND	14	VS
15	GND	15	HS
16	GND	16	PCLK
17	GND	17	DE
18	GND	18	B0
19	GND	19	B1
20	GND	20	B2
21	GND	21	B3
22	GND	22	B4
23	GND	23	G0
24	GND	24	G1
25	GND	25	G2
26	GND	26	G3
27	GND	27	G4
28	GND	28	G5
29	GND	29	R0
30	GND	30	R1
31	GND	31	R2
32	GND	32	R3
33	GND	33	R4
34	RESET	34	RESET
35	GND	35	CS
36	GND	36	SCL
37	GND	37	SDA
38	IM0	38	IM0
39	IM1	39	IM1
40	IM2	40	IM2

CIRCUIT DIAGRAM



展开出货

接口选择	IM0	IM1	IM2
MIPI 2L	1	0	1
RGB 16位	0	1	0

NOTES:
1. DISPLAY TYPE: 2.0", 480*360 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL
4. DRIVER IC:ST7701S
5. LCM (White 9 AVG 1/9) :
   Brightness: 600cd/m^2 (TYP)
   Uniformity:80%(MIN)
6. BACK LIGHT: 6 chip white LEDs If=120mA,Vf=2.9V-3.3V
7. OPERATING TEMP: -20° C TO 60° C,STORAGE TEMP: -30° C TO 70° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS

深圳市优瑞泰克科技有限公司

PART NO.:	ET020HV08-T			MODULE NO.:	00
DRAWN BY:	LIU	DATE:		PROJECTION:	
CHECKED BY:		DATE:		SCALE:N.T.S	UNIT: mm
APPROVED BY:		DATE:		SHEET: 1 OF 1	

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+60	°C
LCM Storage Temperature	T_{STG}	-30	+70	°C
Humidity	RH	-	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	--	--	--	V
Supply Voltage for(DC/DC)	VDD	2.5	2.8	3.6	V
Supply Voltage for(DC/DC)	AVDD				V
Supply Voltage for(DC/DC)	AVEE				V

4.2 Back-Light Unit Characeristics

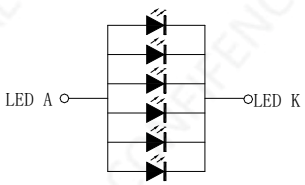
The back-light system is an edge-lighting type with 6 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	2.9	--	3.3	V	-
Forward current	I_F	--	120	-	mA	-
Luminance(With LCD)	Lv		600	--	cd/m^2	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



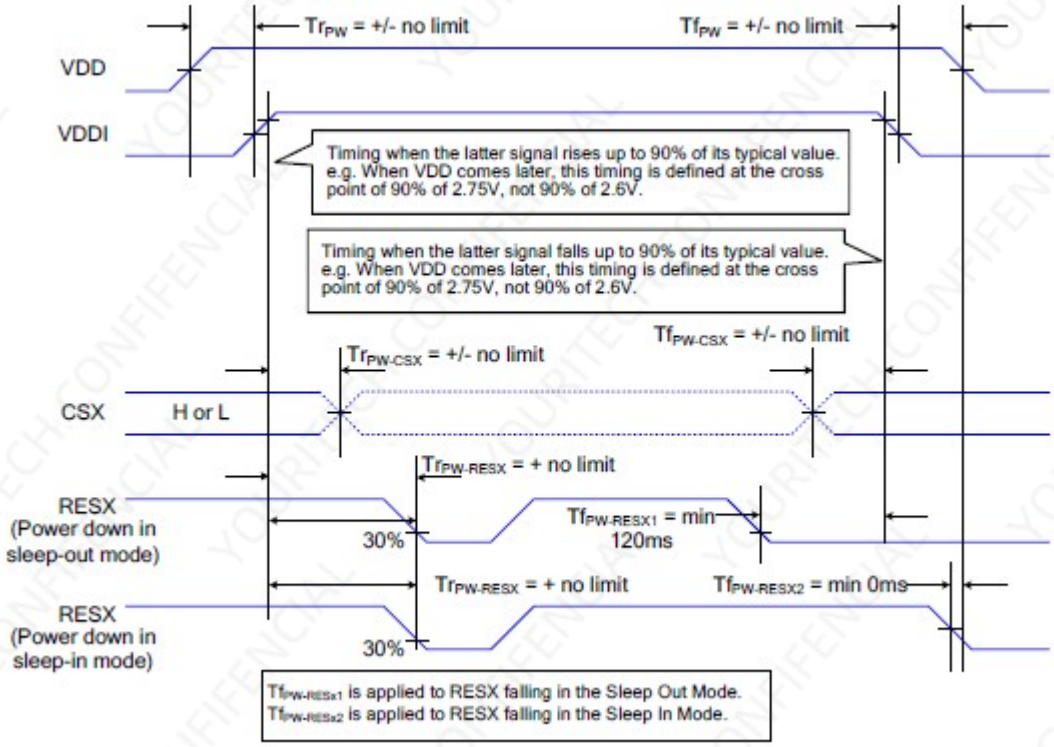
5. Module Function Description

Pin No.	Symbol RGB interface	(RGB interface)Functional	Notes
1	LEDK	Power supply for backlight cathode input terminal.	
2	LEDA	Power supply for backlight anode input terminal.	
3	GND	Power Ground	
4	VDD	Power supply：2.5V～3.3V	
5	GND	Power Ground	
6	GND	Power Ground	
7	GND	Power Ground	
8	GND	Power Ground	
9	GND	Power Ground	
10	GND	Power Ground	
11	GND	Power Ground	
12	GND	Power Ground	
13	GND	Power Ground	
14	VSYNC	Vertical synchronizing input signal for RGB interface operation.	
15	HSYNC	Horizontal synchronizing input signal for RGB interface operation.	
16	PCLK	Dot clock signal for RGB interface operation.	
17	DE	Data enable signal for RGB interface operation.	
18~22	B0~B7	RGB interface data bus.	
23~28	G0~G5	RGB interface data bus.	
29~33	R0~R4	RGB interface data bus.	
34	RESET	The external reset input initializes the chip with a low input.	
35	CS	Chip select signal input pin	
36	SCL	Serial interface clock	
37	SDA	Input/Output signal pin	
38	IM0	Connected to Power Ground	
39	IM1	Connected to Power supply：2.5V～3.3V	
40	IM2	Connected to Power Ground	
Pin No.	Symbol MIPI interface	(MIPI interface)Functional	Notes
1	LEDK	Power supply for backlight cathode input terminal.	

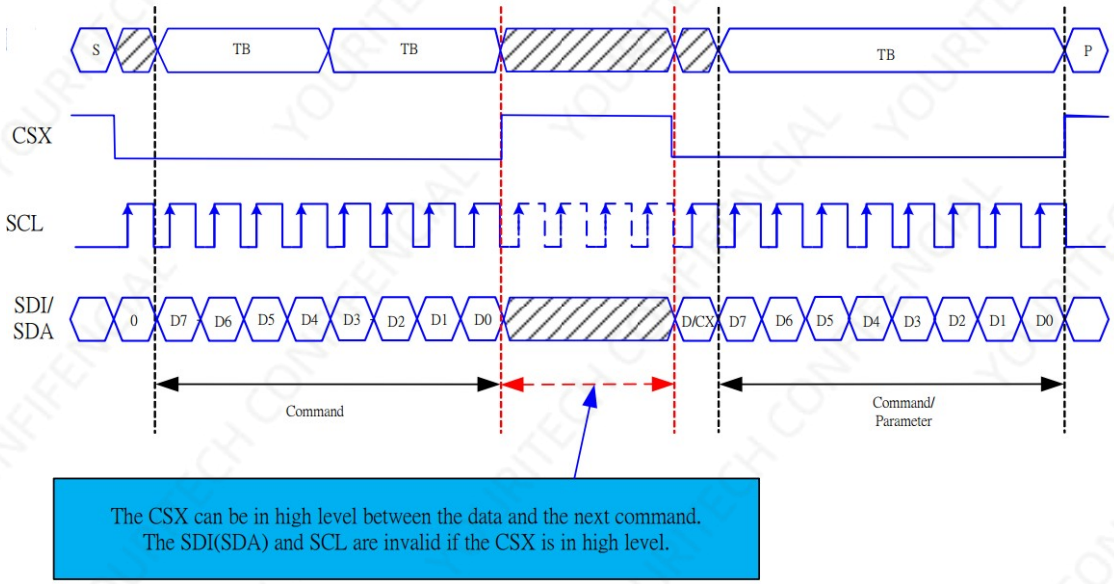
2	LEDA	Power supply for backlight anode input terminal.	
3	GND	Power Ground	
4	VDD	Power supply: 2.5V ~ 3.3V	
5	D0N	MIPI-DSI Data differential signal input pins	
6	D0P	MIPI-DSI Data differential signal input pins	
7	GND	Power Ground	
8	CLKN	MIPI-DSI CLOCK differential signal input pins	
9	CLKP	MIPI-DSI CLOCK differential signal input pins	
10	GND	Power Ground	
11	D1N	MIPI-DSI Data differential signal input pins	
12	D1P	MIPI-DSI Data differential signal input pins	
13	GND	Power Ground	
14	GND	Power Ground	
15	GND	Power Ground	
16	GND	Power Ground	
17	GND	Power Ground	
18~22	GND	Power Ground	
23~28	GND	Power Ground	
29~33	GND	Power Ground	
34	RESET	The external reset input initializes the chip with a low input.	
35	GND	Power Ground	
36	GND	Power Ground	
37	GND	Power Ground	
38	IM0	Connected to Power supply: 2.5V ~ 3.3V	
39	IM1	Connected to Power Ground	
40	IM2	Connected to Power supply: 2.5V ~ 3.3V	

6. Timing Characteristics

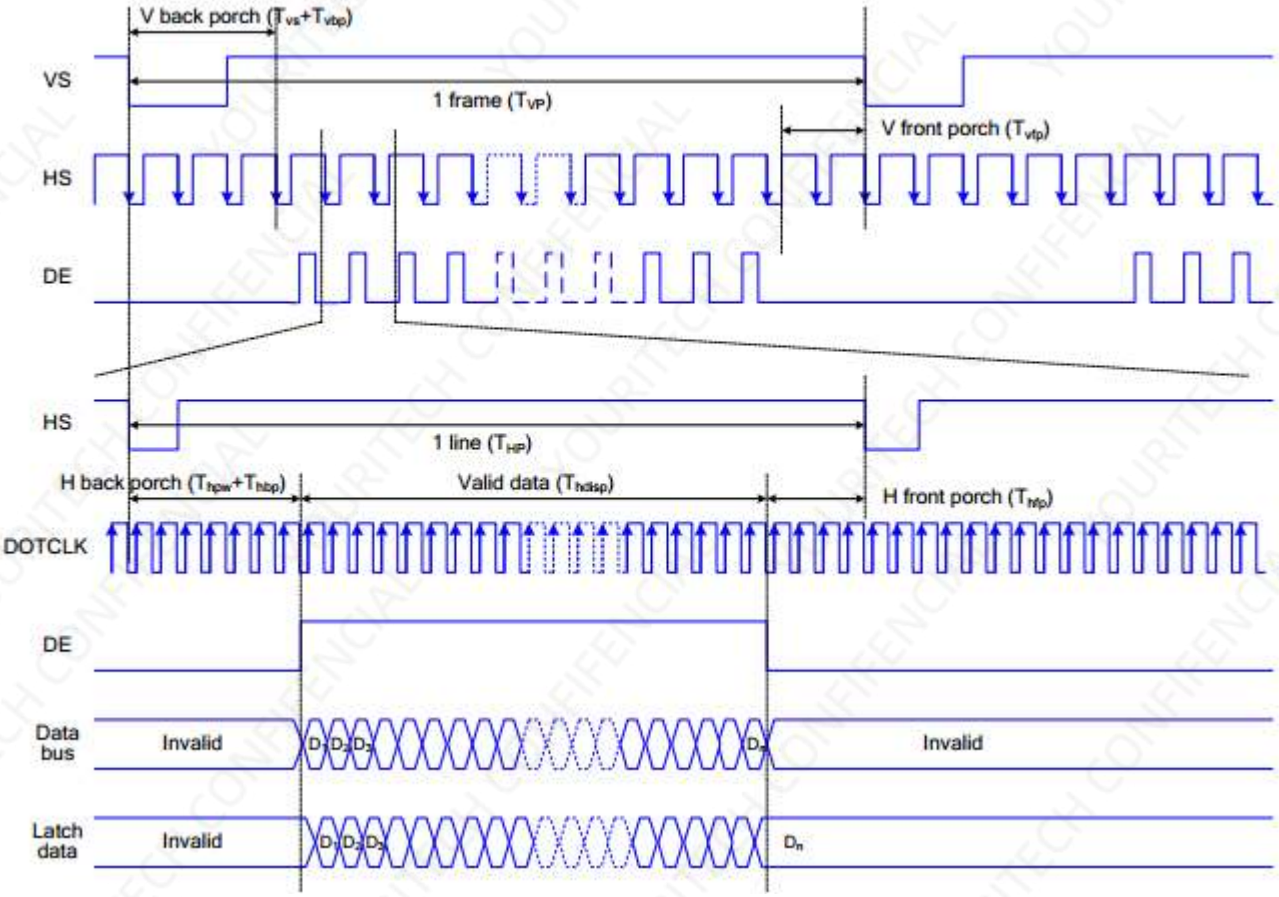
POWER ON/OFF SEQUENCE



SPI interface pause



The timing chart of RGB interface DE mode is shown as follows.



Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	1	-	255	Clock
Horizontal Sync. Back Porch	hbp	1	--	255	Clock
Horizontal Sync. Front Porch	hfp	1	--	-	Clock
Vertical Sync. Width	vs	1	--	254	Line
Vertical Sync. Back Porch	vbp	1	--	254	Line
Vertical Sync. Front Porch	vfp	2	--	--	Line

DSI-MIPI Interface Timing Characteristics of IC

Normal Write Mode (VCC = IOVCC=2.4~3.3V)

High Speed Mode

DSI clock channel timing

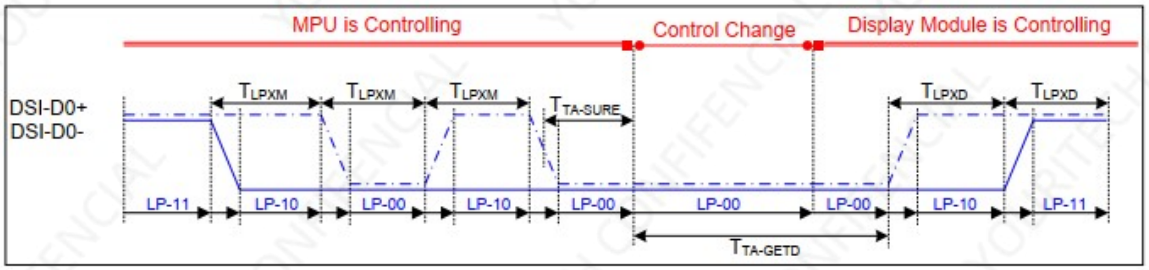
Rising and falling time on clock and data channel

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

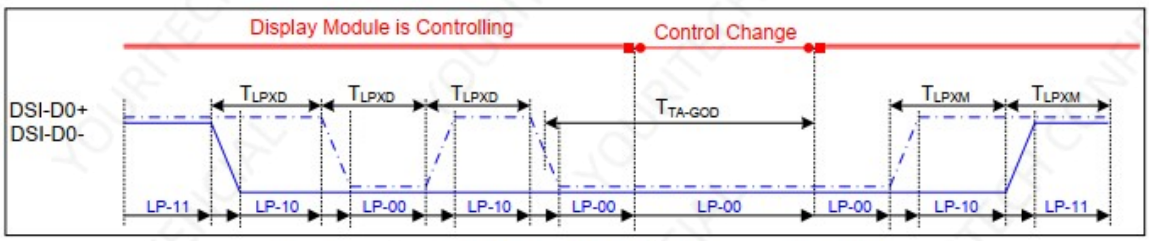
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Mipi Interface- High Speed Mode Timing Characteristics

Lowe Power Mode



Bus Turnaround (BTA) from display module to MPU Timing



Bus Turnaround (BTA) from MPU to display module Timing

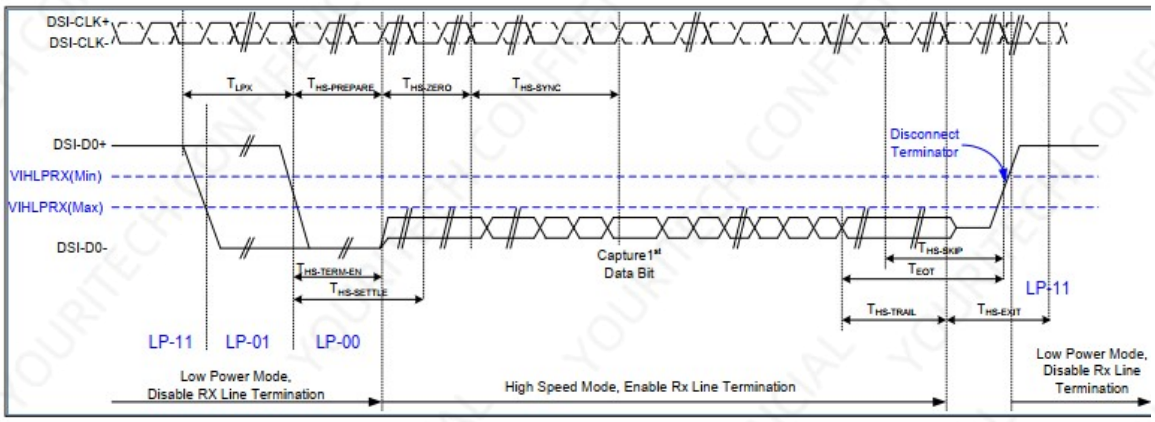
VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

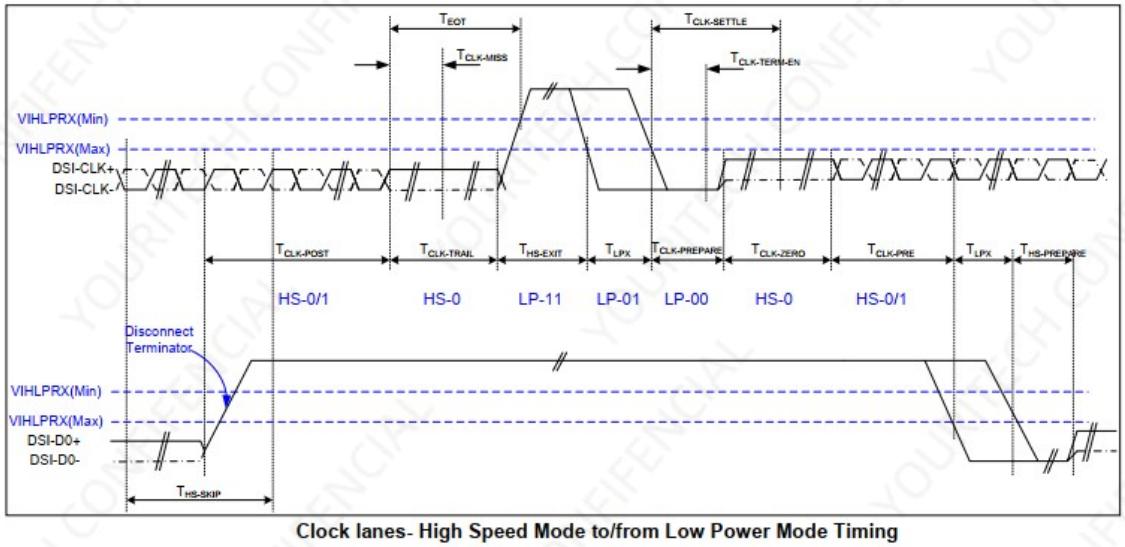
Mipi Interface Low Power Mode Timing Characteristics

DSI Bursts Mode

DSI Bursts Mode



Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing

VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

Reset Description:

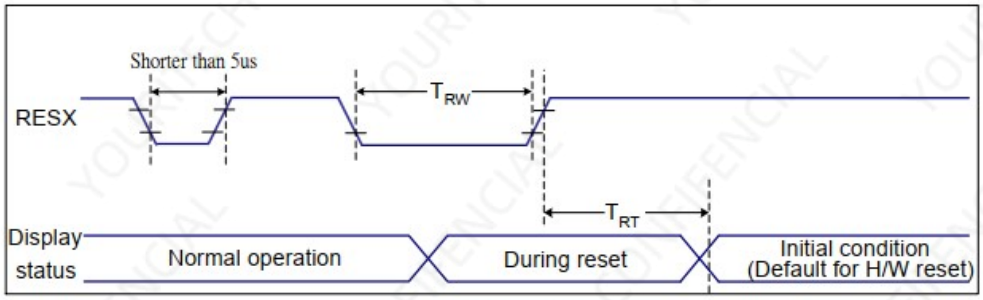


Figure 9 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

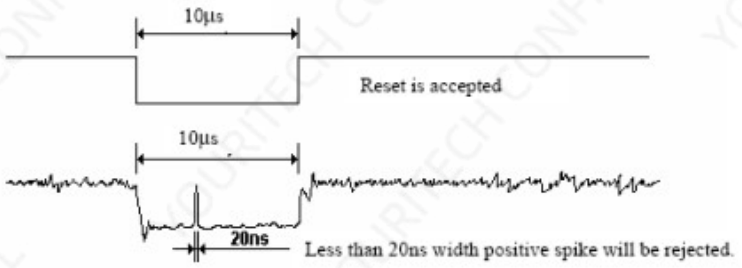
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Optical Specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T (%)	Θ=0 Normal viewing angle	4.5	5.0	—	%	Measuring with normal polarizer，Reference Only Base on Vop=4.5V
Transmittance (without Polarizer)		T (%)		15.21	16.91	—	%	
Contrast Ratio		CR		800	1000	—	—	(1)(2)
Response Time		$T_{R+}T_F$		—	35	45	msec	(1)(3)
Color Gamut	(%)			35	40	—	%	C-light
Color Chromaticity (CIE1931)	White	W_x		-0.02	0.309	+0.02	—	(1)(4) CF glass C-light
		W_y			0.342			
	Red	R_x			0.593		—	
		R_Y			0.322			
	Green	G_x			0.313		—	
		G_Y			0.529			
	Blue	B_x			0.163		—	
		B_Y			0.185			
Viewing Angle	Hor.	Θ_L	CR>10	70	80	—	—	(1)(4) Measuring with normal polarizer，Reference Only
		Θ_R		70	80	—		
	Ver.	Θ_U		70	80	—		
		Θ_D		70	80	—		
Optima View Direction		Free						(5)

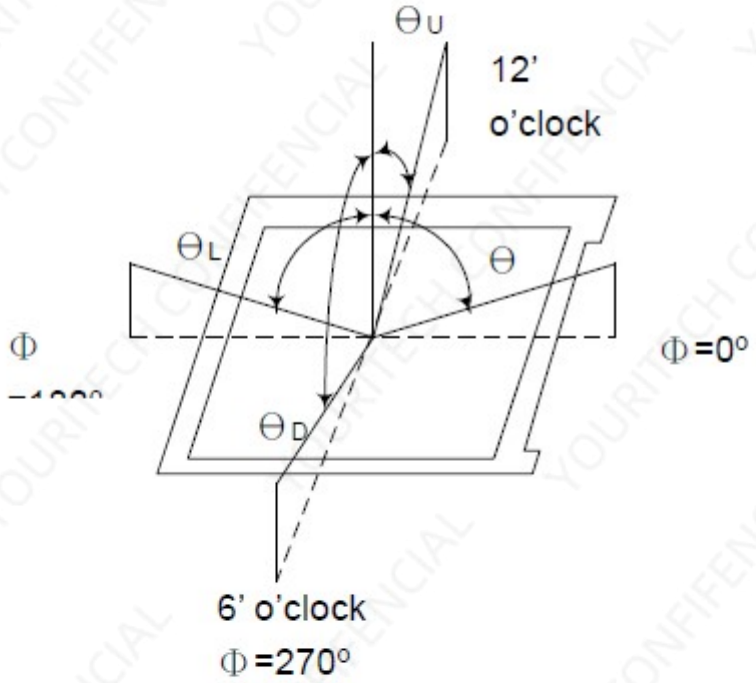
Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : 25±2°C
- 15min. warm-up time.

Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

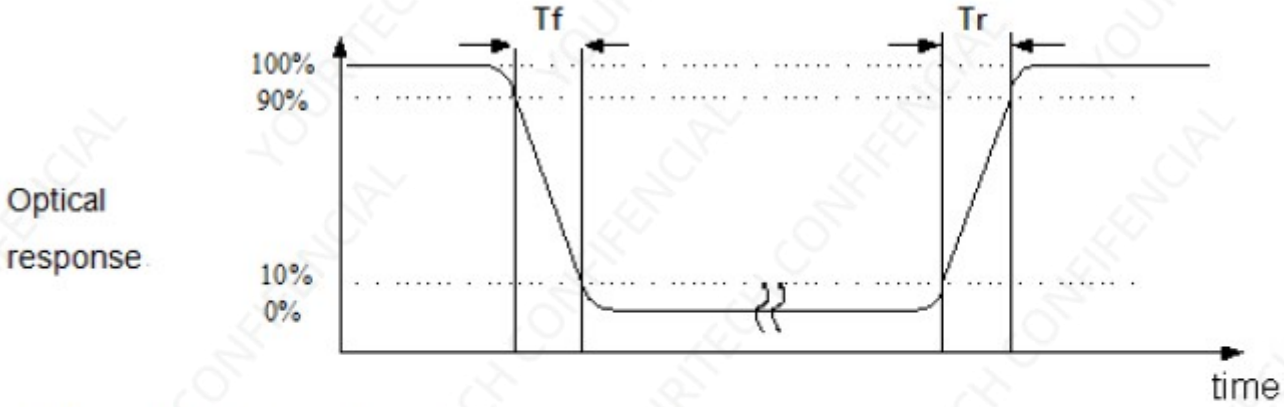
Note (1) Definition of Viewing Angle:



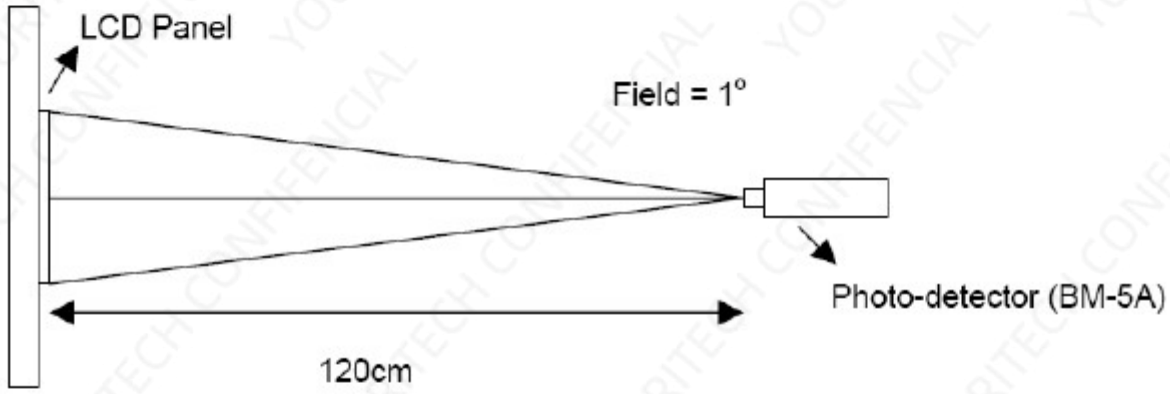
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

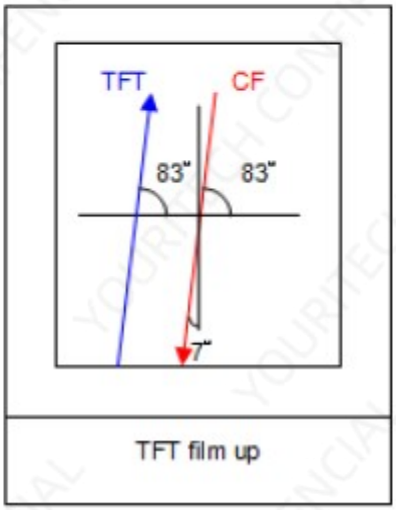
Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.)



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+70°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+60°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state， -20℃（30min） ~60℃（30min），50 cycles	

9. Packing Method----TBD

- END -