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Custom Display

Production Custom designs Installation

Mechanical design



MODEL NO : ET020HV09-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-11-28

☐ Preliminary Specification

☒ Final Product Specification

Customer : _____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 240xRGBx320

As to basic specification of the driver IC, refer to the IC (ST7789T3) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;

ALL O'CLOCK Type LCD

240 dot-segment and 320 dot-common outputs;

65K/262K Color can be selected by software;

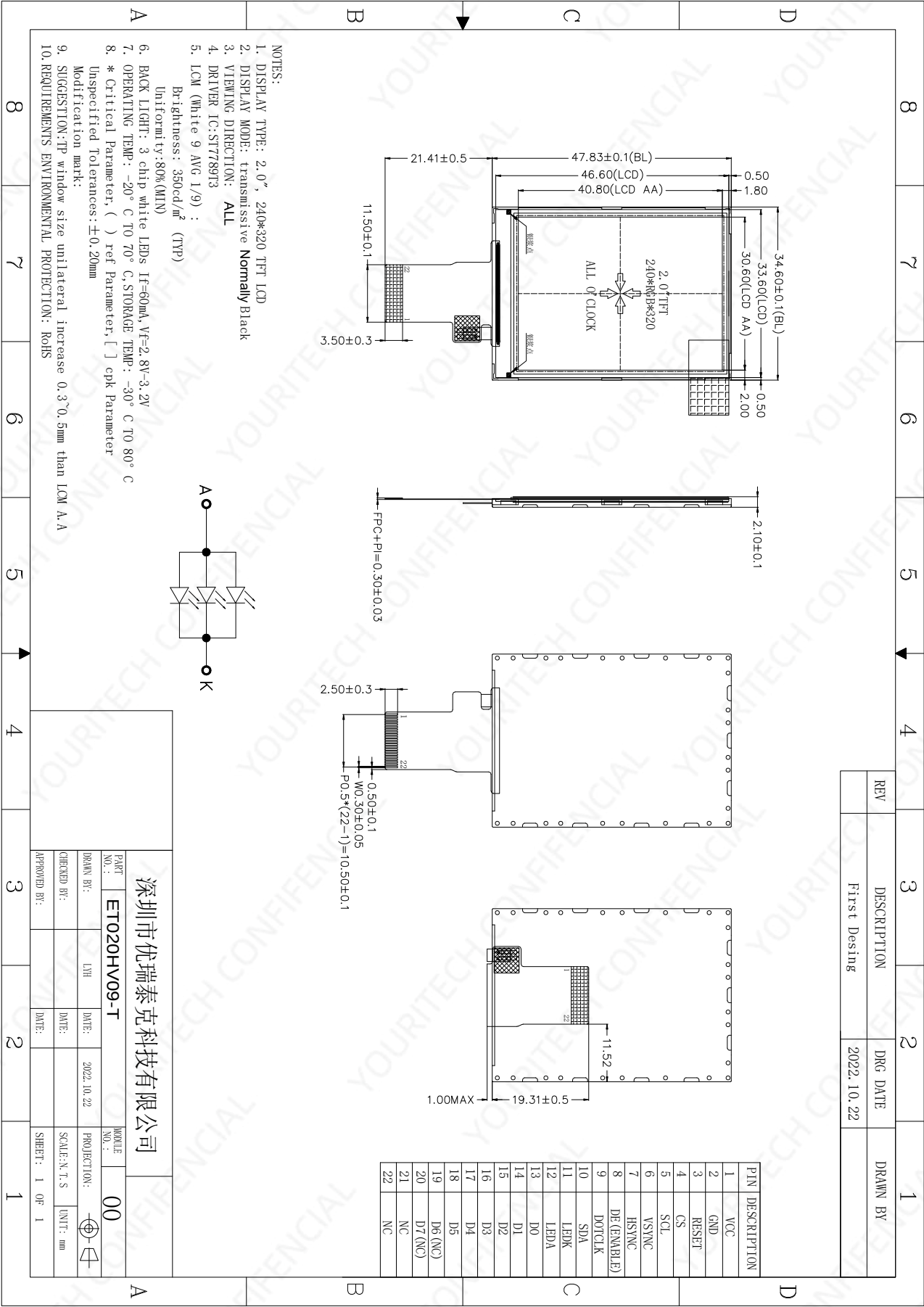
White LED back light;

6bit RGB interface

1.3 Applications:

2. LCM General specification

ITEM	Standard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	240*3RGB(H)X320(V)	Dots
Pixel arrangement	RGB Vertical stripe	--
Pixel Pitch (H*V)	0.1275(H) x0.1275 (V)	mm
Active area	30.60(H) x 40.80(V)	mm
Module Size(W*H*T)	34.60(W)x47.83(H)x2.10(T)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	ST7789T3	--
TFT interface	6bit RGB interface	--
Approx. Weight	TBD	g
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--



3. Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T _{OPR}	-20	+70	°C
LCM Storage Temperature	T _{STG}	-30	+80	°C
Humidity	RH	--	90	%

4. Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	--	--	--	V
Supply Voltage for(DC/DC)	VDD	2.5	2.8	3.3	V
Supply Voltage for(DC/DC)	AVDD	--	--	--	V
Supply Voltage for(DC/DC)	AVEE	--	--	--	V

4.2 Back-Light Unit Characteristics

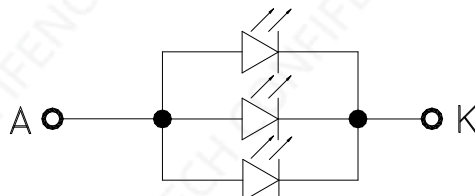
The back-light system is an edge-lighting type with 3 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V _F	5.6	--	6.6	V	--
Forward current	I _F	--	60	--	mA	--
Luminance(With LCD)	L _v	--	350	--	cd/m ²	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

- (1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

5.1 LCM Pin Descriptions

Pin No.	Symbol	Functional	Notes
1	VCC	Power supply 2.5V~3.3V	
2	GND	Power Ground	
3	RESET	Reset signal input terminal. Active at 'L'.	
4	CS	Chip select signal input pin	
5	SCL	Synchronous clock signal pin	
6	HS	Horizontal (Line) synchronizing input signal for RGB interface operation.	
7	VS	Vertical (Frame) synchronizing input signal for RGB interface operation.	
8	DE	Data enable signal for RGB interface operation.	
9	DOTCLK	Dot clock signal for RGB interface operation.	
10	SDA	SPI interface input pin.	
11	LEDK	Power supply for backlight cathode input terminal.	
12	LEDA	Power supply for backlight anode input terminal.	
13-18	D0-D5	RGB interface data bus.	
19	D6(NC)	NC	
20	D7(NC)	NC	
21-22	NC	NC	

6. Timing Characteristics

VDDI and VDD can be applied in any order.

In CABG function application, VDDI power on need delay 5ms after VDD has been supplied.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

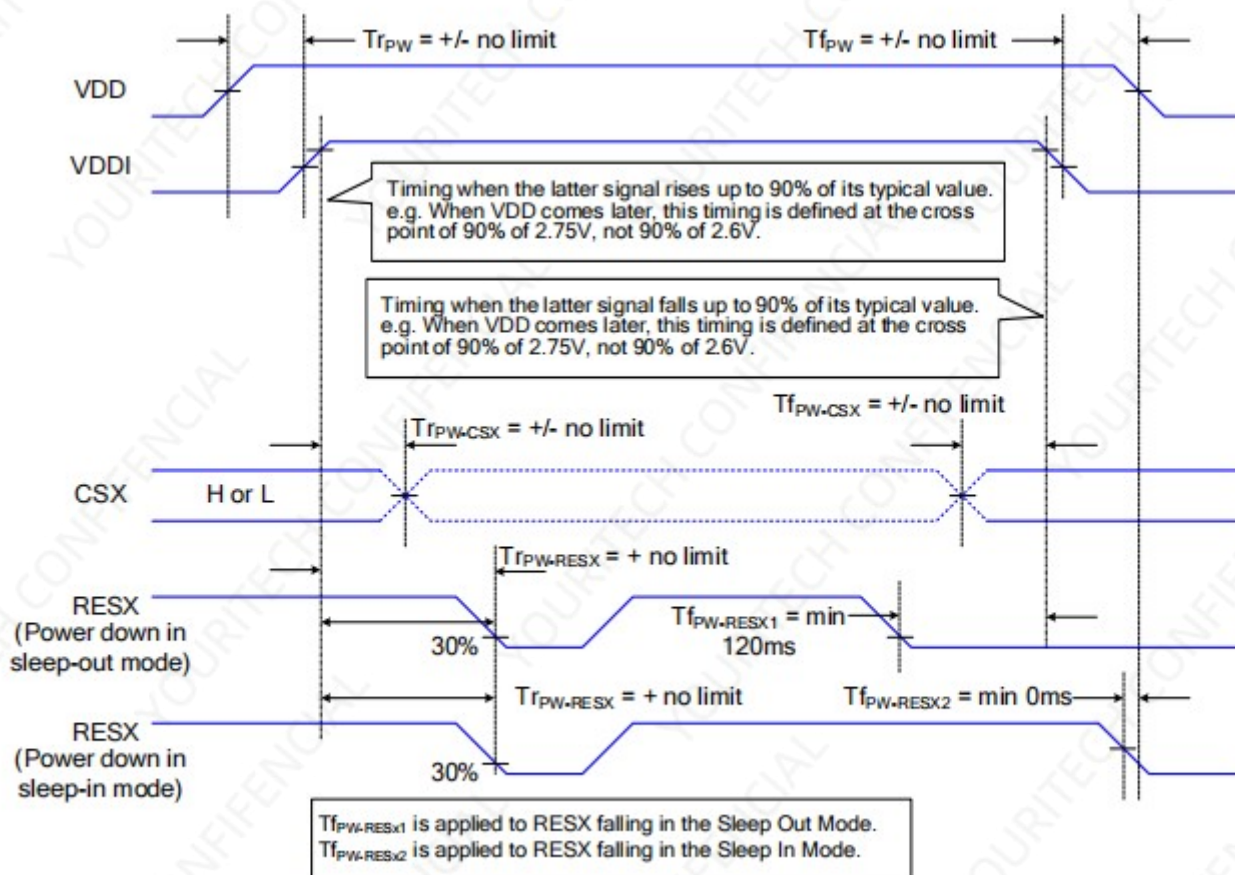
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



RGB Interface Characteristics:

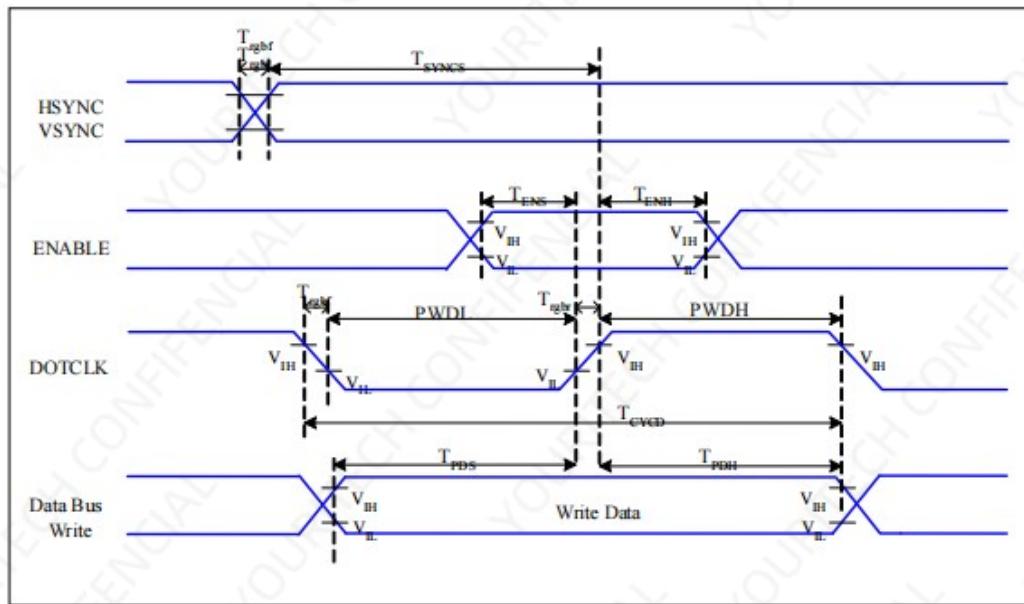


Figure 6 RGB Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25°C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNC}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

Table 7 18/16 Bits RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNC}	VSYNC, HSYNC Setup Time	35	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	35	-	ns	

	T_{ENH}	Enable Hold Time	35	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	35	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	35	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	80	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	10	ns	
DB	T_{PDS}	PD Data Setup Time	35	-	ns	
	T_{PDH}	PD Data Hold Time	35	-	ns	

Table 8 6 Bits RGB Interface Timing Characteristics

Reset Timing:

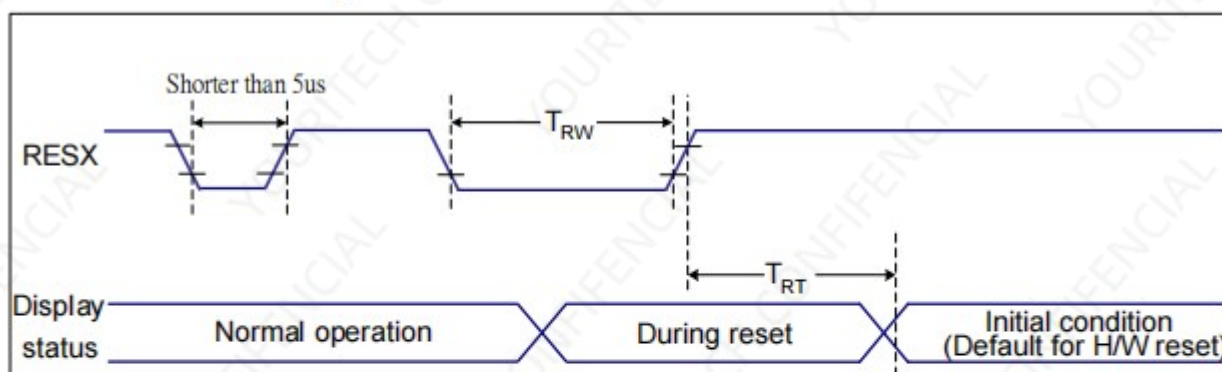


Figure 7 Reset Timing

$VDDI=1.65$ to $3.3V$, $VDD=2.4$ to $3.3V$, $AGND=DGND=0V$, $T_a=25^{\circ}C$

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:

7.Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T(%)	—	—	(4.50)	—	%	Normal POL
Transmittance (without Polarizer)		T(%)	—	—	(12.20)	—	%	
Contrast Ratio		CR	Θ=0 Normal viewing angle	640	800	—	—	(1)(2)
Response Time		T _R + T _F		—	30	40	msec	(1)(3)
Color Gamut		S(%)		54	60	—	%	
Color Chromaticity (CIE1931)	White	W _x		+/-0.02	(0.296)	+/-0.02		(1)(4) CF glass
		W _y			(0.325)			
	Red	R _x			(0.647)			
		R _y			(0.329)			
	Green	G _x			(0.279)			
		G _y			(0.550)			
	Blue	B _x			(0.134)			
		B _y			(0.123)			
Viewing Angle	Hor.	Θ _L	CR>10	—	80	—	Viewing Angle base on using Normal Polarizer , Reference Only	
		Θ _R		—	80	—		
	Ver.	Θ _U		—	80	—		
		Θ _D		—	80	—		
Optima View Direction		ALL						(5)

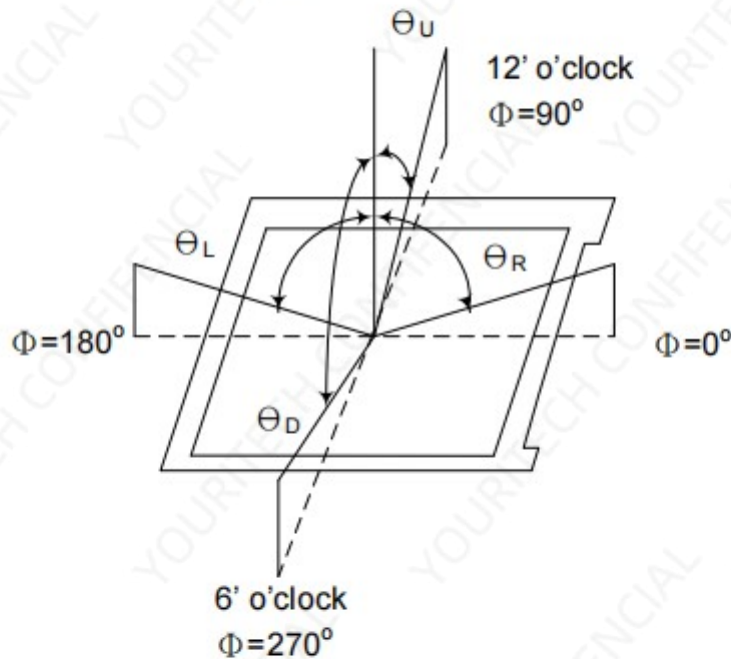
Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : $25 \pm 2^\circ\text{C}$
- 15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1) Definition of Viewing Angle:

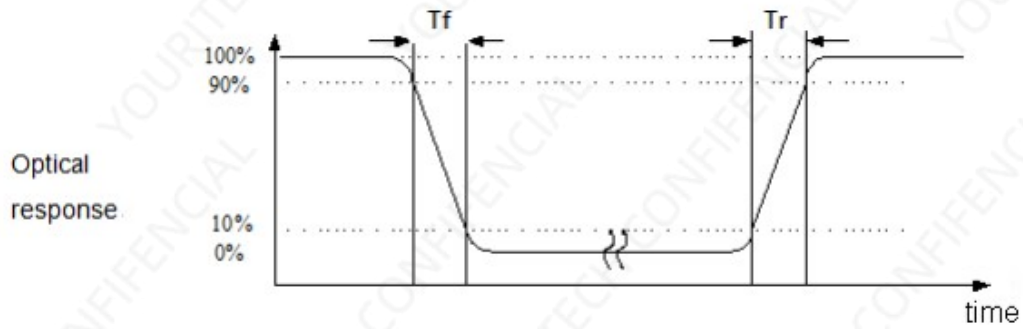


Note (2) Definition of Contrast Ratio (CR):

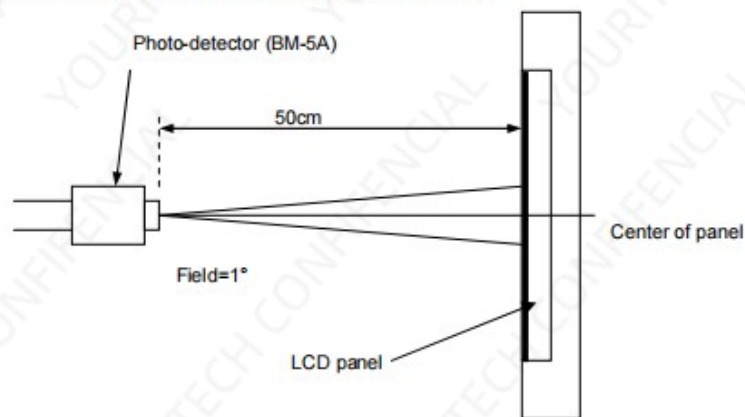
measured at the center point of panel

$$\text{CR} = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

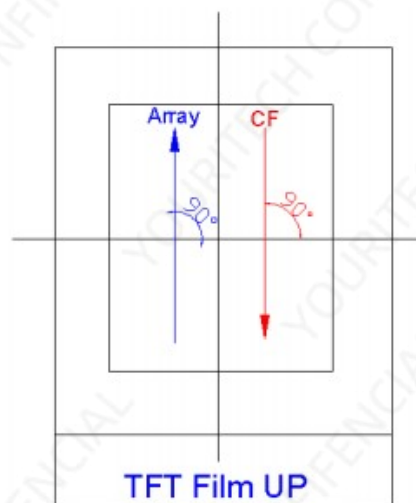
Note (3) Definition of Response Time: Sum of T_R and T_F



Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.)



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test is OK. Missing Segment, short, unclear segment non-display, display abnormally and liquid crystal leakage un-allowed. 2. No low temperature bubbles, end seal loose and fall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Temp. Operating	+70°C / 96H	
4	Low Temp. Operating	-20°C / 96H	
5	High Temperature / Humidity storage	50°C x 90%RH / 96H	
6	Thermal and cold shock	Static state, -20°C (30min) ~60°C (30min), 50 cycles	

9. Packing Method----TBD

- END -