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Project No. 项目编号	ET021WV02-T
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	Standard LCD Module TFT: 480*RGBx480Dots 2.1" TFT LCD

客户确认Customer Approval	
项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	



1. Introduction

1.1 Scope of application

This specification applies to the LCD module that is supplied by YOURITECH TECHNOLOGY

LCD specification: Dots 480xRGBx480

As to basic specification of the driver IC, refer to the IC (Sitronix: ST7701S) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;

ALL Viewing Type LCD

480 dot-segment and 480 dot-common outputs;

16.7M Color can be selected by software;

White LED back light;

2lane MIPI interface

1.3 Applications:



2. LCM General specification

ITEM	Standard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	480*3RGB(H)X480(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.111(H) × 0.111(V)	mm
Active area	53.28(H) x 53.28(V)	mm
Viewing direction	ALL Viewing	-
TFT Driver IC	ST7701S	
TFT interface	2lane MIPI Interface	-
Approx. Weight	TBD	g
Module Size(W*H*T)	56.18(W) ×59.71(H) ×2.20(T)	mm
Touch structure	--	
Touch Driver IC	--	-
Touch Interface	--	





3. Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T _{OPR}	-20	+60	°C
LCM Storage Temperature	T _{STG}	-30	+70	°C
Humidity	RH	-	90	%

4. Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	IOVCC	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VCC	2.6	2.8	3.6	V
Supply Voltage for(DC/DC)	AVDD				V
Supply Voltage for(DC/DC)	AVEE				V

4.2 Back-Light Unit Characteristics

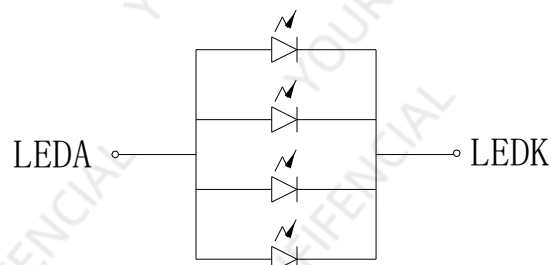
The back-light system is an edge-lighting type with 4 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V _F	2.8		3.2	V	-
Forward current	I _F	--	80	-	mA	-
Luminance(With LCD+CTP)	L _v		TBD	--	cd/m ²	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

- (1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	LCM Functional	Notes
1	LEDA	Power supply for backlight anode input terminal.	
2	LEDK	Power supply for backlight cathode input terminal.	
3	LEDK	Power supply for backlight cathode input terminal.	
4	VC1	Power supply : 2.6V ~ 3.6V	
5	IOVCC	I/O Power supply : 1.65V ~ 3.3V	
6	RESET	Reset signal input terminal. Active at 'L'.	
7	TE	Tearing effect output pin is used to synchronize MCU frame writing,	
8	PWM	LCD backlight control PWM output pin.	
9	GND	Power Ground	
10	MIPI_0P	MIPI-DSI clock data Lane 0 positive-end input/output pin.	
11	MIPI_0N	MIPI-DSI clock data Lane 0 negative-end input/output pin.	
12	GND	Power Ground	
13	MIPI_1P	MIPI-DSI clock data Lane 1 positive-end input/output pin.	
14	MIPI_1N	MIPI-DSI clock data Lane 1 negative-end input/output pin.	
15	GND	Power Ground	
16	MIPI_CKP	MIPI-DSI clock data Lane positive-end input pin.	
17	MIPI_CKN	MIPI-DSI clock data Lane negative-end input pin.	
18	GND	Power Ground	
19	NC	NC	
20	NC	NC	
21	GND	Power Ground	
22	NC	NC	
23	NC	NC	
24	GND	Power Ground	
25	CTP_INT	Touch panel interrupt output	
26	CTP_SDA	Touch panel I2C data	
27	CTP_SCL	Touch panel I2C clock	
28	CTP_RST	Touch panel reset	
29	CTP_VCI	Touch panel Power supply 2.8~3.3V	
30	GND	Power Ground	



6. Timing Characteristics

POWER ON/OFF SEQUENCE

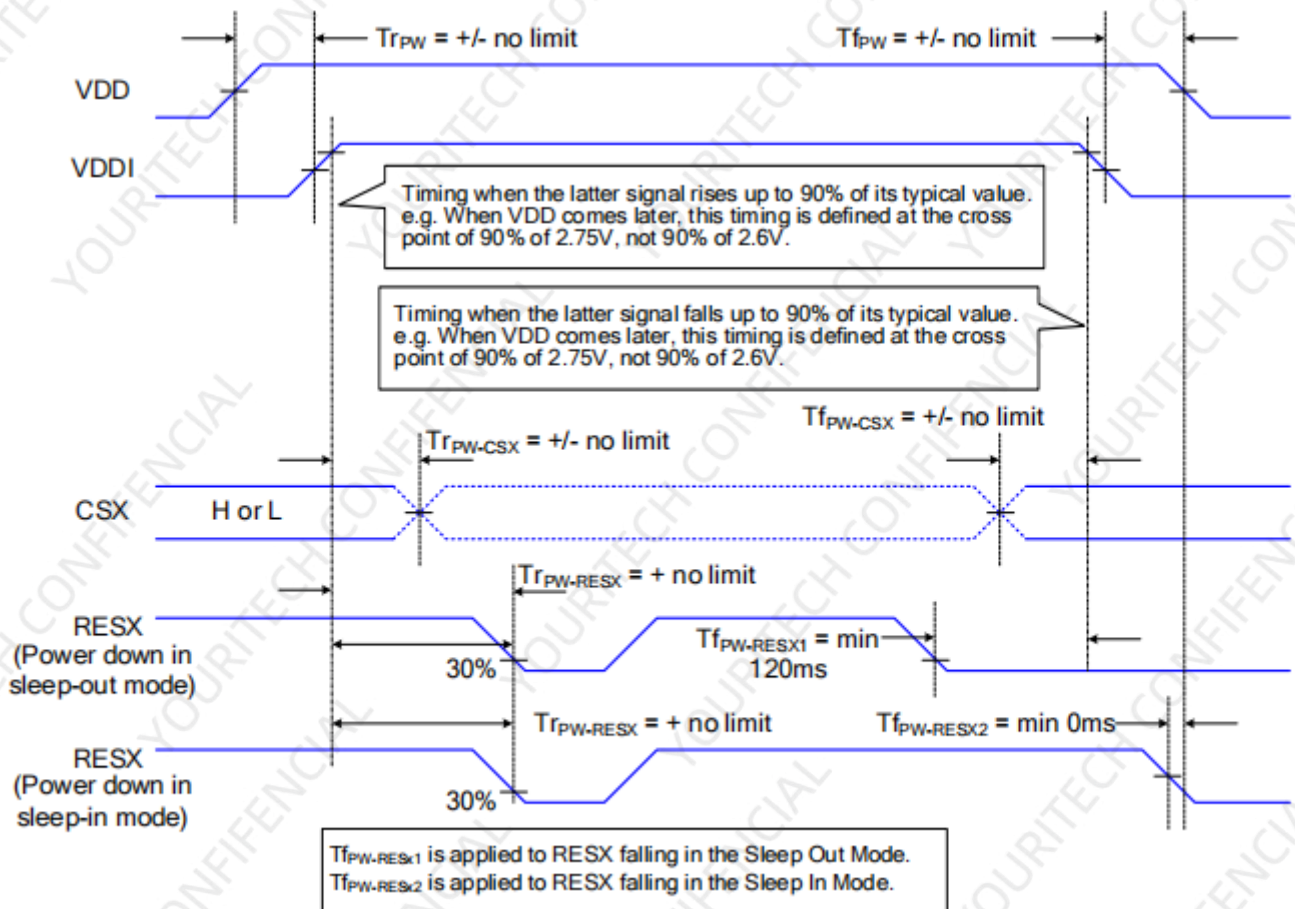
VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released.

CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

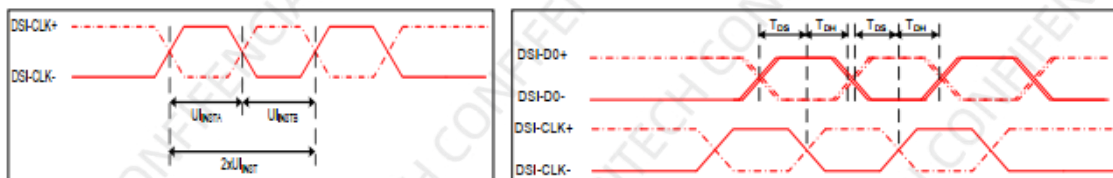
Notes:

1. There will be no damage to the ST7701S if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

The power on/off sequence is illustrated below



DSI-MIPI Interface Timing Characteristics of IC High Speed Mode



DSI clock channel timing

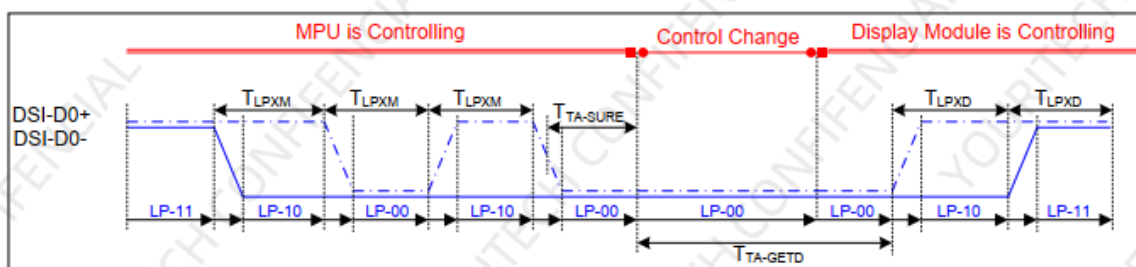
Rising and falling time on clock and data channel

$V_{DDI}=1.8, V_{DD}=2.8, AGND=DGND=0V, T_a=25^{\circ}C$

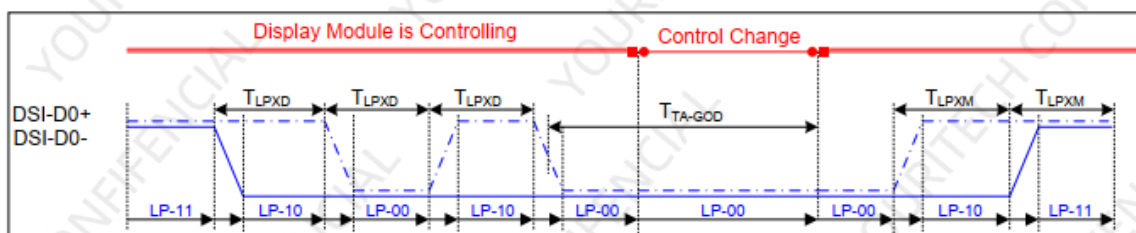
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xU_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	U_{INSTA} U_{INSTB}	UI instantaneous halves	2	12.5	ns	$UI = U_{INSTA} = U_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Mipi Interface- High Speed Mode Timing Characteristics

Low Power Mode



Bus Turnaround (BTA) from display module to MPU Timing



Bus Turnaround (BTA) from MPU to display module Timing



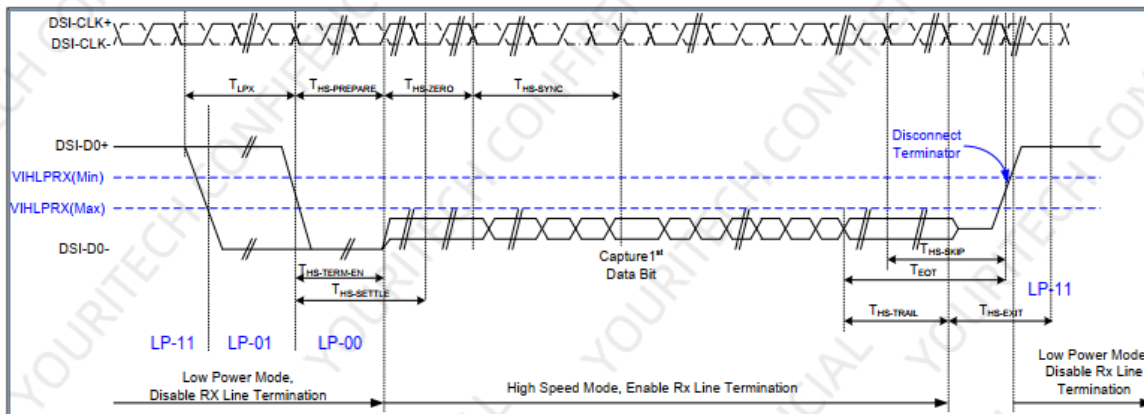
$V_{DDI}=1.8, V_{DD}=2.8, A_{GND}=DGND=0V, T_a=25^\circ C$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2 \times T_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5 \times T_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4 \times T_{LPXD}$		ns	Output

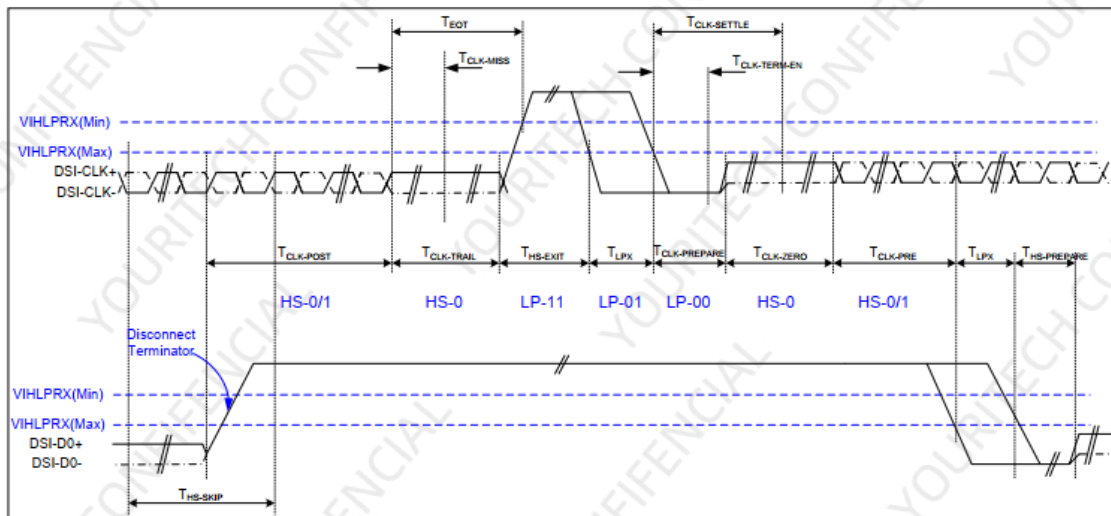
Mipi Interface Low Power Mode Timing Characteristics

DSI Bursts Mode

DSI Bursts Mode



Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing



VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25 °C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	-	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105ns+12 UI	ns	Input



Reset Description:

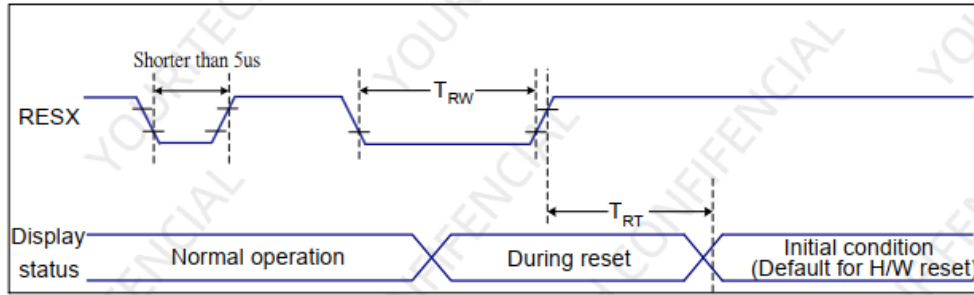


Figure 9 Reset Timing

VDDI=1.8, VDD=2.8, AGND=DGND=0V, $T_a=25^\circ\text{C}$

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5) 120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

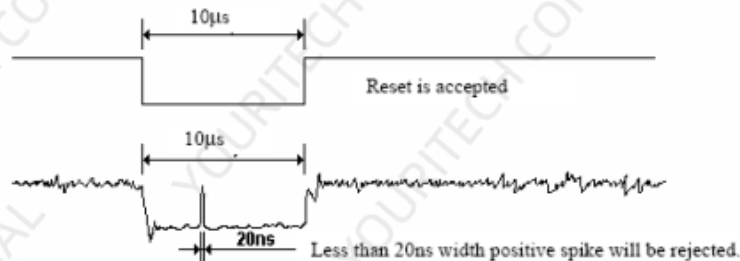
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.



7.Optical Characteristics

Optical Specification

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle	Horizontal	Θ3	CR> 10	80	85		°	Note 1
		Θ9		80	85		°	
	Vertical	Θ12		80	85		°	
		Θ6		80	85		°	
Contrast Ratio		CR	Θ= 0°	800:1	1000:1			Note 2
Transmittance		T(%)	Θ= 0°	3.6	4.0			Note 3
NTSC		%	Θ= 0°	64	69			
Reproduction Of color	Red	Rx	Θ= 0°	0.640	0.655	0.670		Note 4 *Color filter Glass With OC
		Ry		0.312	0.327	0.342		
	Green	Gx		0.269	0.284	0.299		
		Gy		0.579	0.594	0.609		
	Blue	Bx		0.123	0.138	0.153		
		By		0.096	0.111	0.126		
White		Wx	Θ= 0°	0.285	0.300	0.315		
		Wy		0.311	0.326	0.341		
Response Time		Tr+Tf	Θ= 0°		30	35	ms	Note 5

Note:

- Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIG.1).
- Contrast measurements shall be made at viewing angle of $\Theta = 0^\circ$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIG. 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

- Transmittance is the value without APF Pol.
- The color chromaticity coordinates specified in Table1 shall be calculated from



The spectral data measured with all pixels first in red, green, blue and white.

Measurements shall be made at the center of the C/F.

Measurement condition is C - light source & Halogen Lamp

5. The electro-optical response time measurements shall be made as FIG.2 by switching the "data" input signal ON and OFF.

The times needed for the luminance to change from 10% to 90% is T_r , and 90% to 10% is T_f .

Figure 1. Measurement Set Up

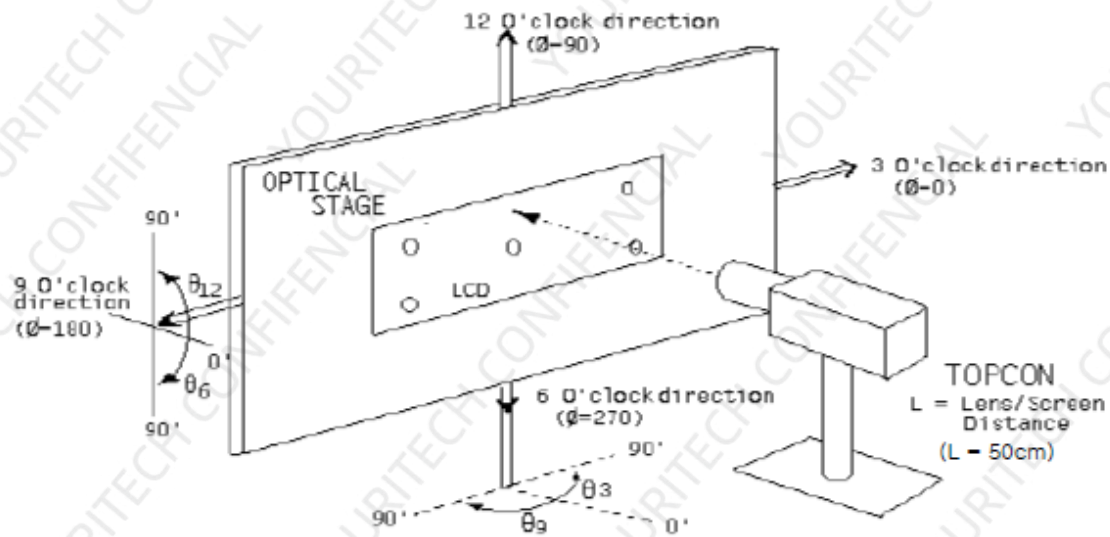
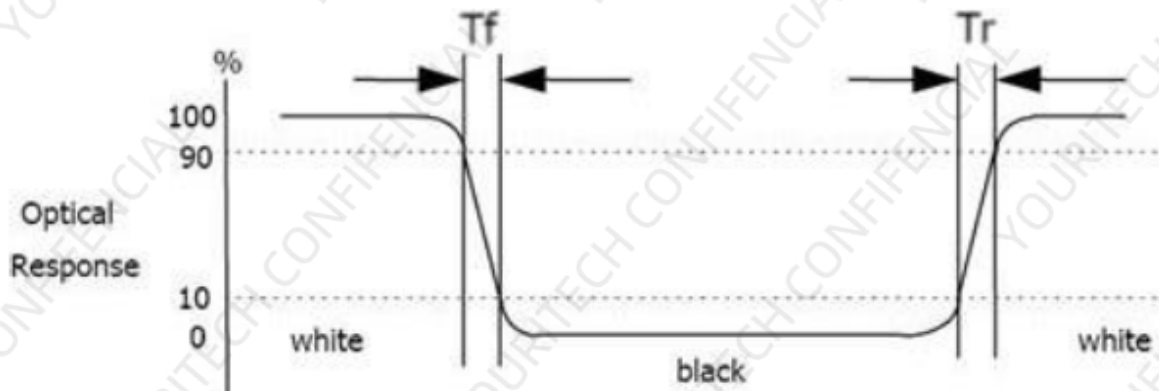


Figure 2. Response Time Testing



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+70°C / 96H	1. Functional test is OK. Missing Segment, short, unclear segment non-display, display abnormally and liquid crystal leakage un-allowed. 2. No low temperature bubbles, end seal loose and fall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Temp. Operating	+60°C / 96H	
4	Low Temp. Operating	-20°C / 96H	
5	High Temperature / Humidity storage	50°C x 90%RH / 96H	
6	Thermal and cold shock	Static state, -20°C (30min) ~60°C (30min), 50 cycles	

9. Packing Method----TBD

- END -

