YOURITech
AN EUROTECH COMPANY

INDUSTRIAL STRENGTH...
Start Your Application From YOURITECH

Integration support
Obsolescence Management
PCAP
Embedded Systems
Human Machine Interface
Touch Solutions
Production
Custom designs
Installation
Software
Mechanical design
Quality Management
Open Frame Monitors
LCD Controller
Research & Development
Firmware
EMC tests
on-site service
In-house Manufacturing
Optical Bonding
Cover glass
System solutions
OEM Solutions
Custom Display

Erotech YOURITech AN EUROTECH COMPANY AOSHITE 奥视特 Your Reliable Display Panel and Smart Touch Embedded Solution Partner

For more information about comprehensive display panels and touch embedded solutions, welcome contact us at:

https://www.youritech.com
info@youritech.com

MODEL NO : ET024QV12-TT

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-11-29

□Preliminary Specification

■Final Product Specification

Customer :_____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 480xRGBx640
As to basic specification of the driver IC, refer to the IC (ST7701SN) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

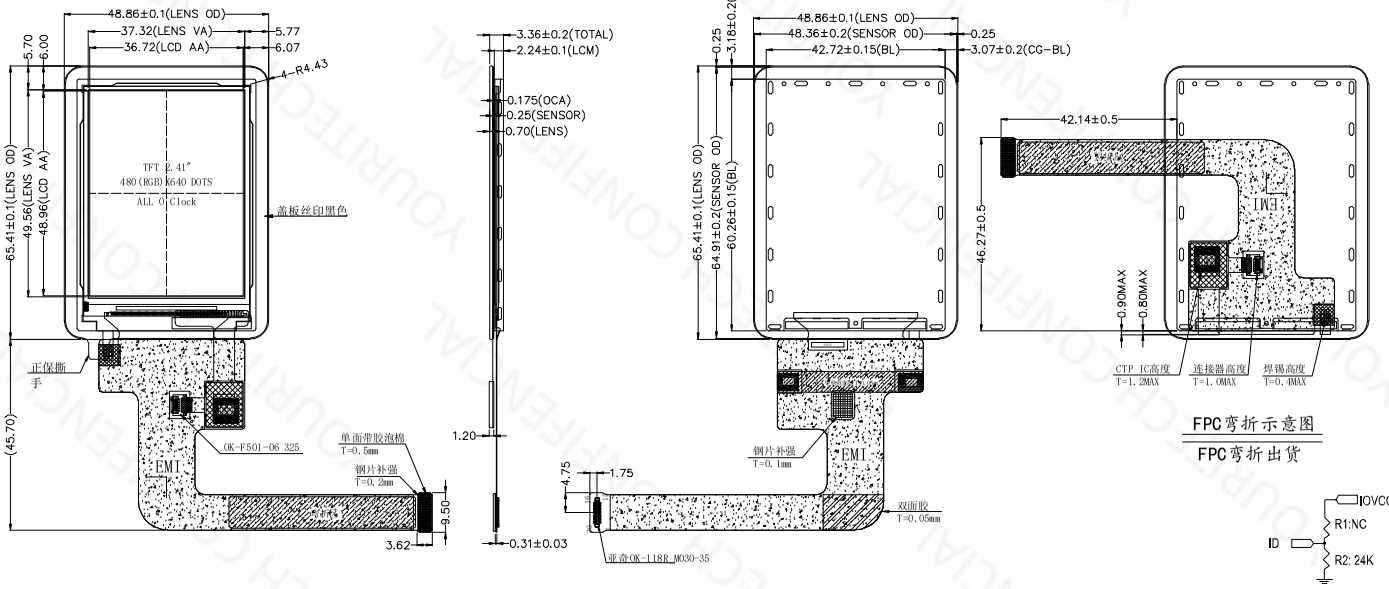
Structure: TFT PANNEL+IC +FPC1+BL+CTP;
ALL O'CLOCK Type LCD
480 dot-segment and 640 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
2lane MIPI interface

1.3 Applications:

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	480*3RGB(H)X640(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.0765 (H) x 0.0765 (V)	mm
Active area	36.72(H) x 48.96(V)	mm
Viewing direction	ALL O'CLOCK	-
TFT Driver IC	ST7701SN	
TFT interface	2lane MIPI Interface	-
LCM Size(W*H*T)	42.72(W) ×60.26(H) ×2.24(T)	mm
LCM+CTP Size(W*H*T)	48.86(W) ×65.41(H) ×3.36(T)	mm
Approx. Weight	TBD	g
Touch structure	G+F	
Touch Driver IC	GHSC6540	
Touch Interface	I2C	

REV	DESCRIPTION	DRG DATE	DRAWN BY
	First Desing	2022.10.26	

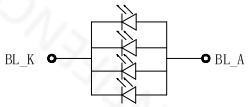


FPC弯折示意图
FPC弯折出货

LCM-PIN

PIN NO	DEFINATION
1	GND
2	LEDK
3	LEDA
4	GND
5	IOVCC 1.8V
6	VCI 2.8V
7	GND
8	CLKP
9	CLKN
10	GND
11	DOP
12	DON
13	GND
14	DIP
15	DIN
16	GND
17	GND
18	TP_RST
19	TP_INT
20	TP_SDA
21	TP_SCL
22	TP_VDD2.8V
23	GND
24	GND
25	TE
26	RESET
27	GND
28	GND
29	NC
30	ID

NOTES:
1. DISPLAY TYPE: 2.41", 480*640 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL O'Clock
4. DRIVER IC:ST7701SN
5. LCM (White 9 AVG 1/9) :
   Brightness: 450cd/m² (TYP)
   Uniformity:80%(MIN)
6. BACK LIGHT: 4 chip white LEDs If=80mA,Vf=2.8V~3.2V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS



BACKLIGHT CIRCUIT

CTP 技术参数:
1、结构G+F: Cover Glass+OCA+ITO FILM+FPC,Cover Glass:0.7MM, OCA:0.125mm, ITO FILM:0.125mm,总厚度: 0.95±0.1mm;
2、IC型号: CHSC6540(COF), 支持单点+手势触摸,工作电压:2.8V, FPC接口线为IIC标准接口, IO电压: 1.8V; 座标原点: 左上角。
3、透光率: ≥85%;TP分辨率: 480*640;
4、工作温湿度范围:-20℃~+70℃,≤90%RH;
储存温湿度范围:-30℃~+80℃,≤90%RH;
5、表面硬度: ≥6H (750gf/铅笔硬度测试) ;
6、Cover Glass材质: (旭硝子) 钢化玻璃,产品符合RoHS标准;
8、其他未标注公差:±0.15;✛为重点管控尺寸

TP-PIN

Pin	Definition
1	GND
2	TP_VDD
3	TP_IIC_SCL
4	TP_IIC_SDA
5	TP_INT
6	TP_RESET

深圳市优瑞泰克科技有限公司

PART NO.:	ET024QV12-TT			MODULE NO.:	00
DRAWN BY:	LIU	DATE:		PROJECTION:	
CHECKED BY:		DATE:		SCALE: N.T.S	UNIT: mm
APPROVED BY:		DATE:		SHEET: 1 OF 1	

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
TP Operating Temperature & Humidity (20%～90%RH)	T_{OPR}	-20	+70	°C
TP SStorage Temperature & Humidity (20%～90%RH)	T_{STG}	-30	+80	°C
Humidity	RH	-	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VCCIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VCC	2.5	2.8	3.3	V
Supply Voltage for(DC/DC)	AVDD				V
Supply Voltage for(DC/DC)	AVEE				V

4.2 Back-Light Unit Characeristics

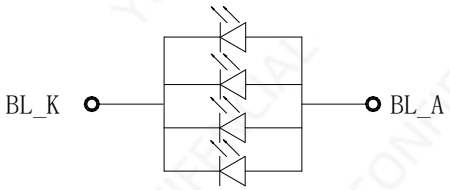
The back-light system is an edge-lighting type with 4 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	2.8		3.2	V	-
Forward current	I_F	--	80	-	mA	-
Luminance(With LCD+CTP)	Lv		450	--	cd/m^2	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	Functional	Notes
1	GND	Power Ground	
2	LEDK	Power supply for backlight cathode input terminal.	
3	LEDA	Power Supply For LED Backlight Anode Input.	
4	GND	Power Ground	
5	IOVCC 1.8V	Power Supply For I/O.	
6	VCI 2.8V	Power Supply For LCD.	
7	GND	Power Ground	
8	CLKP	Positive polarity of low voltage differential clock signal	
9	CLKN	Negative polarity of low voltage differential clock signal	
10	GND	Power Ground	
11	D0P	Positive polarity of low voltage differential data 1 signal	
12	D0N	Negative polarity of low voltage differential data 1 signal	
13	GND	Power Ground	
14	D1P	Positive polarity of low voltage differential data 1 signal	
15	D1N	Negative polarity of low voltage differential data 1 signal	
16-17	GND	Power Ground	
18	CTP_RST 1.8V	Touch panel reset	
19	CTP_INT 1.8V	Touch panel interrupt output	
20	CTP_SDA 1.8V	Touch panel I2C data	
21	CTP_SCL 1.8V	Touch panel I2C clock	
22	CTP_VCC 2.8V	Touch panel Power supply 2.8~3.3V	
23-24	GND	Power Ground	
25	TE	Frame head pulse for tearing effect.	
26	RESET	Reset signal input terminal. Active at ‘L’.	
27-28	GND	Power Ground	
29	NC	NC	
30	ID	ID read PIN for ID circuit.	

6. Timing Characteristics

POWER ON/OFF SEQUENCE

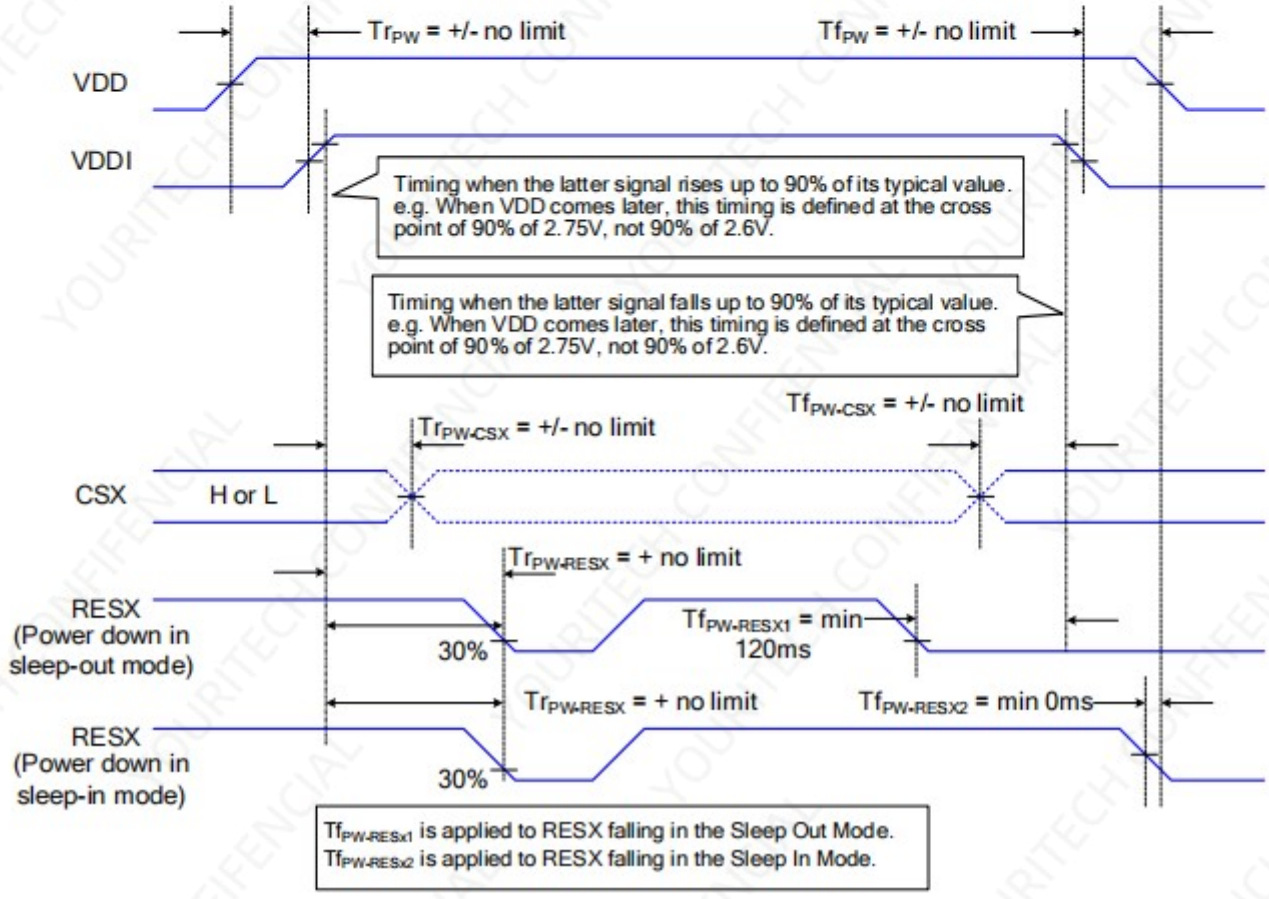
VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released.

CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

Notes:

1. There will be no damage to the ST7701SN if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

The power on/off sequence is illustrated below



Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until "Power On Sequence" powers it up.

MIPI Interface Characteristics:

High Speed Mode

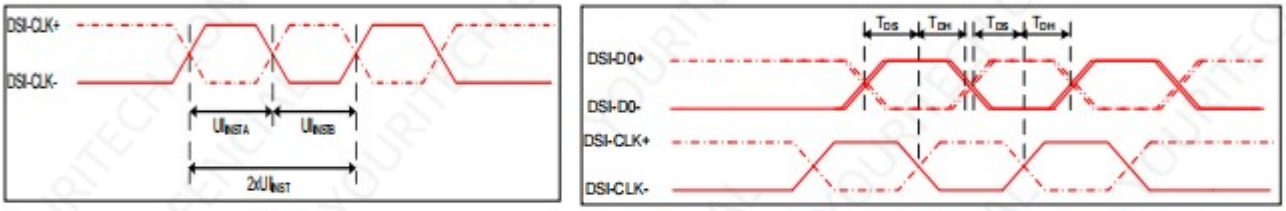


Figure 4 DSI clock channel timing

Figure 5 Rising and falling time on clock and data channel

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	2.5	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	1.25	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Table 7 Mipi Interface- High Speed Mode Timing Characteristics

Lowe Power Mode

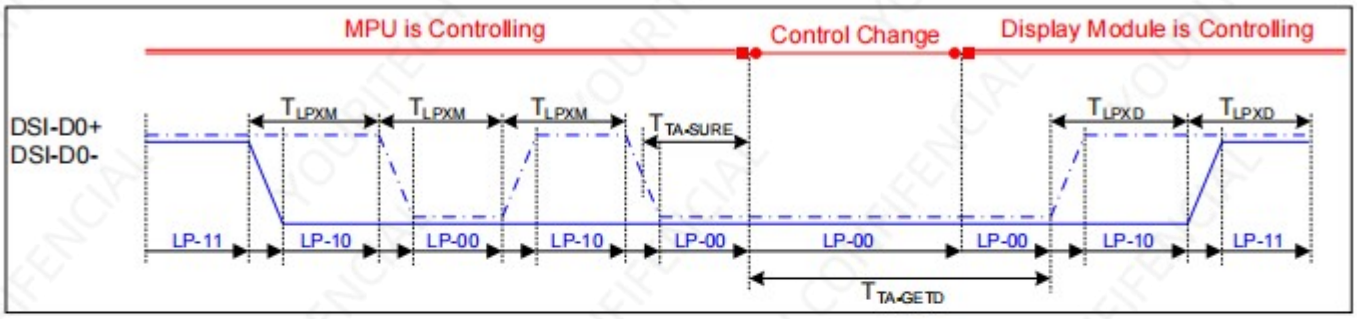


Figure 6 Bus Turnaround (BTA) from display module to MPU Timing

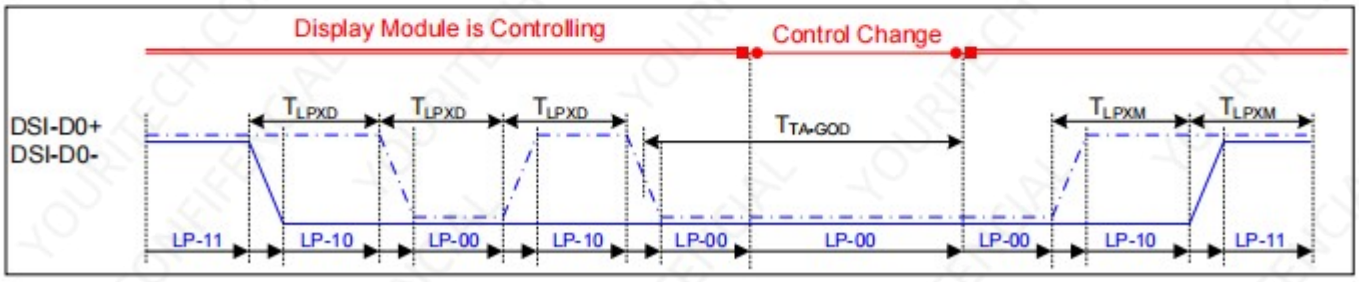


Figure 7 Bus Turnaround (BTA) from MPU to display module Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

Table 8 Mipi Interface Low Power Mode Timing Characteristics

DSI Bursts Mode

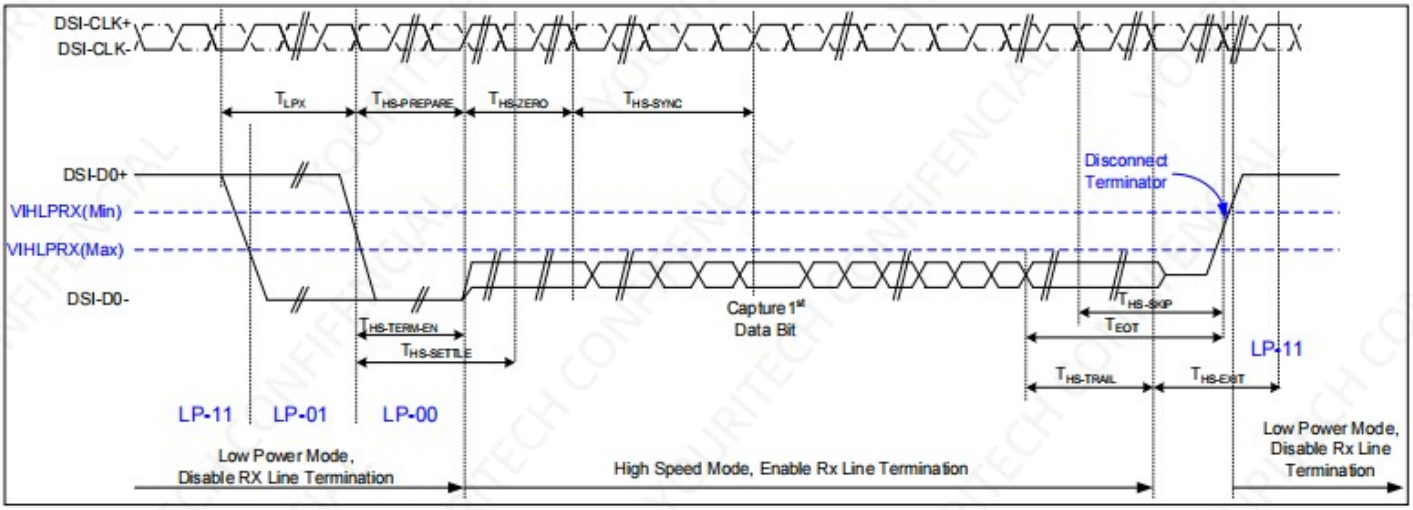


Figure 7 Data lanes-Low Power Mode to/from High Speed Mode Timing

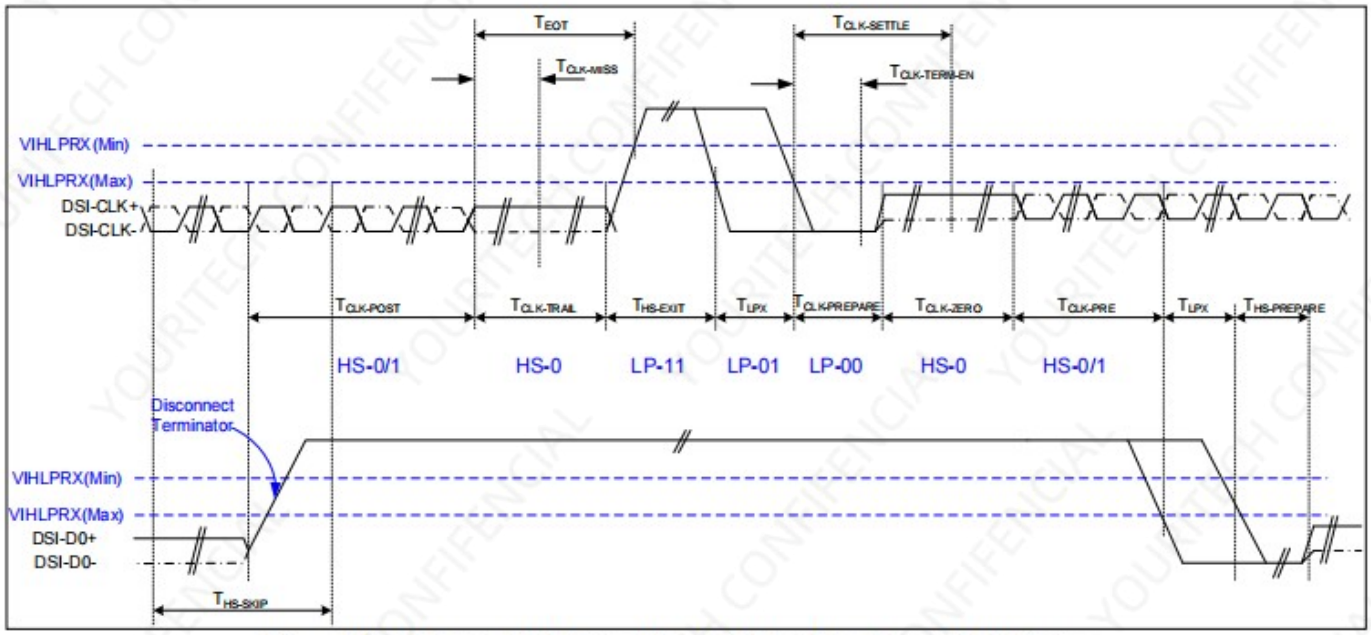


Figure 8 Clock lanes- High Speed Mode to/from Low Power Mode Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

Reset Description:

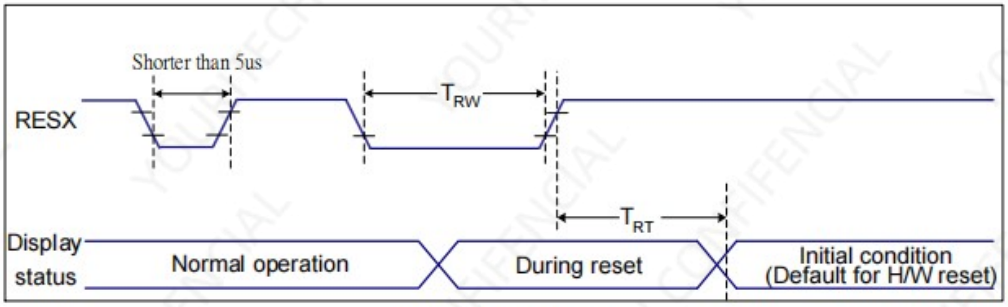


Figure 9 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

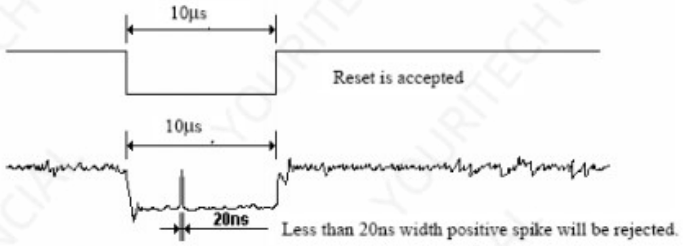
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Optical Specification

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Threshold Voltage		Vsat		4.1	4.3	4.5	V	Fig.1
		Vth		1.6	1.8	2.0	V	
Viewing Angle	Horizontal	Θ3	CR>10	70	80			Note 1
		Θ9		70	80			
	Vertical	Θ12		70	80			
		Θ6		70	80			
Contrast Ratio		CR	Θ= 0°	800	1000			Note 2
Transmittance		T(%)	Θ= 0°	3.2	3.6			Note 3
NTSC		%	Θ= 0°	58	63			Only CF
Reproduction Of color	Red	Rx	Θ= 0°	0.625	0.640	0.655		Note 4 *Color filter Glass (with OC)
		Ry		0.311	0.326	0.341		
	Green	Gx		0.279	0.294	0.309		
		Gy		0.565	0.580	0.595		
	Blue	Bx		0.134	0.149	0.164		
		By		0.090	0.105	0.120		
White		Wx	Θ= 0°	0.287	0.302	0.317		
		Wy		0.314	0.329	0.344		
Response Time		Tr+Tf	Θ= 0°		35	40	ms	Note 5

Note:

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIG.2).
2. Contrast measurements shall be made at viewing angle of Θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIG. 2) Luminance Contrast Ratio (CR) is defined mathematically.

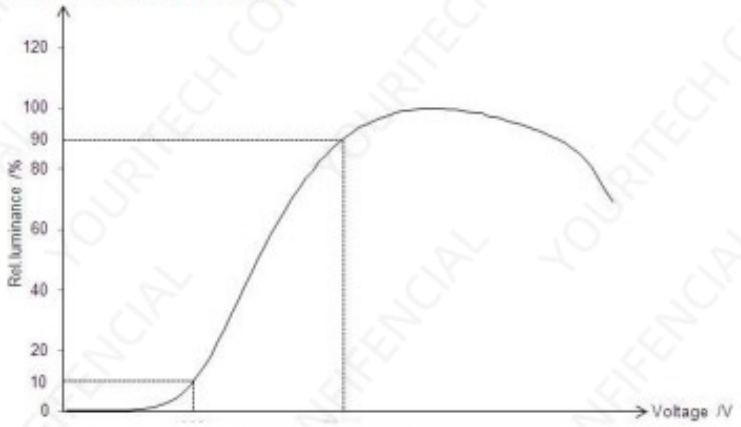
$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the value with APF Polarizer.

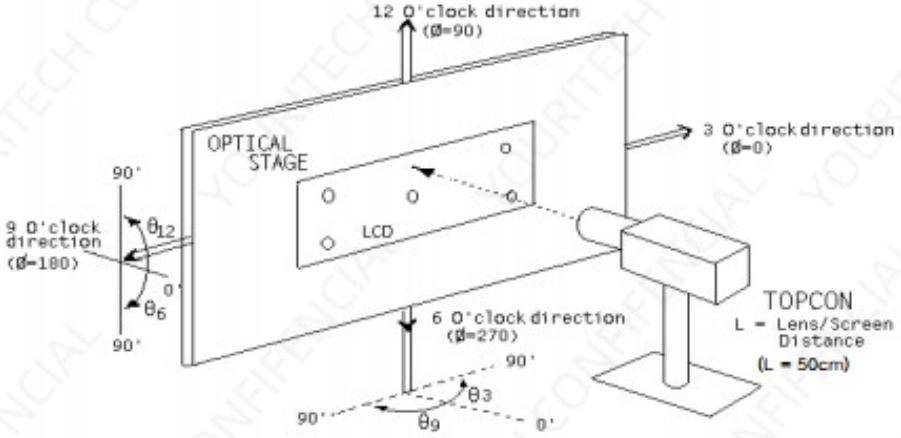
4. The color chromaticity coordinates specified in Table1 shall be calculated from
The spectral data measured with all pixels first in red, green, blue and white.
Measurements shall be made at the center of the C/F.
Measurement condition is C - light source & Halogen Lamp

5. The electro-optical response time measurements shall be made as FIG.3 by switching the "data" input signal ON and OFF.
The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

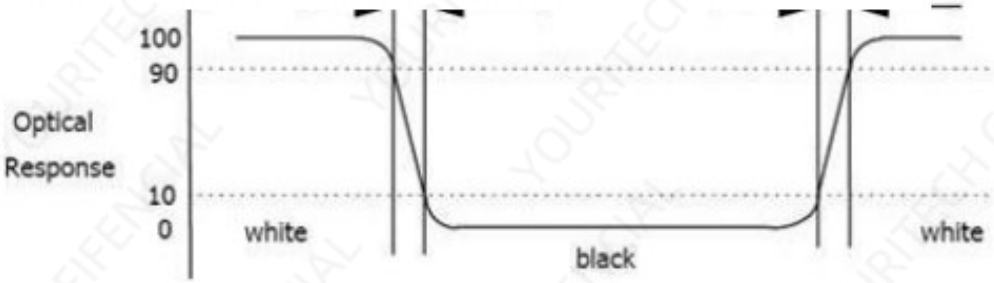
Figure 1. The definition of Vth & Vsat



Figur



Figur



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state， -20℃（30min） ~60℃（30min），50 cycles	

9. Packing Method----TBD

- END -