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SPECIFICATION FOR LCM+CTP Module

MODULE No:	ET024QV21-KT
CUSTOMER:	

YOURITECH	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
2020.10.13	V1.0	ALL	FIRST ISSUE

Contents

1.Basic Specifications

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorpho us silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Pan el, driver circuit,capacitance touch panel,back-light unit. The resolution of a 2.41 " TFT-LCD contains 480x640 pixels, and can display up to 65K/262K/16.7M colors.

1.1 TFT Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	36.72(H)*48.96(V)(2.41 ")	mm	
Driver element	TFT active matrix	-	
Display colors	65K/262K/16.7M	colors	
Number of pixels	480(RGB)*640	dots	
Pixel arrangement	RGB Vertical stripe	-	
Pixel pitch	0.0765(H)*0.0765(V)	mm	
Viewing angle	Free	o'clock	
Controller IC	ST7701SI	-	
LCM Interface	SPI+16/18/24 BIT RGB	-	
Display mode	Transmissive /Normally Black	-	
Operating temperature	-30 ~ +80	℃	
Storage temperature	-30 ~ +80	℃	
Module bonding technology	Optical bonding between LCM and CTP	-	

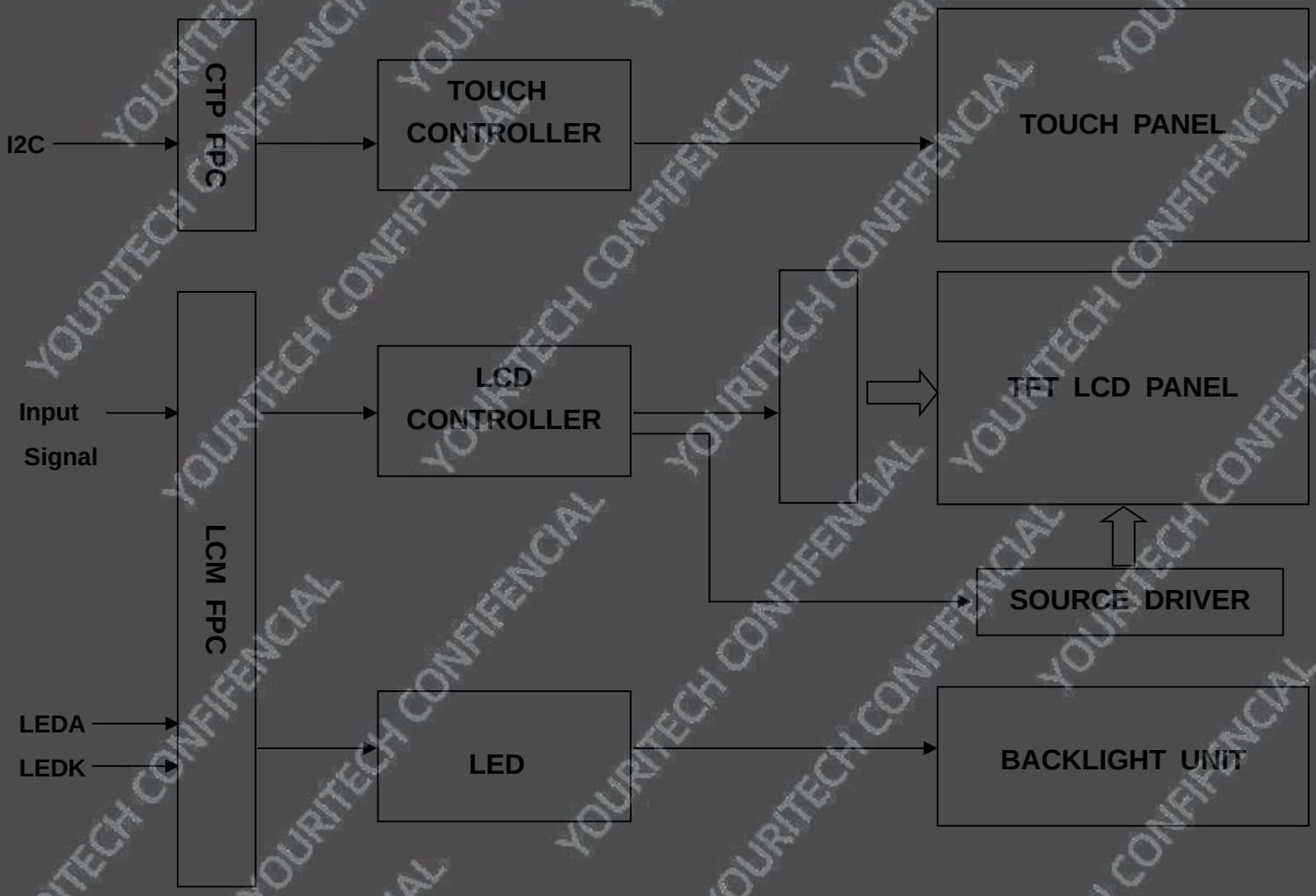
1.2 CTP Features

General information Items	Specification	Unit	Note
	Main Panel		
Resolution	480(H)*640(V)	-	
Structure	G+G	-	
Controller IC	FT5436	-	
Interface	I2C	-	
Slave Adress	0x38(7bit)/8bit:0x70(Write) 0x71(Read)	-	
Touch mode	Five point and Gestures	-	
Logic level	1.8 or 3.3	V	Set by VDDIO

1.3 Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	48.72	-	mm	
	Vertical(V)	-	70.26	-	mm	
	Depth(D)	-	3.94	-	mm	
Weight		-	20	-	g	

2. Block Diagram



3. Outline dimension

4. Input terminal Pin Assignment

4.1 TFT PIN Define

NO.	SYMBOL	DISCRIPTION	I/O
1	NC	--	--
2	NC	--	--
3	NC	--	--
4	NC	--	--
5	GND	Ground.	P
6	GND	Ground.	P
7	VCI	Supply voltage.	P
8	IOVCC	I/O power supply voltage.	P
9	SDO	SPI interface output pin.-The data is output on the falling edge of the SCL signal.-If not used, let this pin open.	O
10	SDI	Data lane in 1 data lane serial interface. The data is latched on the rising edge of the SCL signal.	I
11	SCL	This pin is used serial interface clock in 3-wire 9-bit serial data interface.	I
12	CS	Chip select input pin (“Low” enable).	I
13	RESET	Reset pin. Must be reset after power is supplied.	I
14-37	DB23-DB0	24-bit parallel bi-directional data bus RGB interface mode . Fix to GND level when not in use	I
38	DE	Data enable signal for RGB interface peration.	I
39	PCLK	Dot clock signal for RGB interface operation.	I
40	HSYNC	Line synchronizing signal for RGB interface operation.	I
41	VSYNC	Frame synchronizing signal for RGB interface operation.	I
42	NC	--	--
43	LEDK	Cathode pin of backlight.	P
44	NC	--	--
45	LEDA	Anode pin of backlight.	P

4.2 CTP PIN Define

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VDDIO	I/O power supply voltage.	P
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P

5. LCD Optical Characteristics

5.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal viewing angle	800	1000	--		(1)(2)
Response time	Rising	$T_{R+}T_F$		--	--	35	msec	(1)(3)
	Falling							
Color Gamut		S(%)		50	55	--	%	
Color Filter Chromacicity	White	W_X		0.262	0.302	0.342		CA-310 test
		W_Y		0.285	0.325	0.365		
	Red	R_X		0.569	0.609	0.649		
		R_Y		0.312	0.352	0.392		
	Green	G_X		0.288	0.328	0.368		
		G_Y		0.540	0.580	0.620		
	Blue	B_X		0.114	0.154	0.194		
		B_Y		0.041	0.081	0.121		
Viewing angle	Hor.	ΘL	CR>10	70	80	--		(1)(4)
		ΘR		70	80	--		
	Ver.	ΘU		70	80	--		
		ΘD		70	80	--		
Option View Direction		Free						

Measuring Condition

Measuring surrounding : dark room

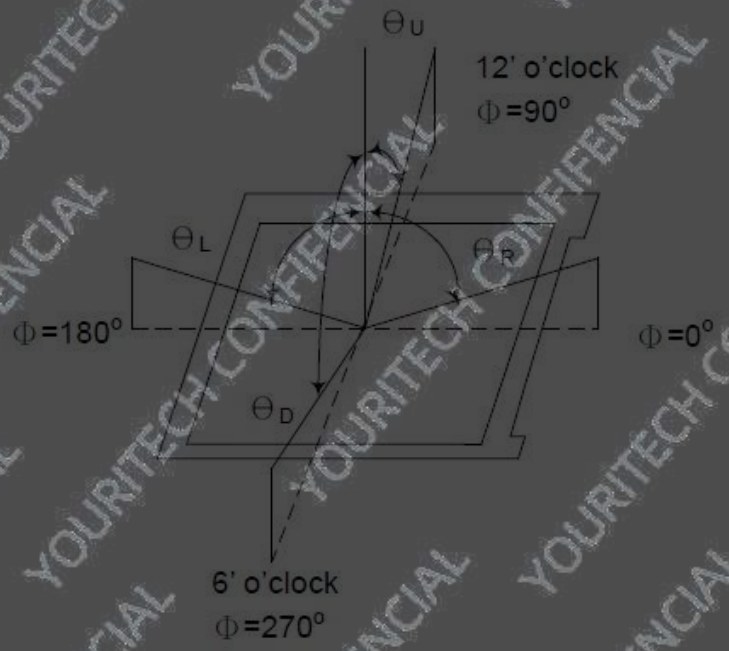
Ambient temperature : 25±2°C

15min. warm-up time.

Measuring Equipment

FPM520 , which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

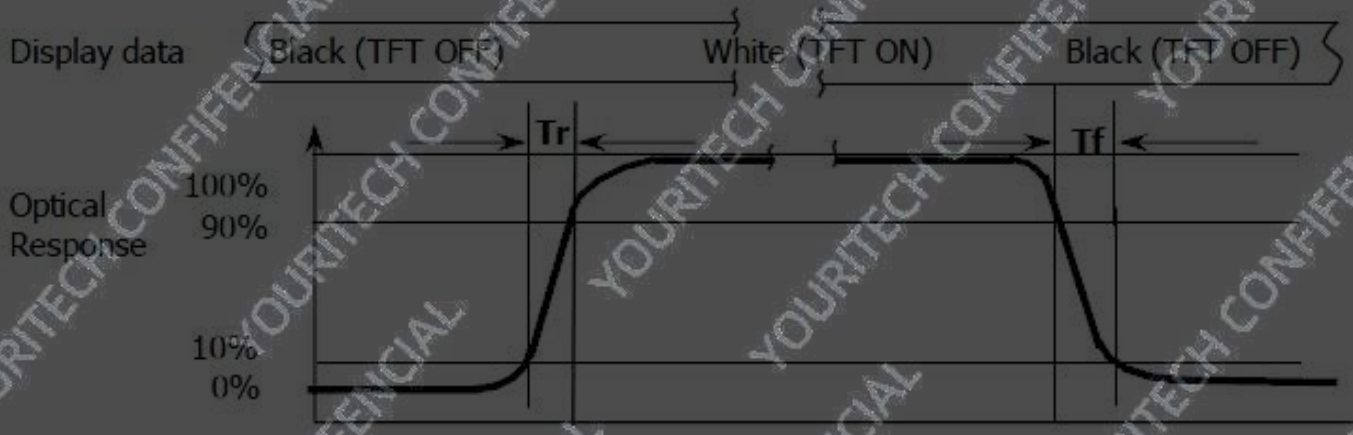
Note (1): Definition of Viewing Angle :



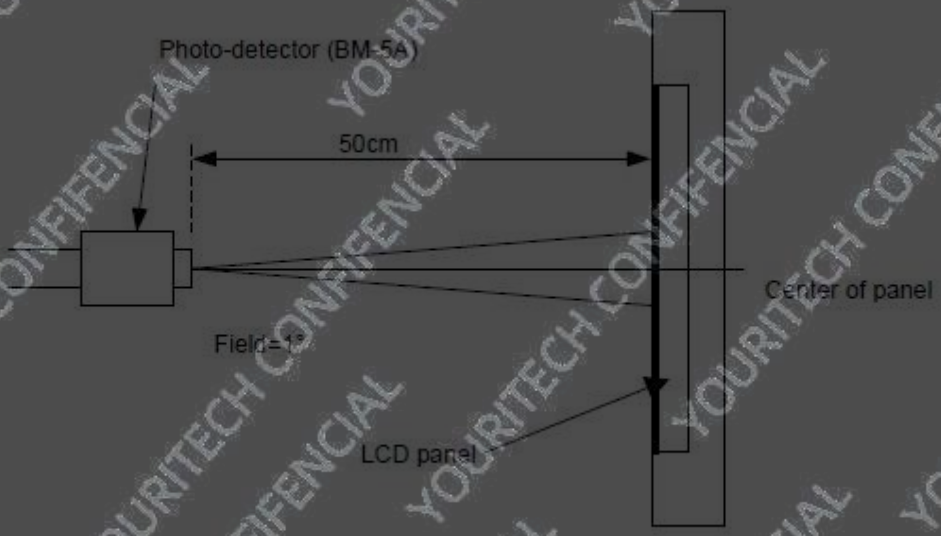
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



6. Electrical Characteristics

6.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VCI	-0.3	4.6	V	Note1
Digital interface supply Voltage	IOVCC	-0.3	4.6	V	Note1
Operating temperature	T_{OP}	-30	+80	℃	
Storage temperature	T_{ST}	-30	+80	℃	

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

6.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	3.3	3.6	V	
Digital interface supply Voltage	IOVCC	1.65	1.8	3.3	V	
Normal mode Current	IDD	--	20	40	mA	
Level input voltage	V_{IH}	0.7*IOVCC	--	IOVCC	V	
	V_{IL}	GND	--	0.3*IOVCC	V	
Level output voltage	V_{OH}	0.8*IOVCC	--	IOVCC	V	
	V_{OL}	GND	--	0.2*IOVCC	V	

6.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 4 double chips LED

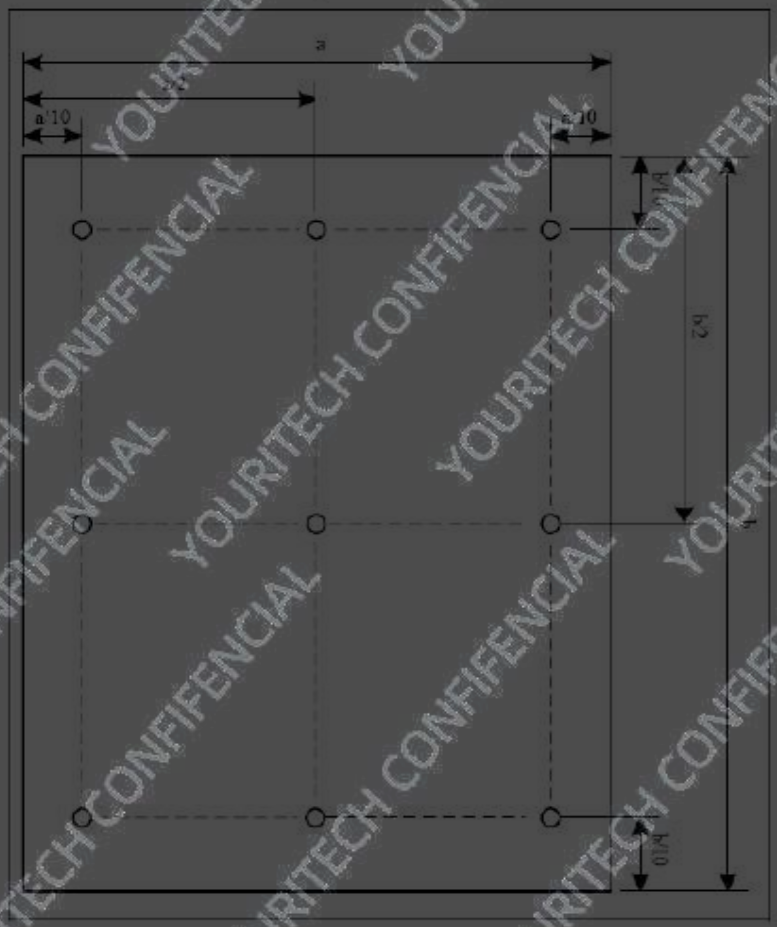
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	--	20	--	mA	
Forward Voltage	V_F	--	24	25.6	V	
LCM Luminance	LV	640	680	--	cd/m2	Note3
LED life time	Hr	--	50000	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.

BLU CIRCUIT DIAGRAM

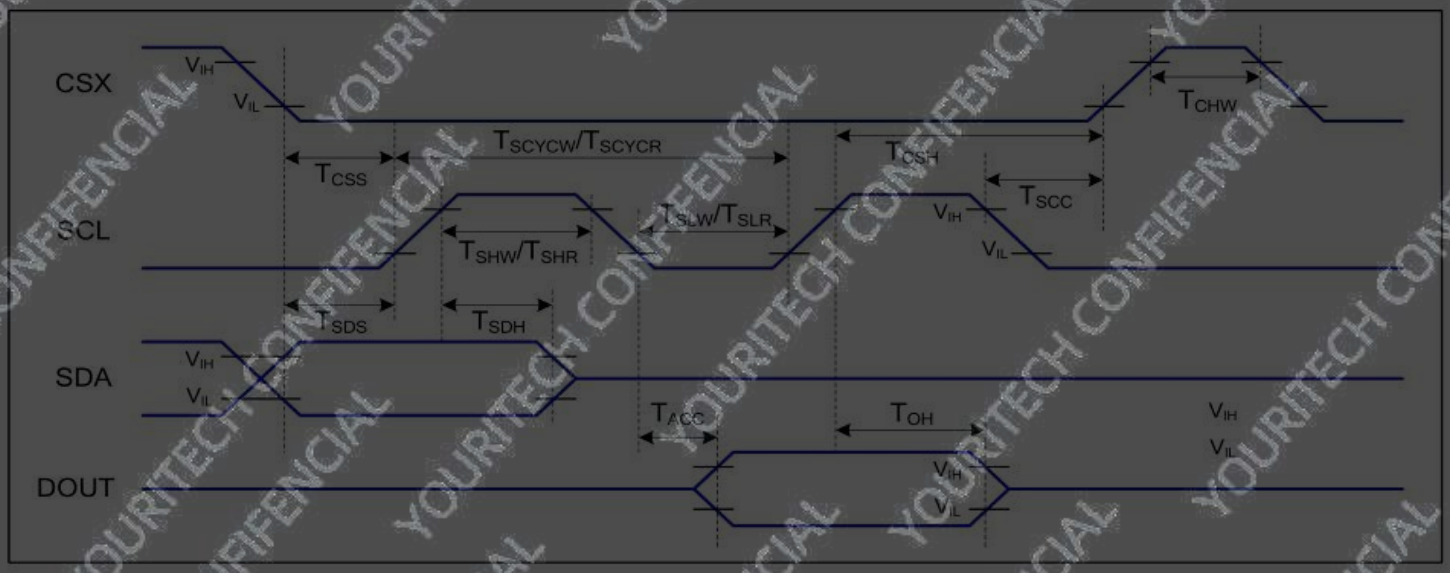
Note (3) Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

7. AC Characteristics

7.1 Serial Interface Characteristics (3-line serial):



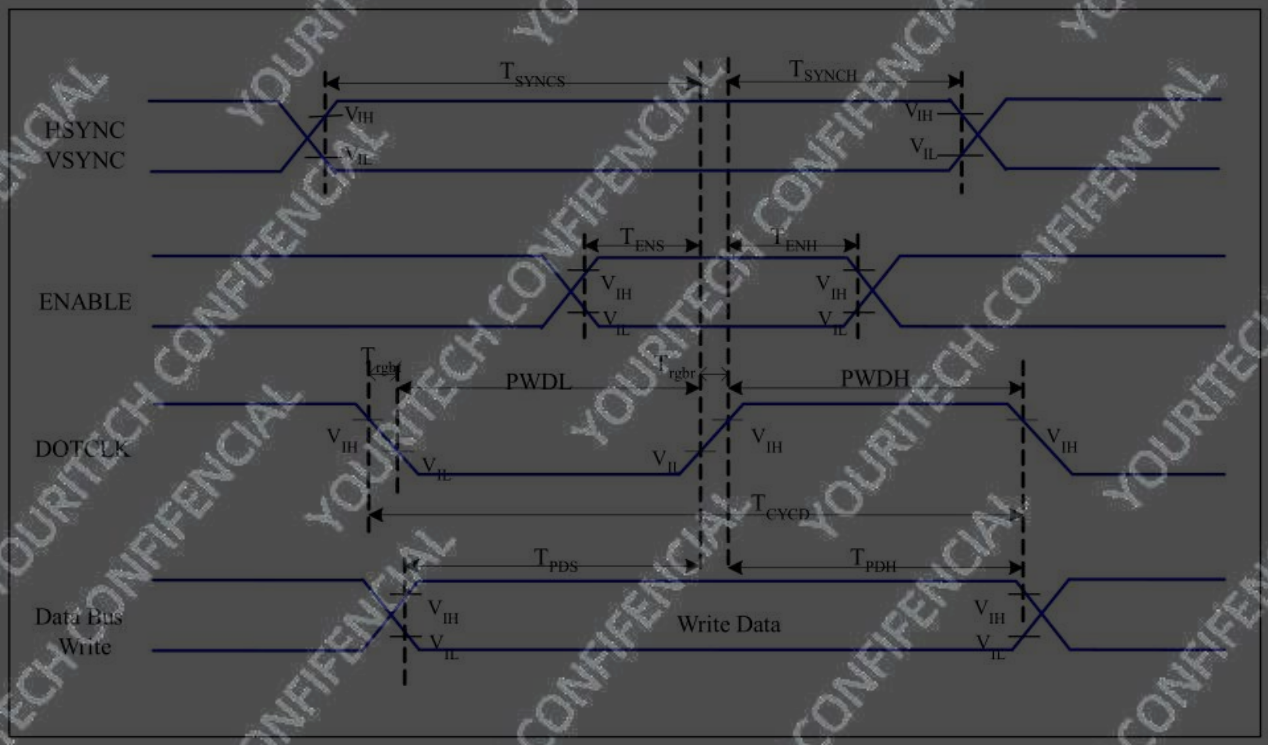
3-line serial Interface Timing Characteristics

IOVCC=1.8V,VCI=2.8V,Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	60		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

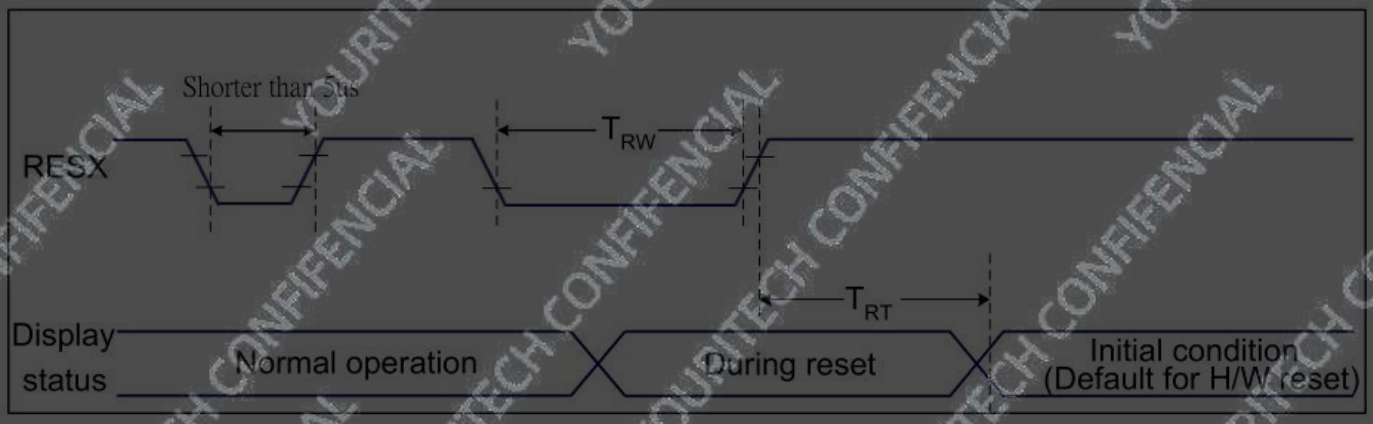
7.2. RGB Interface Characteristics :



RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	5	-	ns	
	T_{ENH}	Enable Hold Time	5	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	33		ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	5	-	ns	
	T_{PDH}	PD Data Hold Time	5	-	ns	

7.3 Reset input timing：



Reset Timing

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Reset Timing

Notes:

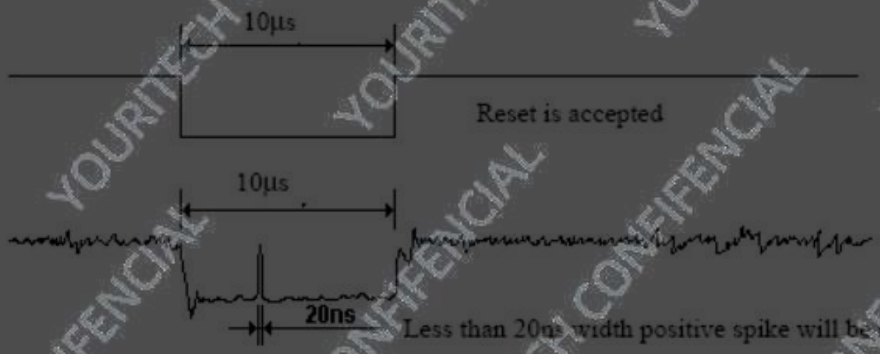
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. RGB Interface

The ST7701S support RGB interface Mode 1 and Mode 2. The interface signals as shown in table 6.3.1. The Mode 1 and Mode 2 function is select by setting in the Command 2, please reference application note. In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D[23:0]), when DE is high state. The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to ST7701S.

In RGB Mode 2, back porch of Vsync is defined by VBP_HVRGB [7:0] of RGBCTR command. And back porch of Hsync is defined by HBP_HVRGB [7:0] of RGBCTR command. Front porch of Vsync are not setting by this mode.

RGB I/F Mode	PCLK	DE	VS	HS	DB[23:0]	Register for Blanking Porch setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

Symbol	Name	Description
PCLK	Pixel clock	Pixel clock for capturing pixels at display interface
HS	Horizontal sync	Horizontal synchronization timing signal
VS	Vertical sync	Vertical synchronization timing signal
DE	Data enable	Data enable signal (assertion indicates valid pixels)
DB[23:0]	Pixel data	Pixel data in 16-bit,18-bit and 24-bit format

The interface signals of RGB interface

8.1 RGB Color Format

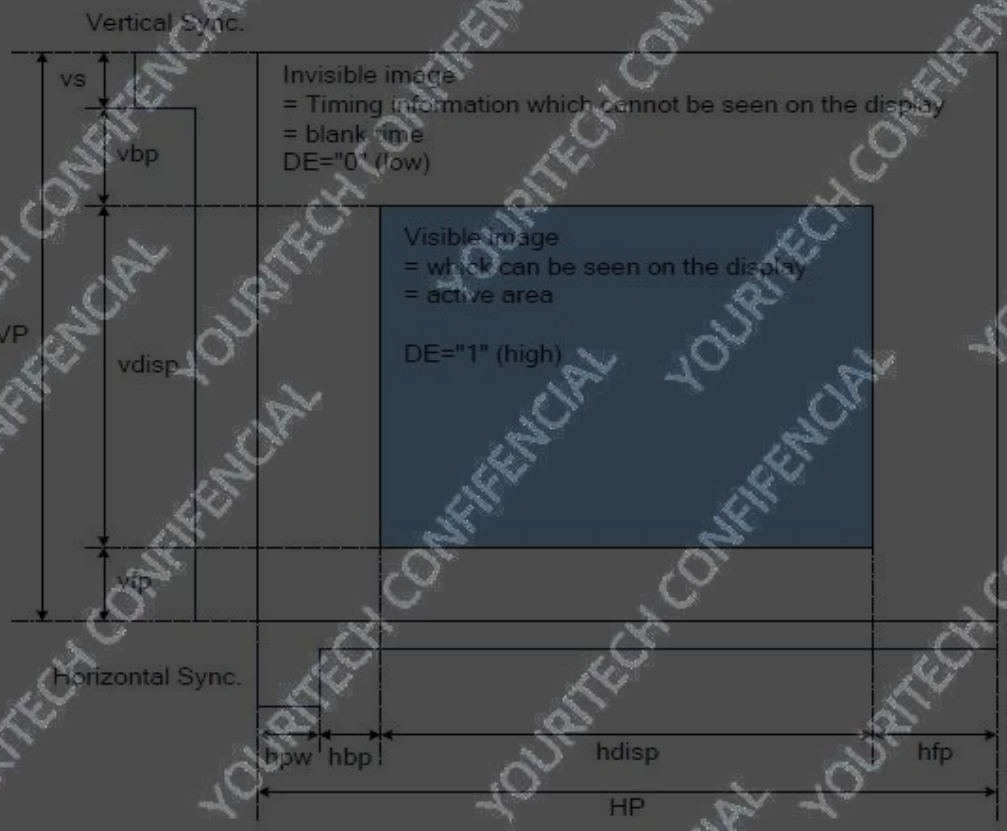
ST7701S supports two kinds of RGB interface, DE mode (mode 1) and HV mode (mode 2), and 16bit/18bit and 24 bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D[23:0] pins can be used; when HV mode is selected and the VSYNC, HSYNC, DOTCLK, D[23:0] pins can be used. When using RGB interface, only serial interface can be selected.

Pad name	24 bits configuration VIPF[3:0]=0111	18 bits configuration VIPF[3:0]=0110		16 bits configuration VIPF[3:0]=0101
		MDT=0	MDT=1	
DB[23]	R7	Not used	Not used	Not used
DB[22]	R6	Not used	Not used	Not used
DB[21]	R5	R5	Not used	Not used
DB[20]	R4	R4	Not used	R4
DB[19]	R3	R3	Not used	R3
DB[18]	R2	R2	Not used	R2
DB[17]	R1	R1	R5	R1
DB[16]	R0	R0	R4	R0
DB[15]	G7	Not used	R3	Not used
DB[14]	G6	Not used	R2	Not used
DB[13]	G5	G5	R1	G5
DB[12]	G4	G4	R0	G4
DB[11]	G3	G3	G5	G3
DB[10]	G2	G2	G4	G2
DB[09]	G1	G1	G3	G1
DB[08]	G0	G0	G2	G0
DB[07]	B7	Not used	G1	Not used
DB[06]	B6	Not used	G0	Not used
DB[05]	B5	B5	B5	Not used
DB[04]	B4	B4	B4	B4
DB[03]	B3	B3	B3	B3
DB[02]	B2	B2	B2	B2
DB[01]	B1	B1	B1	B1
DB[00]	B0	B0	B0	B0

The interface color mapping of RGB interface

8.2 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.



DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	FCLK	--	20	--	MHz
Horizontal Sync. Width	hpw	1	2	255	Clock
Horizontal Sync. Back Porch	hbp	1	14	255	Clock
Horizontal Sync. Front Porch	hfp	1	8	--	Clock
Vertical Sync. Width	vs	1	2	254	Line
Vertical Sync. Back Porch	vbp	1	10	254	Line
Vertical Sync. Front Porch	vfp	1	8	--	Line

Note:

1. Typical value are related to the setting frame rate is 60Hz.

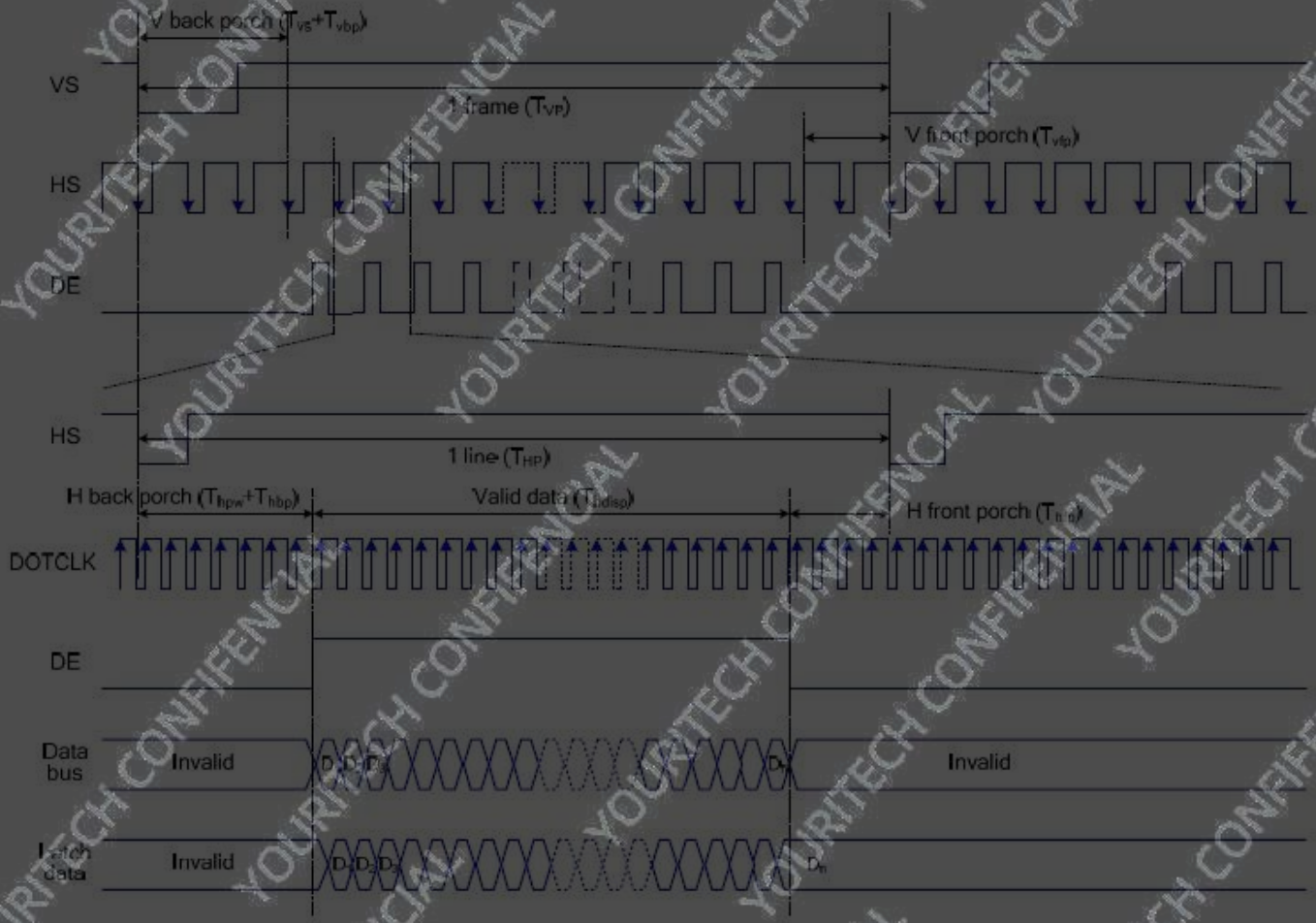
8.3 RGB Interface Mode Selection

ST7701S supports two kinds of RGB interface, DE mode and HV mode. The table shown below uses command C3h to select RGB interface mode.

DE/Sync	RGB Mode
0	DE mode
1	HV mode

8.4 RGB Interface Timing

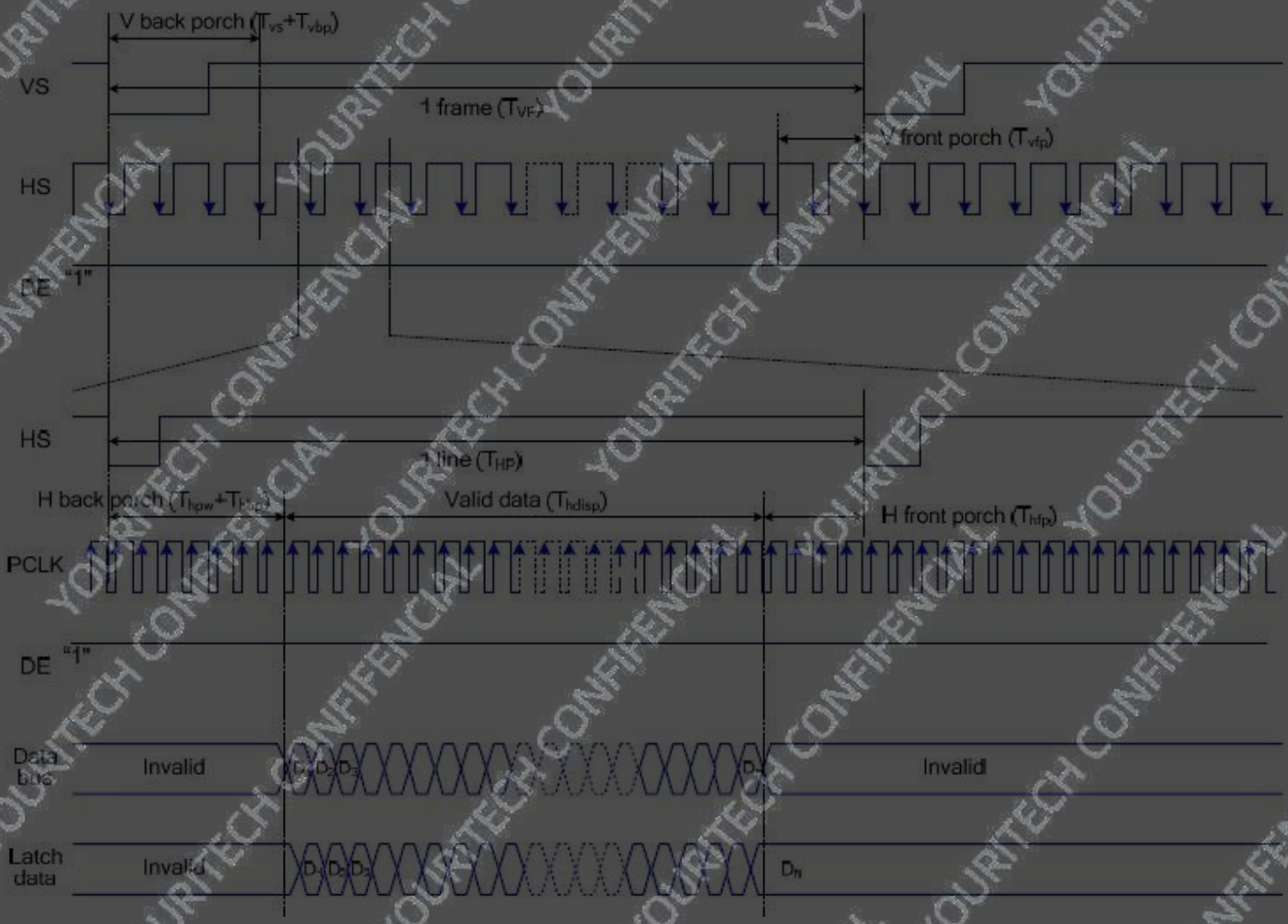
The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.



Timing chart of RGB interface HV mod

9. CTP Specification

9.1 Electrical Characteristics

9.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	-0.3	3.6	V	1
I/O Digital Voltage	VDDIO	1.8	3.6	V	1
Operating temperature	T_{OP}	-20	+70	℃	-
Storage temperature	T_{ST}	-30	+80	℃	-

NOTES:

1. If used beyond the absolute maximum ratings, FT5436 may be permanently damaged. It is strongly recommanded that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

9.1.2 DC Electrical Characteristics (Ta=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Digital supply voltage	VDD		2.8	3.3	3.6	V	
I/O Digital supply voltage	VDDIO		1.8	3.3	3.6	V	
Normal operation mode Current consumption	I_{opr}	VDD=2.8V Ta=25℃ MCLK= 17.5Mhz	-	11	-	mA	
Monitor mode Current consumption	I_{mon}		-	0.43	-	mA	
Sleep mode Current consumption	I_{slp}		-	42	-	uA	
Level input voltage	V_{IH}		$0.7V_{DDIO}$	-	V_{DDIO}	V	
	V_{IL}		-0.3	-	$0.3V_{DDIO}$	V	
Level output voltage	V_{OH}	I_{OH}=-0.1mA	$0.7V_{DDIO}$	-	-	V	
	V_{OL}	I_{OH}=0.1mA	-	-	$0.3V_{DDIO}$	V	

9.2 POWER ON/Reset/Wake Sequence

The GPIO such as INT and I2C are advised to be low before powering on. Reset should be pulled down to be low before powering on.INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Trst is more than 5ms.

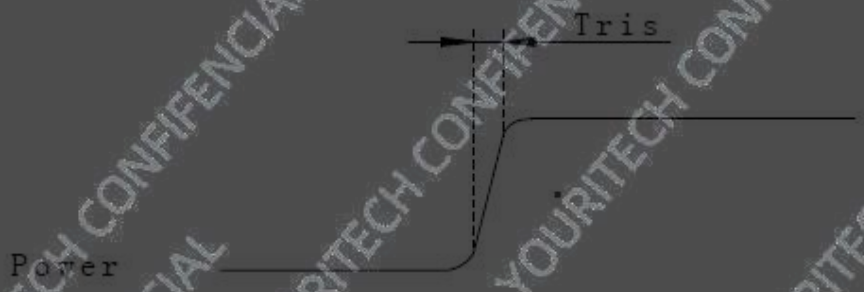


Figure 3-7 Power on time

Figure 3-8 Power Cycle requirement

Figure 3-9 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on

Figure 3-10 Reset Sequence

Table 3-5 Power on Reset/Wake Sequence Parameters

Parameter	Description	Min	Max	Units
Trs	Rise time from 0.1VDD to 0.9VDD	-	3	ms
Tpon	Time of starting to report point after powering on	300	-	ms
Tprt	Time of being low after powering on	1	-	ms
Trsi	Time of starting to report point after resetting	300	-	ms
Trst	Reset time	5		ms

9.3 I2C Timing

FT5436 supports the I2C interfaces, which can be used by a host processor or other devices.

The I2C is always configured in the Slave mode. The data transfer format is shown in **Figure 2-4.**

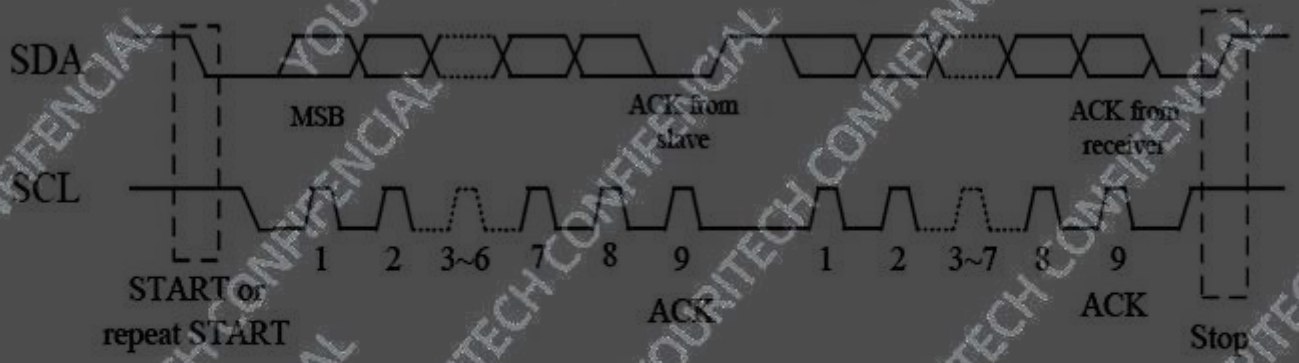


Figure 2-4 I2C Serial Data Transfer Format

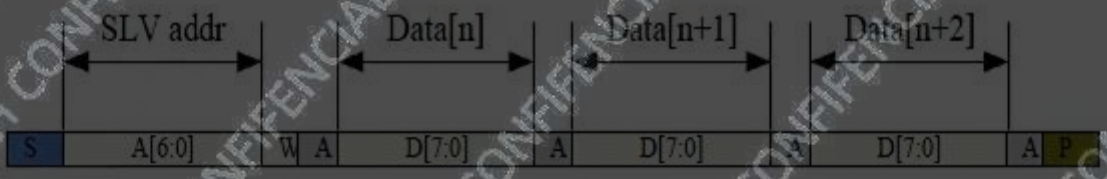


Figure 2-5 I2C master write, slave read

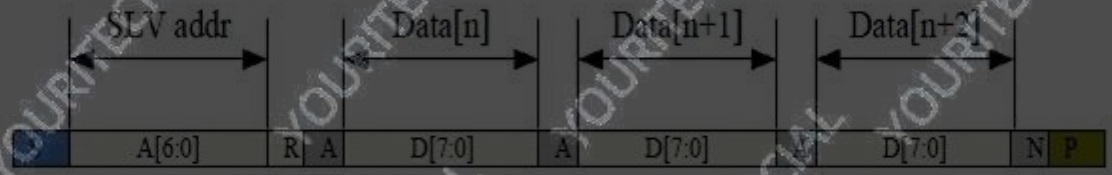


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/ W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	0	400	KHz
Bus free time between a STOP and START condition	1.3		us
Hold time (repeated) START condition	0.6		us
Data setup time	100		ns
Setup time for a repeated START condition	0.6		us
Setup Time for STOP condition	0.6		us

10. LCD Module Out-Going Quality Level

10.1 VISUAL & FUNCTION INSPECTION STANDARD

10.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

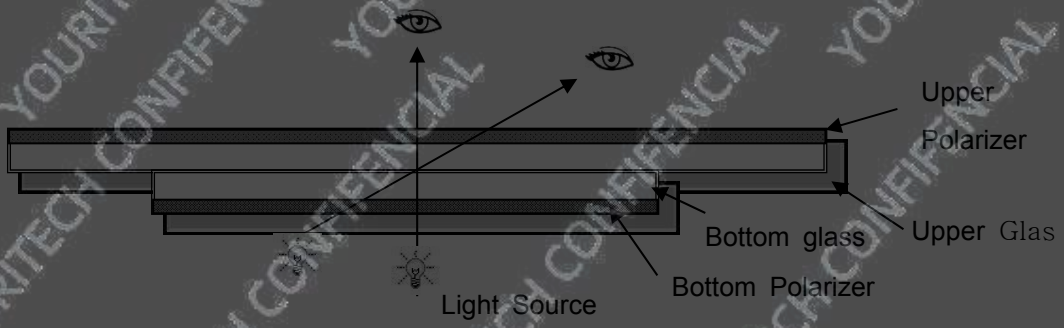
Temperature : 25±5℃

Humidity : 65%±10%RH

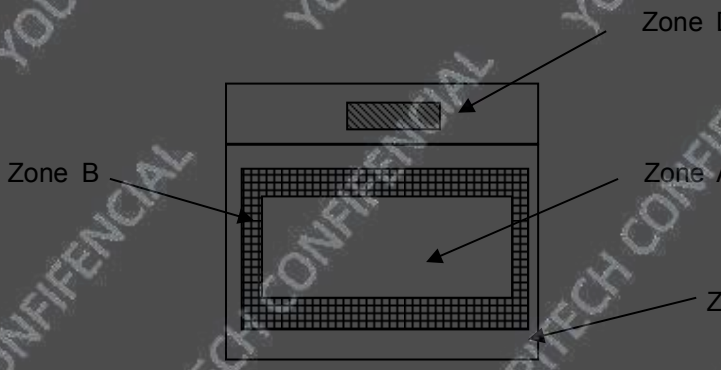
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



10.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer

Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

10.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ
AQL:

Major defect	Minor defect
0.65	1.5

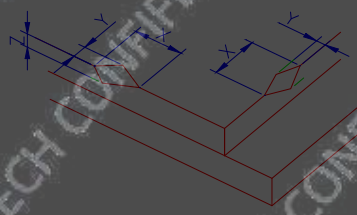
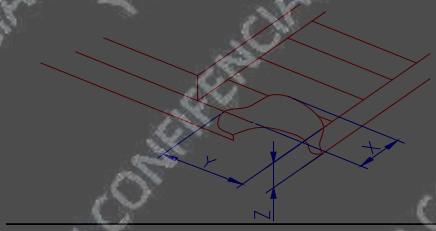
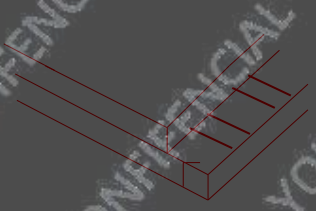
LCD: Liquid Crystal Display , LCM: Liquid Crystal Module, CTP: Capacitive Touch Panel

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc	Major
2	Missing	Missing components and etc	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed,deformation and etc	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot,Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer/CTP	Black/White spot/line, scratch, crack, etc.	

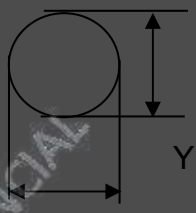
Note1: a) Light dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

10.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

Spot defect



Φ=(X+Y)/2

① light dot（black/white spot、pinhole, stain，etc.）

Size (mm) \ Zone	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧6mm)		
0.25<Φ≤0.4	2(distance≧6mm)		
Φ>0.4	0		

② Dim spot（light leakage、dent、dark spot，etc）

Size (mm) \ Zone	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧6mm)		
0.25<Φ≤0.4	2(distance≧6mm)		
Φ>0.4	0		

③ Polarizer accidented spot

Size (mm) \ Zone	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance≧6mm)		
Φ>0.5	0		

④Polarizer Bubble

Size (mm) \ Zone	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	3(distance≧6mm)		
Φ>0.4	0		

3.0	LCD Pixel defect	Pixel bad points

Item	Zone A	Acceptable Qt
Bright dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Dark dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm
Total bright and dark dot		N≤4

Note:

A) Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

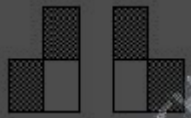
C) 2 dot adjacent = 1 pair = 2 dots

Picture:

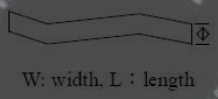
2 dot adjacent

2 dot adjacent

2 dot adjacent (vertical)



2 dot adjacent (slant)

<table>
<tr>
<td>4.0</td>
<td>Line defect (LCD /Polarizer backlight black/white line, scratch, stain)
 

W: width, L：length
N：Count</td>
<td>
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Length(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.03</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.04</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.04<W≤0.05</td><td>L≤2.0</td><td colspan="2">N≤1</td></tr>
<tr><td>W>0.05</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td>
</tr>
<tr>
<td>5.0</td>
<td>Electronic Components SMT.</td>
<td>Not allow missing parts，solderless connection，cold solder joint，mismatch，The positive and negative polarity opposite</td>
</tr>
<tr>
<td>6.0</td>
<td>Display color& Brighness.</td>
<td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td>
</tr>
<tr>
<td>7.0</td>
<td>LCD Mura/Waving/ Hot spot</td>
<td>Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.</td>
</tr>
</table>

<table>
<tr>
<td>8.0</td>
<td>CTP Related</td>
<td>CTP Cover sensor accidented black/white spot</td>
<td>
<table>
<tr><td rowspan="2">Size Φ(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.1<Φ≤0.2</td><td colspan="2">3（distance≧6mm）</td></tr>
<tr><td>0.20<Φ≤0.25</td><td colspan="2">2（distance≧6mm）</td></tr>
<tr><td>Φ＞0.25</td><td colspan="2">0</td></tr>
</table>
</td>
</tr>
</table>

CTP Cover scratch

Width(mm)	Ignore (mm)	Acceptable Qty		
		A	B	C
Φ≤0.03	Ignore	Ignore		
0.03<W≤0.04	L≤3.0	N≤2		
0.04<W≤0.05	L≤2.0	N≤1		
0.05<W	Define as spot defect			

CTP Cover Pinhole/ Lack of ink

Size (mm) \ Zone	Acceptable Qty
	C
Φ≤0.1	Ignore
0.1<Φ≤0.25	3(distance≧6mm)
0.25<Φ≤0.3	2(distance≧6mm)
Φ>0.3	0

CTP Bonding bubble/ accidented spot

Size Φ(mm)	Acceptable Qty	
	A	B
Φ≤0.1	Ignore	
0.1<Φ≤0.2	3(distance≧6mm)	
0.2<Φ≤0.25	2(distance≧6mm)	
Φ>0.25	0	

Assembly deflection

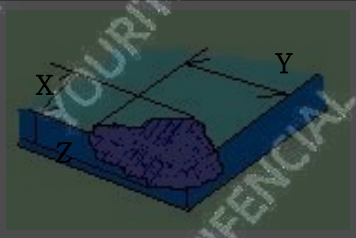
beyond the edge of backlight ≤0.2mm

CTP cover broken

X：length
Y：width
Z：height

X	Y	Z
X≤0.5mm	Y≤0.5mm	Z<cover thickness

*Circuitry broken is not allowed.



		CTP cover broken X：length Y：width Z：height	X: X≤0.3mm; Y: Y≤0.3mm; Z: Z<cover thickness * Circuitry broken is not allowed.	

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	CTP no function	Not allowed

11. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20℃, 96HR	
High Temperature Storage	80℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Operating	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-10℃,30 min ↔ +60℃,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

Remark:

1.The test samples should be applied to only one test item.

2.Sample size for each test item is 5~10pcs.

3.For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.

4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

6. The color fading mura of polarizing filter should not care.

12. Cautions and Handling Precautions

12.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

12.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.