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Project No. 项目编号	ET024VG10-T
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	**Standard LCD Module** **TFT：240*RGBx320Dots** **2.4”TFT LCD**

客户确认Customer Approval	
项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	

1. Introduction

1.1 Scope of application

This specification applies to the LCD module that is supplied by YOURITECH TECHNOLOGY

LCD specification: Dots 240xRGBx320.

As to basic specification of the driver IC, refer to the IC (ST7789T3) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;

ALL O'clock Type LCD

240dot-segment and 320 dot-common outputs;

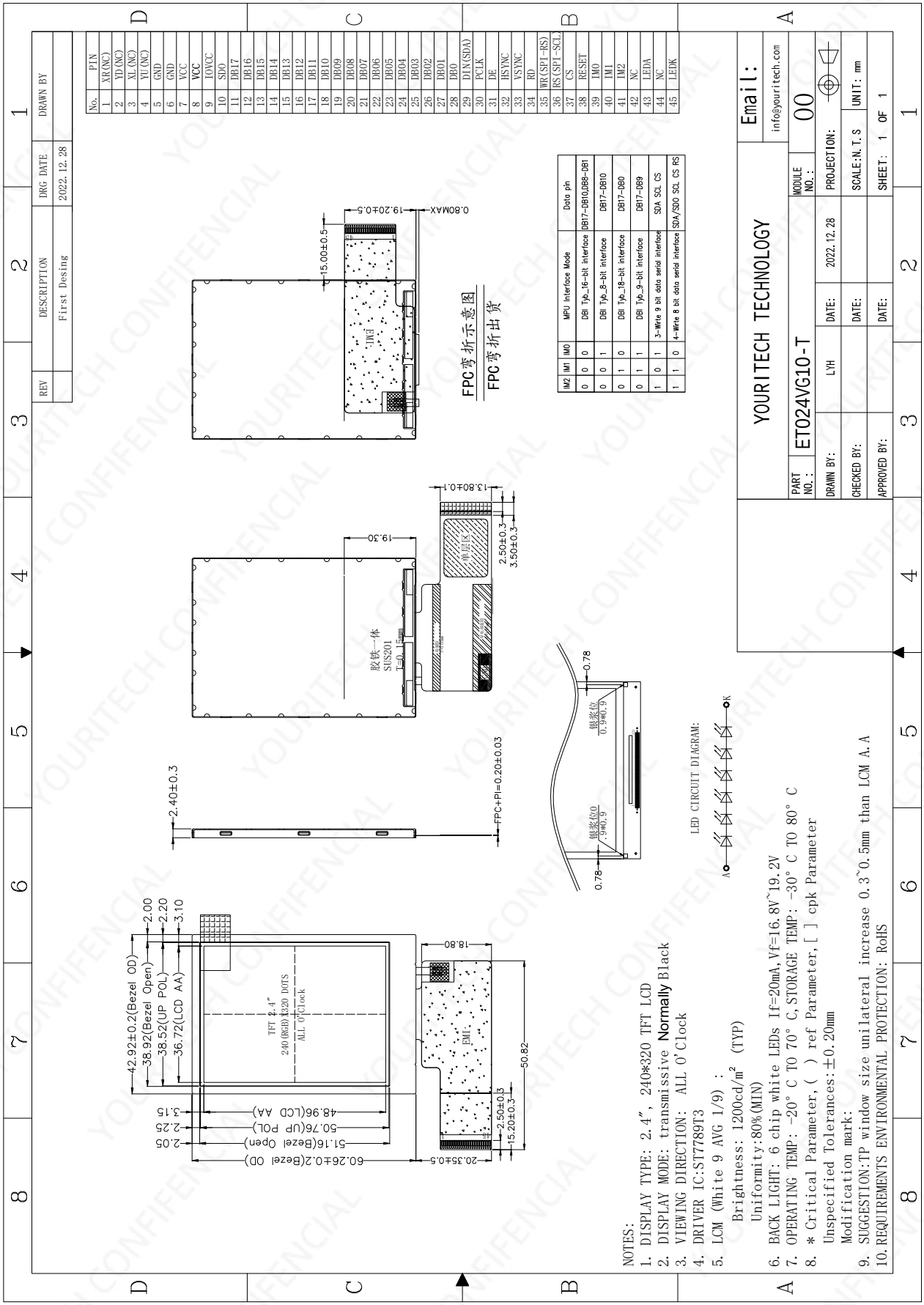
65K/262K Color can be selected by software;

White LED back light;

SPI/RGB/MCU interface

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	240*3RGB(H)X320(V)	Dots
Pixel arrangement	RGB Vertical stripe	--
Pixel Pitch (W*H)	0.153(W) × 0.153(H)	mm
Active area	36.72(W) ×48.96(H)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	ST7789T3-G4	--
TFT interface	SPI/RGB/MCU interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	42.92 (W) ×60.26(H) ×2.40(T)	mm
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--


YOURITECH TECHNOLOGY
Email: info@youritech.com
PART NO.: ET024VG10-T
DRAWN BY: LYH
DATE: 2022.12.28
MODULE NO.: 00
PROJECTION:
CHECKED BY:
APPROVED BY:
SCALE: N.T.S
UNIT: mm
SHEET: 1 OF 1
REV
DESCRIPTION: First Desing
DRG DATE: 2022.12.28
DRAWN BY
No. PIN
1 XR(NC)
2 YD(NC)
3 XL(NC)
4 YU(NC)
5 GND
6 GND
7 VCC
8 VCC
9 IOVCC
10 SDO
11 DB17
12 DB16
13 DB15
14 DB14
15 DB13
16 DB12
17 DB11
18 DB10
19 DB09
20 DB08
21 DB07
22 DB06
23 DB05
24 DB04
25 DB03
26 DB02
27 DB01
28 DB0
29 DIN(SDA)
30 PCLK
31 DE
32 HSYNC
33 VSYNC
34 RD
35 WR(SPI-RS)
36 RS(SPI-SCL)
37 CS
38 RESET
39 IM0
40 IM1
41 IM2
42 NC
43 LEDA
44 NC
45 LEDK
IM2 IM1 IM0 MPU interface Mode Data pin
0 0 0 DBI Typ_16-bit interface DB17-DB10,DB8-DB1
0 0 1 DBI Typ_8-bit interface DB17-DB10
0 1 0 DBI Typ_18-bit interface DB17-DB0
0 1 1 DBI Typ_9-bit interface DB17-DB9
1 0 1 3-Wire 9 bit data serial interface SDA SCL CS
1 1 0 4-Wire 8 bit data serial interface SDA/SDO SCL CS RS
FPC弯折示意图
FPC弯折出货
0.80MAX
19.20±0.5
15.00±0.5
19.30
13.80±0.1
2.50±0.3
3.50±0.3
2.40±0.3
FPC+PI=0.20±0.03
0.78
0.78
42.92±0.2(Bezel OD)
38.92(Bezel Open)
38.52(UP POL)
36.72(LCD AA)
2.00
2.20
3.10
TFT 2.4"
240(RGB)X320 DOTS
ALL 0'Clock
18.80
50.82
20.35±0.5
15.20±0.3
2.50±0.3
60.26±0.2(Bezel OD)
51.16(Bezel Open)
50.76(UP POL)
48.96(LCD AA)
3.15
2.25
2.05
LED CIRCUIT DIAGRAM:
NOTES:
1. DISPLAY TYPE: 2.4", 240*320 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL 0'Clock
4. DRIVER IC:ST7789T3
5. LCM (White 9 AVG 1/9) :
Brightness: 1200cd/m² (TYP)
Uniformity:80%(MIN)
6. BACK LIGHT: 6 chip white LEDs If=20mA,Vf=16.8V~19.2V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
Unspecified Tolerances:±0.20mm
Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage for(DC/DC)	VCI	2.6	2.8	3.3	V	--
Supply Voltage for(IO)	IOVCC	1.65	1.8	3.3	V	--

4.2 Back-Light Unit Characeristics

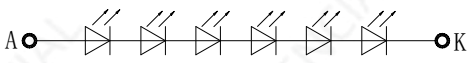
The back-light system is an edge-lighting type with 6 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	16.8	--	19.2	V	--
Forward current	I_F	--	20	--	mA	--
Luminance(With LCD)	Lv	--	1200	--	cd/m^2	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin	Symbol	Functional	Notes
1	XR(NC)	NC	
2	YD(NC)	NC	
3	XL(NC)	NC	
4	YU(NC)	NC	
5~6	GND	Power Ground	
7~8	VCI	Power supply 2.8V	
9	IOVCC	Power supply 1.65~3.3V	
10	SDO	Serial data output pin.	
11~28	DB17~DB0	MCU parallel interface data bus.	
29	DIN(SDA)	Serial data input/output pin.	
30	PCLK	Dot clock signal for RGB interface operation.	
31	DE	Data enable signal for RGB interface operation.	
32	HS	Line synchronous signal for RGB interface operation.	
33	VS	Frame synchronous signal for RGB interface operation.	
34	RD	Read strobe signal.	
35	WR(SPI-RS)	Write strobe signal.	
36	RS	Register selection signal.	
37	CS	Chip selection signal pin.	
38	RESET	Reset signal input terminal. Active at 'L'.	
39~41	IM0~IM2	The interface mode select	
42	NC	NC	
43	LEDA	Power supply for backlight anode input terminal.	
44	NC	NC	
45	LEDK	Power supply for backlight cathode input terminal.	

IM2	IM1	IM0	MPU Interface Mode	Data pin
0	0	0	DBI Tyb_16-bit interface	DB17-DB10,DB8-DB1
0	0	1	DBI Tyb_8-bit interface	DB17-DB10
0	1	0	DBI Tyb_18-bit interface	DB17-DB0
0	1	1	DBI Tyb_9-bit interface	DB17-DB9
1	0	1	3-Wirte 9 bit data serial interface	SDA SCL CS
1	1	0	4-Wirte 8 bit data serial interface	SDA/SDO SCL CS RS

6. Timing Characteristics

Power ON/OFF Sequence

VDDI and VDD can be applied in any order.

In CABC function application, VDDI power on need delay 5ms after VDD has been supplied.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

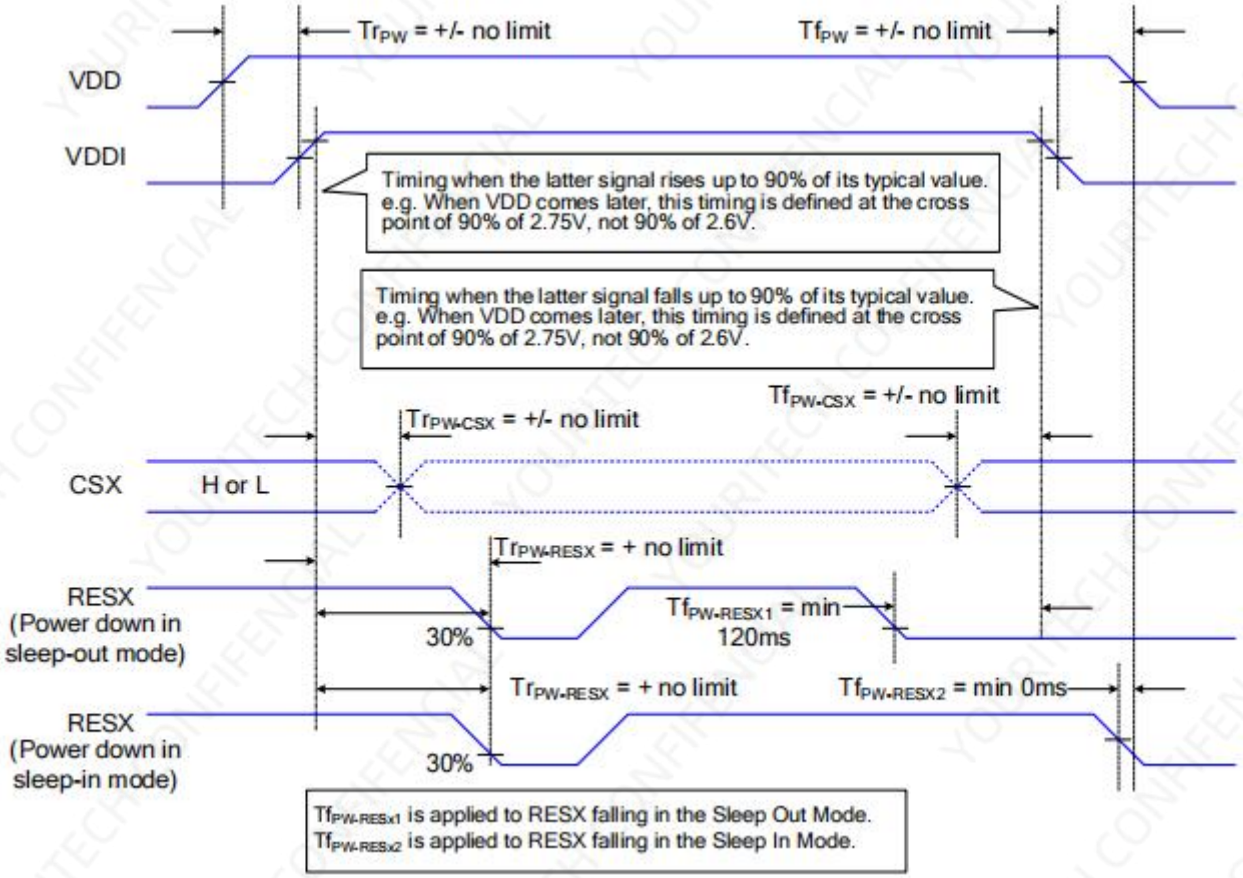
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



Serial Interface Characteristics (3-line serial):

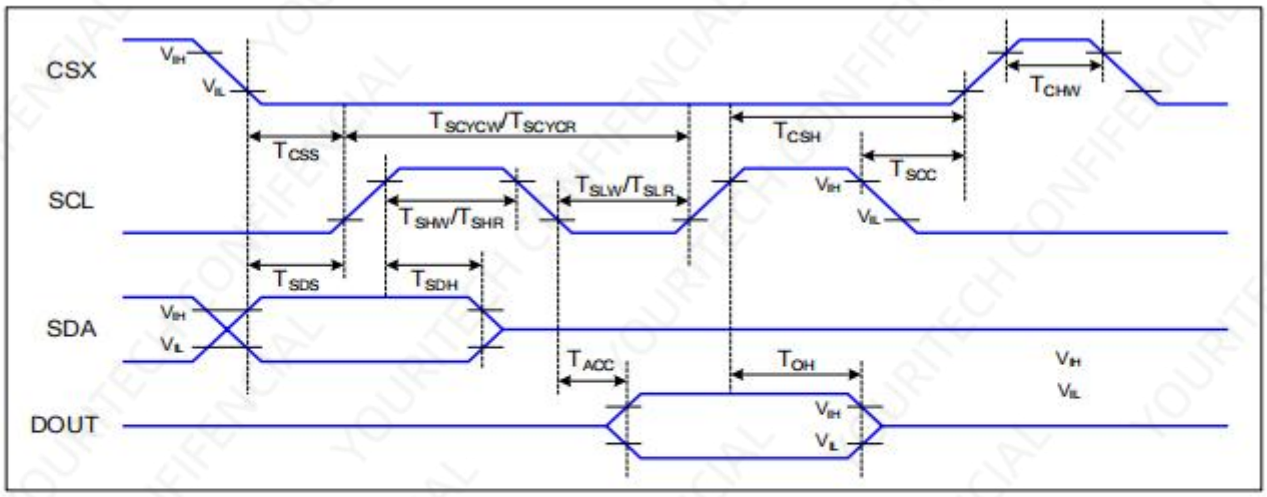


Figure 4 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	TCSS	Chip select setup time (write)	15		ns	
	TCSH	Chip select hold time (write)	15		ns	
	TCSS	Chip select setup time (read)	60		ns	
	TSCC	Chip select hold time (read)	65		ns	
	TCHW	Chip select "H" pulse width	40		ns	
SCL	TSCYCW	Serial clock cycle (Write)	16		ns	
	TSHW	SCL "H" pulse width (Write)	7		ns	
	TSLW	SCL "L" pulse width (Write)	7		ns	
	TSCYCR	Serial clock cycle (Read)	150		ns	
	TSHR	SCL "H" pulse width (Read)	60		ns	
	TSLR	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	TSDS	Data setup time	7		ns	
	TSDH	Data hold time	7		ns	
DOUT	TACC	Access time	10	50	ns	For maximum CL=30pF
	TOH	Output disable time	15	50	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note1 : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

Serial Interface Characteristics (4-line serial):

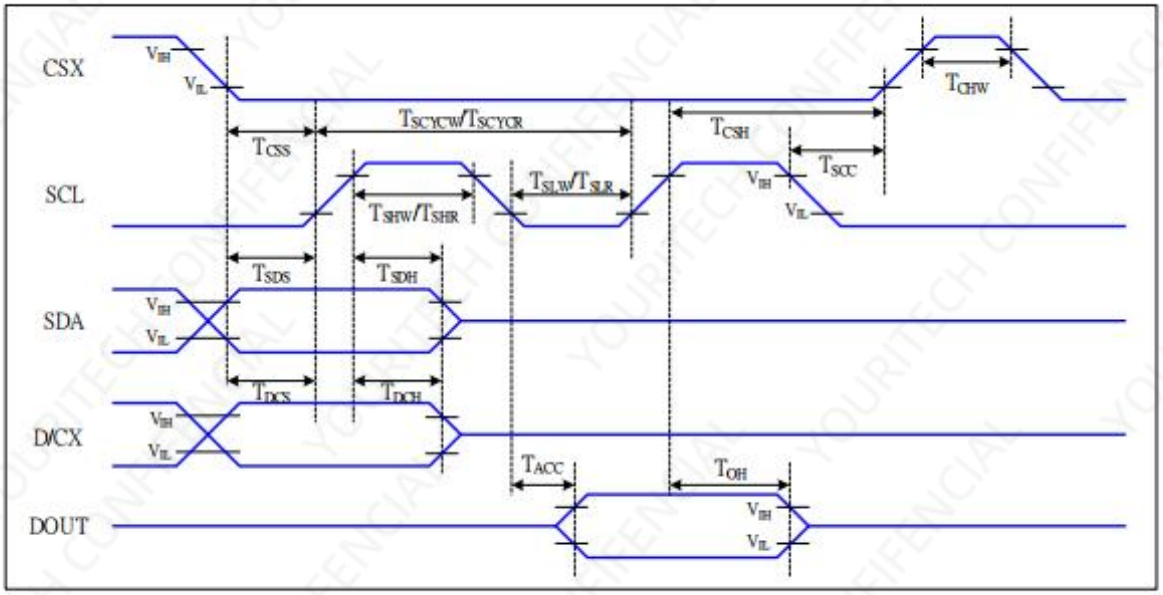


Figure 5 4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	7		ns	
	T_{SLW}	SCL "L" pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 6 4-line serial Interface Characteristics

Note1 : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

Note2: In the read sequence of serial interface, the 500nsec delay time is needed between read command and first read clock.

8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

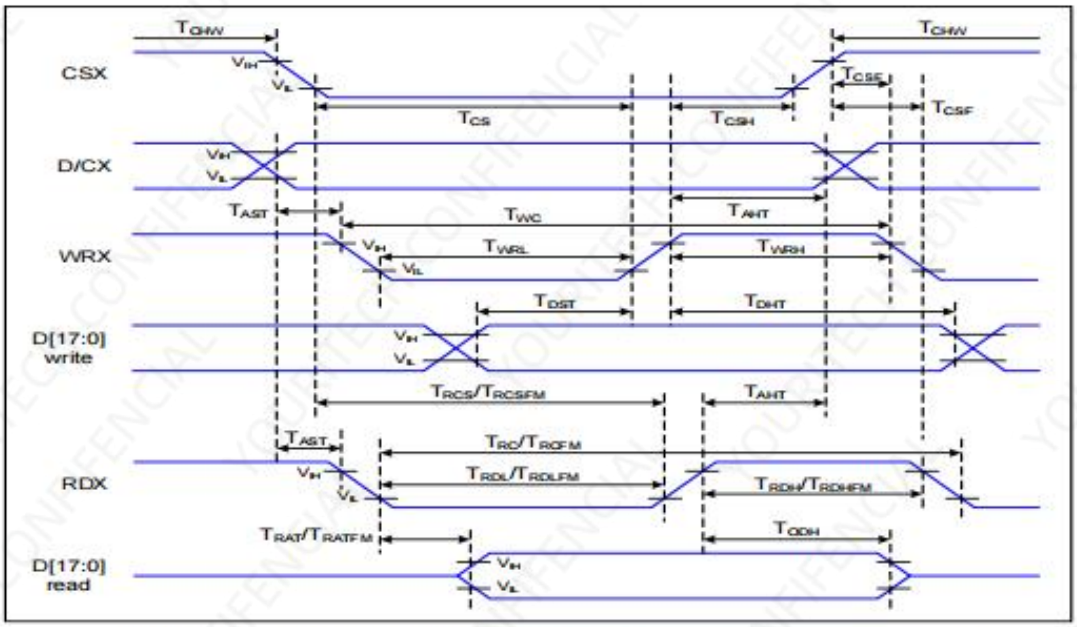


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF

	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Table 4 8080 Parallel Interface Characteristics

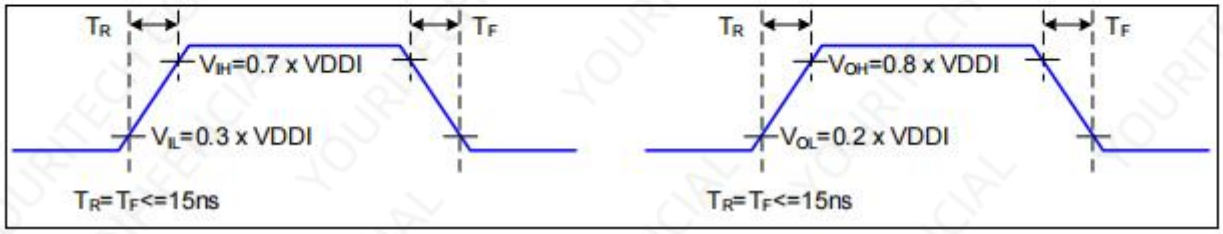


Figure 2 Rising and Falling Timing for I/O Signal

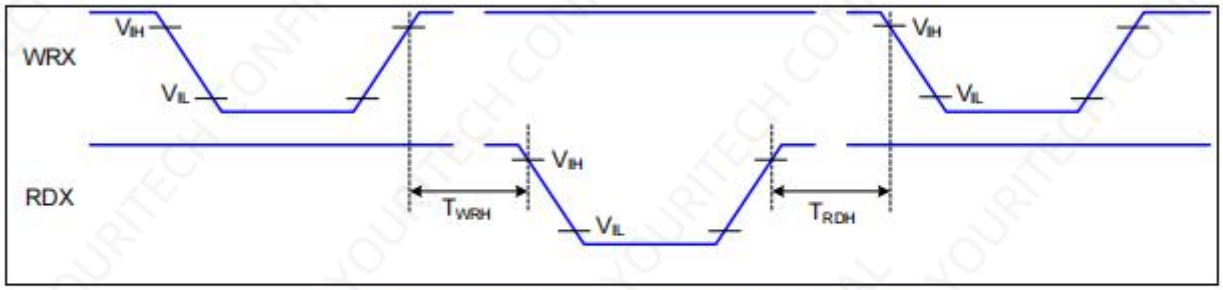


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

RGB Interface Characteristics:

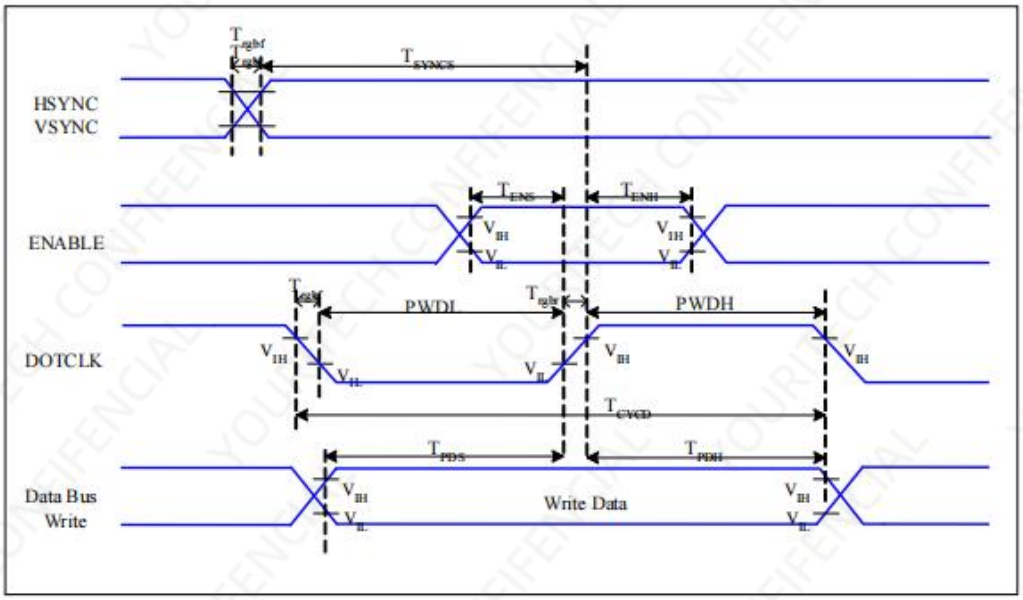


Figure 6 RGB Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

Table 7 18/16 Bits RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	35	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	35	-	ns	
	T_{ENH}	Enable Hold Time	35	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	35	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	35	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	80	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	10	ns	
DB	T_{PDS}	PD Data Setup Time	35	-	ns	
	T_{PDH}	PD Data Hold Time	35	-	ns	

Table 8 6 Bits RGB Interface Timing Characteristics

Reset Timing:

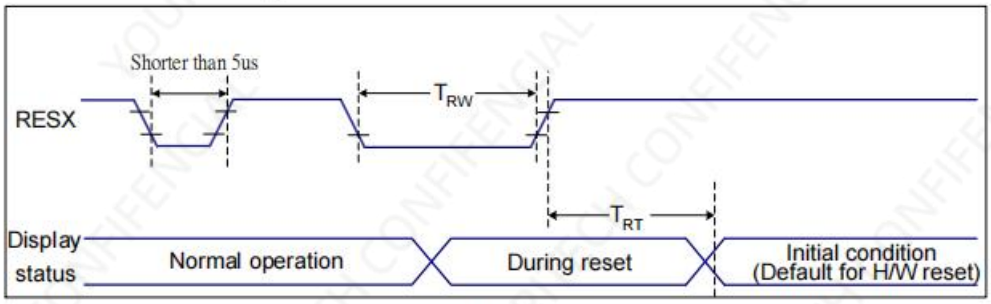


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

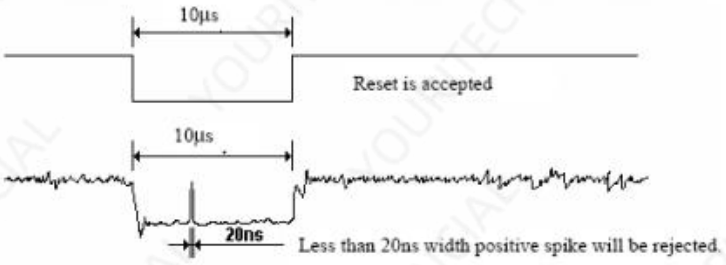
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

7.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T (%)	Θ=0 Normal viewing angle	—	4.65	—	%	Measuring with Polarizer, Reference Only
Transmittance (without Polarizer)		T (%)		—	14.6	—	%	
Contrast		CR		640	800	—	—	(1)(2)
Response time	Rising	T_R		—	16	21	msec	(1)(3)
	Falling	T_F		—	19	24		
Color gamut	(%)			—	70	—	%	C-light
Color chromaticity (CIE1931)	White	W_x		0.290	0.310	0.330	—	(1)(4) CF glass
		W_y		0.316	0.336	0.356		
	Red	R_x		0.627	0.647	0.667	—	
		R_Y		0.297	0.317	0.337	—	
	Green	G_x		0.255	0.275	0.295	—	
		G_Y		0.562	0.582	0.602		
	Blue	B_x		0.120	0.140	0.160	—	
		B_Y		0.068	0.088	0.108		
Viewing angle	Hor.	Θ_L	CR>10	—	80	—	—	(1)(4) Measuring with Polarizer, Reference Only
		Θ_R		—	80	—		
	Ver.	Θ_U		—	80	—		
		Θ_D		—	80	—		
Optima View Direction		Free						(5)

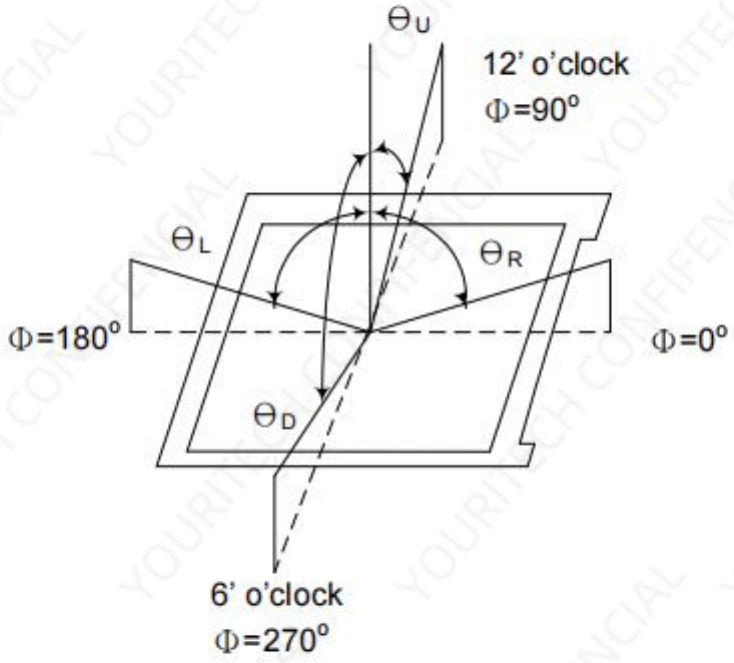
7.2 Measuring Condition

- Measuring surrounding：dark room
- Ambient temperature：25±2°C
- 15min. warm-up time.

7.3 Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

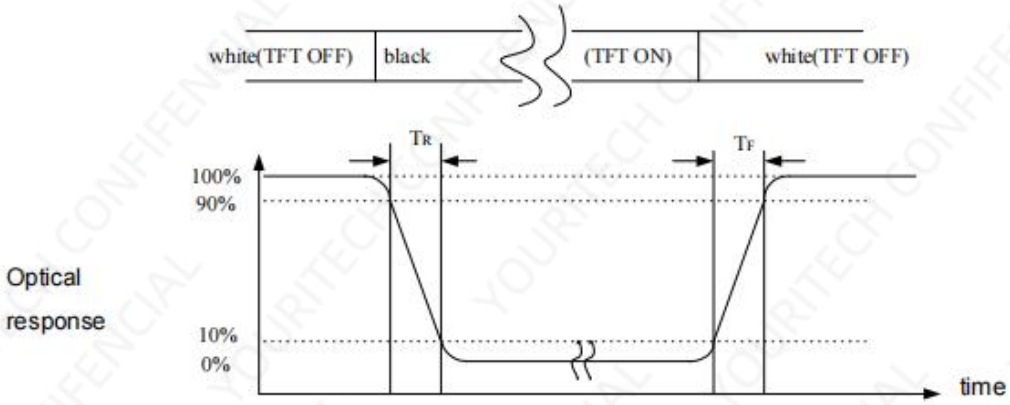
Note (1) Definition of Viewing Angle:



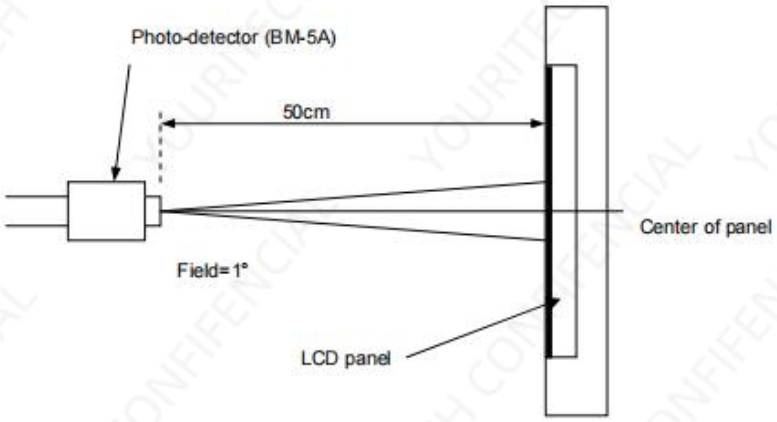
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

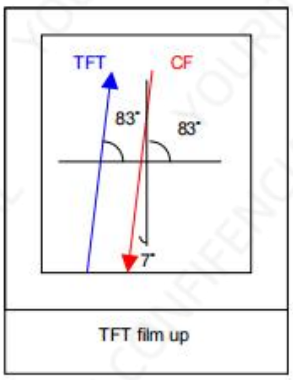
Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	60°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~70℃（30min），10 cycles	

9.Inspection standards

9.1 AQL(Acceptable Quality Level

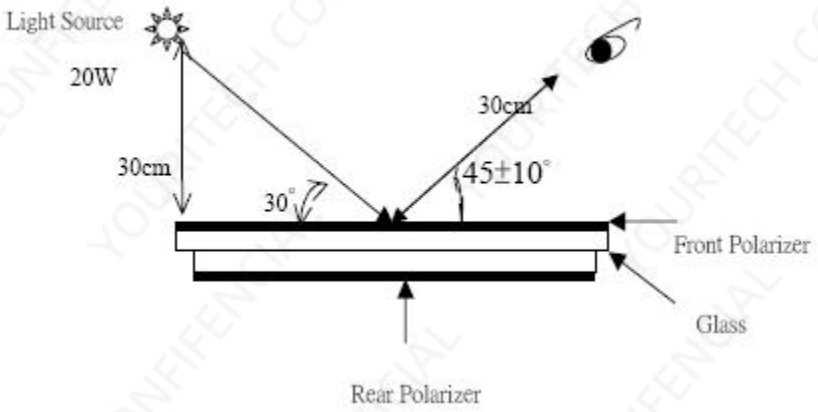
AQL of major and minor defect.

	MAJOR DEFECT	MINOR DEFECT
AQL	1.0	1.5

9.2 Basic conditions for inspection

The LCM face to us, in normal environment, the lux is 1000±200.(Darkroom's lux: 100±50),About an angle of incidence 30,a distance of 30 cm with an angle of 45 degree to check the products without uncovering the film!

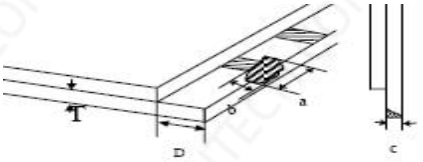
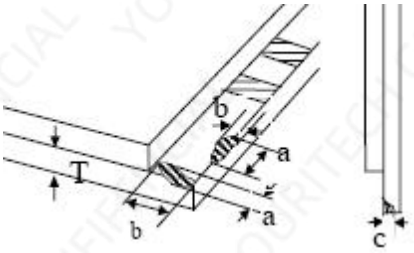
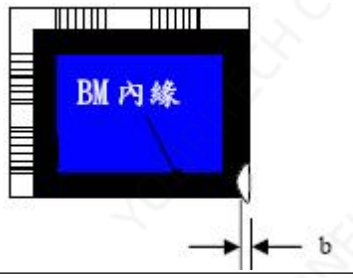
(As shown below)



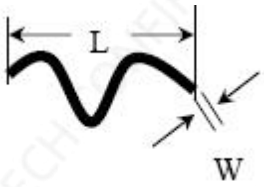
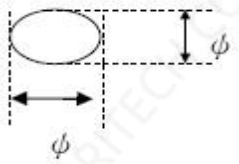
9.3 Inspection item and criteria

9.3.1 Visual inspection criterion in immobility

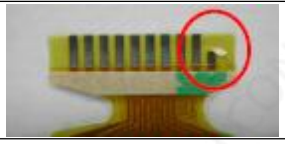
9.3.1.1Glass defect

NO	Defect item	Criteria	Remark
1	Dimension Unconformity (Major defect)	By Engineering Drawing	
2	Cracks (Major defect)	1. Linear cracks panel 【Reject】 2. Nonlinear crack contrast by limited sample	
3	Glass extrude the conductive area (minor defect)	a: disregards and no influence assemblage. 1) b≤1/3Pin width(non bonding area) 【Accept】 2)bonding area≤0. 5mm 【Accept】	A: Length, b: Width
4	Pin-side ,conductive area damaged (minor defect)	(a c: disregards) b≤1/3of effective length for bonding electrode 【Accept】	a: length, b: Width, c: Thickness 
5	Pin-side,non-conductive area damaged (minor defect)	1)Damage area don't touch the ITO (Inclueling contraposition mark, except scribing mark) 【Accept】 2)C<T b≦BM1/3of width 【Accept】 3)c=T b not touch the seal glue 【Accept】 4)a disregards	a: Length, b: Width c: Thickness 
6	Non-pin-side damage (minor defect)	c<T 1)b exceeds 1/3Bm 【Reject】 c=T b not touch the seal glue 【Reject】	c: Thickness b: width of damage 

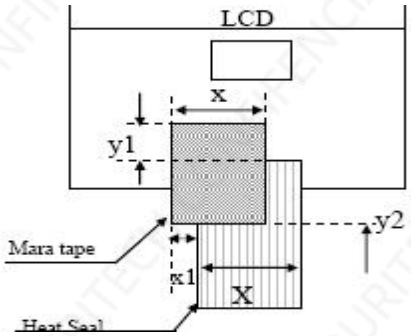
9.3.1.2 LCD appearance defect(View area)

NO	Defect item	Criteria		Remark
1	Fiber、glass cratch、polarizer scratch/folded (minor defect)	Specification	Allowable	note1:L: Length, W: Width note2: disregard if out of AA 
		W≦0.03mm	disregard	
		0.03mm<W≦0.05mm; L≦4.0mm	2	
		0.05mm<W≦0.1mm; L≦4.0mm	1	
		W>0.1mm;L>4.0mm	0	
2	Polarizer bubble、concave and convex (minor defect)	Φ≦0.2mm	disregard	note1: Φ=(L+W)/2, L:Length, W :Width note2:disregard if out of AA
		0.2mm<Φ≦0.3mm	2	
		0.3mm<Φ≦0.5mm	1	
		0.5mm<Φ	0	
3	Black dots、dirty dots、impurities、eye winker (minor defect)	Φ≦0.15mm	disregard	note2:disregard if out of AA 
		0.15mm<Φ≦0.25mm	2	
		0.25mm<Φ≦0.3mm	1	
		0.3mm<Φ	0	
4	Polarizer prick (minor defect)	Φ≦0.1mm	disregard	note1: Φ=(L+W)/2, L=Length, W=Width note2:the distance between two dots>5mm
		0.1mm<Φ≦0.25mm	3	
		Φ>0.25mm	0	

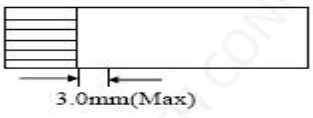
9.3.1.3 FPC

NO	Defect item	Criteria		Remark
1	Copper screen peel (minor defect)	Copper screen peel 【Reject】		
2	No release tape or peel	No release tape or peel 【Reject】		
3	Dirty dot and impurity of FPC for customer using side (minor defect)	Specification	Allowable	Note1: Cannot have stride ITO impurities
		Φ≦0.3mm	2	
		Φ>0.3	0	

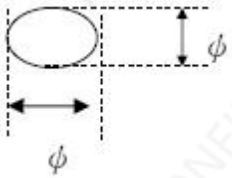
9.3.1.4Black tape &Mara tape

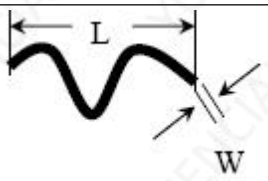
NO	Defect item	Criteria	Remark
1	FPC or H/S black tape (minor defect)	1. shift spec: 1) glue to the polarize 【Reject】 2) IC bare 【Reject】 2. left-and-right spec: 1)exceed of FPC edge or H-S edge【Reject】 2) IC bare 【Reject】	
2	No black tape (major defect)	No black tape 【Reject】	
3	Tape position mistake (minor defect)	Not by engineering drawing	
4	Mara tape defect (minor defect)	Peel before pulling the protecting film 【Reject】	

9.3.1.5Silicon and Taffy glue

NO	Defect item	Criteria	Remark
1	Quantity of silicon (major defect)	Uncover the ITO and circuit area 【Reject】	note: compared by engineering
2	Taffy glue (major defect)	1.Uncover the reveal copper area 【Reject】 2.Cover layer 0.3mm(Min)~3.0mm(Max) 【Reject】	note: if customer has special requirement, refer to the technical document 
3	Depth of glue covering (major defect)	Depth of glue covering overtop front Polarizer 【Reject】	Except of the special requirement

9.3.2Electrical criteria

NO	Defect item	Criteria	Remark	
1	No display (major defect)	No display 【Reject】		
2	Missing line (major defect)	Missing line 【Reject】		
3	Seg-com light and dark (major defect)	Seg-com light and dark 【Reject】	ND filter 2% test	
4	No display in immobility (major defect)	No display in immobility 【Reject】		
5	Flicker of Pattern (major defect)	Flicker of Pattern 【Reject】		
6	Mura (major defect)	ND filter 2%test		
7	Over current (major defect)	Over current 【Reject】		
8	Voltage out of specification (major defect)	Voltage out of specification 【Reject】		
9	Pattern blur, error code (major defect)	Pattern blur, error code 【Reject】		
10	Dark light, Flicker (major defect)	Dark light, Flicker 【Reject】		
11	Black/white dots、Dirty dots、eye winker (major defect)	Specification	Allowable	Note1:disregard if out of AA 
		ϕ ≦0.15mm	disregard	
		0.15mm< ϕ ≦0. 25mm	2	
		0.25mm< ϕ ≦0. 3mm	1	
		0.3mm< ϕ	0	
12	Fiber、glass crutch、Polarizer scratch/folded (major defect)	W≦0.03mm	disregard	Note1:L: Length, W: Width Note2: disregard if out of AA
		0.03mm<W≦ 0. 0. 05mm L≤4. 0mm	2	
		0.05mm<W≦0. 1mm	1	

		L≤4.0mm		
		W>0.1mm;L>4.0mm	0	