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SPECIFICATION FOR LCM+CTP Module

MODULE No:	ET026HV21-KT
CUSTOMER:	

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Revision History

Date	Rev. No.	Page	Summary
2019.08.20	V1.0	ALL	FIRST ISSUE

Contents

1.Basic Specifications

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorpho us silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Pan el, driver circuit, capacitance touch panel, back-light unit. The resolution of a 2.6 " TFT-LCD contains 320x432 pixels, and can display up to 65K/262K/16.7M colors.

1.1 TFT Features

GeneralInformation Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	39.84(H)*53.78 (V) (2.6 inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K/16.7M	colors	-
Number of pixels	320(RGB)*432	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.1245(H)*0.1245(V)	mm	-
Viewing angle	Wide angle	o'clock	-
Controller IC	ILI9488	-	-
Display mode	Normally Black /Transflective	-	-
LCM Interface	8/9/16/18/24 BIT MCU 3/4-line SPI+16/18/24 BIT RGB 3-line/4-line Serial Interface	-	
Operating temperature	-30～+85	℃	-
Storage temperature	-40～+85	℃	-
Module bonding technology	Use Tape bonding between LCM and CTP		

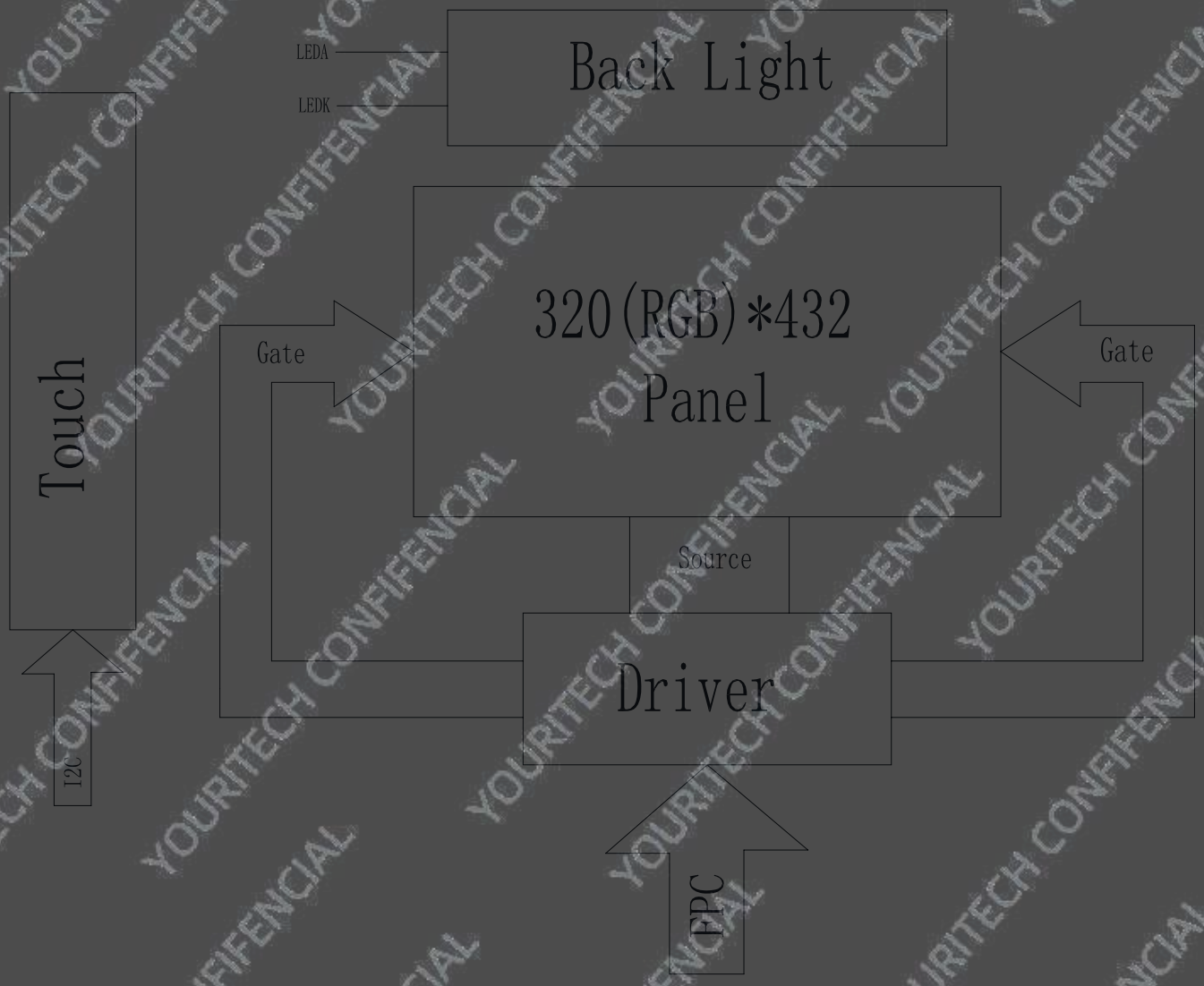
1.2 CTP Features

Resolution	320(H)*432(V)	-	
Structure	G+G	-	
Controller IC	FT5436	-	
Interface	I2C	-	
Slave Adress	0x38(7bit)/8bit:0x70(Write) 0x71(Read)	-	
Touch mode	Multipoint and Gestures	-	-

1.3 Mechanical Information

Module size	Horizontal(H)		46.76		mm	-
	Vertical(V)		65.85		mm	-
	Depth(D)		4.26		mm	-
Weight			25		g	-

2. Block Diagram



3. Outline dimension

4. Input terminal Pin Assignment

4.1 TFT PIN Define

1	GND	Ground.	P
2	LEDA	Cathode pin of backlight.	P
3	LEDK	Cathode pin OF backlight	P
4	NC	--	P
5	CSX	Chip select input pin ("Low" enable). fix this pin at IOVCC or GND when not in use.	I
6	DCX	Display data/command selection pin	I
7	WR(SPI-SCL)	DBI Type B: WRX pin, serves as a write signal DBI Type C: SCL pin as Serial Clock when operates in the seri al interface	I
8	RDX	Serves as a read signal and MCU read data at the rising edge. fix this pin at IOVCC or GND when not in use.	I
9	SDA	Serial input signal.The data is applied on the rising edge of the SCL signal. If not used, fix this pin at IOVCC or GND.	I/O
10	SDO	Serial data output pin in serial bus system interface. If not used, please open this pin.	O
11-34	DB0-DB23	24-bit parallel bi-directional data bus for MCU system and RGB interface mode . Fix to GND level when not in use	I/O
35	DE	Data enable signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.	I
36	PCLK	Dot clock signal for RGB interface operation Fix this pin at IOVCC or GND when not in use.	I
37	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at IOVCC or GND when not in use	I
38	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.	I

39	RESX	This signal will reset the device and must be applied to properly initialize the chip.	I
40	IM2	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. Fix this pin at IOVCC and GND.	I
41	IM1		
42	IM0		
43	VCI	Supply voltage(3.3V).	P
44	VCI		
45	IOVCC	Supply voltage For IO(1.8-3.3V)	P
46	IOVCC		
47	YU(NC)	Touch panel Top Film Terminal	A/D
48	XL(NC)	Touch panel LEFT Glass Terminal	A/D
49	YD(NC)	Touch panel Bottom Film Terminal	A/D
50	XR(NC)	Touch panel Right Glass Terminal	A/D
51	GND	Ground.	P

4.2 CTP PIN Define

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground	P
2	VDDIO	I/O power supply voltage.	P
3	VDD	Supply voltage	P
4	SCL	I2C clock input	I
5	SDA	I2C data input and output	I
6	INT	External interrupt to the host	I
7	RST	External Reset, Low is active	I
8	GND	Ground	P

5. LCD Optical Characteristics

5.1 Optical specification

5.1.1 Transmissive mode

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	note
Contrast Ratio		CR	Θ=0 Normal viewing angle	400	500	--		Note1
Response time	Rising	$T_{R+}T_F$		--	25	50	msec	Note1
	Falling							
Color gamut		S(%)		--	50	--	%	
Color Filter Chromacicity	White	W_X		0.2405	0.2805	0.3205		
		W_Y		0.2717	0.3117	0.3517		
	Red	R_X		0.5412	0.5812	0.6212		
		R_Y		0.2999	0.3399	0.3799		
	Green	G_X		0.2919	0.3319	0.3719		
		G_Y		0.5311	0.5711	0.6111		
	Blue	B_X		0.1152	0.1552	0.1952		
		B_Y		0.0478	0.0878	0.1278		
Viewing angle	Hor.	Θ_{21}	CR>10	60	80	--	deg	Note1
		Θ_{22}		60	80	--		
	Ver.	Θ_{12}		60	80	--		
		Θ_{11}		60	80	--		
Option View Direction		Wide angle						

5.1.2 Reflective mode (Not driving the back light condition)

Item	Symbol	Specifications			unit	Note
Reflection Ratio （With Polarizer）	R （θ＝ϕ＝0°）	1	2	-	%	Here the data are design value.
Reflective Contrast Ratio	Cr （θ＝0°）	-	5	-		Note1
Viewing angle (Cr≥ 2)*	Θ21	-	45	-	deg	Note1
	Θ22	-	45	-		
	Θ12	-	45	-		
	Θ11	-	45	-		

Note1：The polarizers are SRCG31APN2HC5(Top) and SRCH31APT2(Bottom)

5.2 Measuring Condition

- Measuring surrounding：dark room
- Ambient temperature：25±2℃
- 15min. warm-up time.

5.3 Measuring Equipment

[1]Transmittance (T%)

The transmittance of the panel including polarizers is measured with electrical driving.

The Transmittance is defined as:

$$Tr = \frac{I\_t}{I\_o} \times 100\%$$

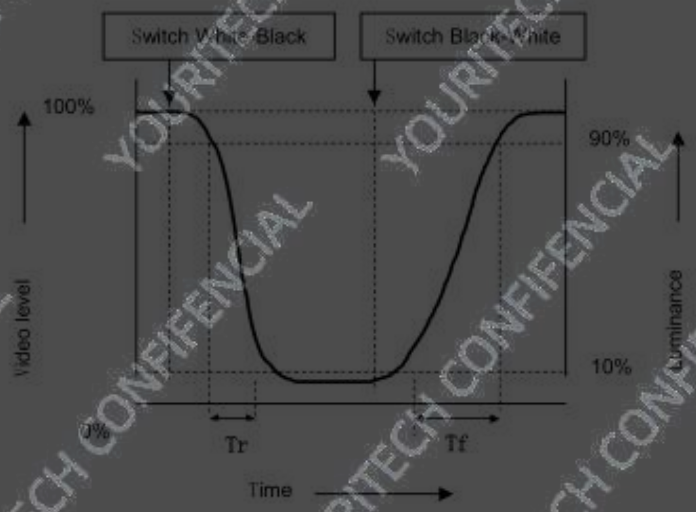
here,

I_o: the brightness of the light source.

I_t : the brightness after panel transmission.

[2] Response Time(Tr、Tf)

The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.

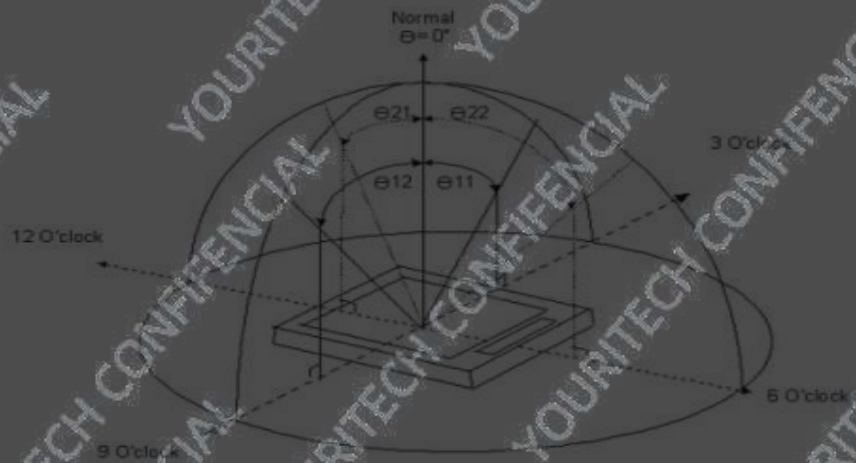


[3] Contrast ratio (Cr)

The contrast ratio (Cr), measured on a module, is the ratio between the luminance (L_w) in a full white area (R=G=B=1) and the luminance (L_d) in a dark area (R=G=B=0).

$$Cr = \frac{L\_w}{L\_d}$$

[4]Viewing angle diagram



[5] Definition of color gamut

Measuring machine:CPT-01. NTSC'S Primaries: R(x,y,Y)、G(x,y,Y)、B(x,y,Y)

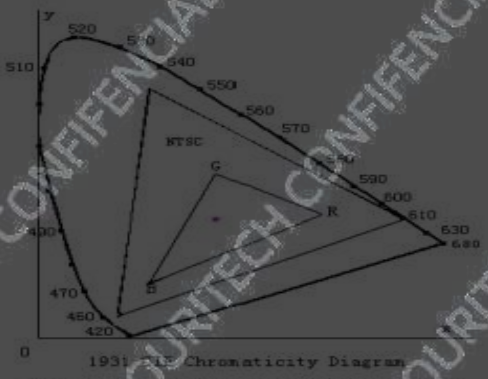


Fig. 1931 CIE chromaticity diagram

Color gamut: $S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$

6. Electrical Characteristics

6.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Digital Supply Voltage	VCI	-0.3	3.3	V
Digital interface supple Voltage	IOVCC	-0.3	3.3	V
Operating temperature	T_{OP}	-30	+85	℃
Storage temperature	T_{ST}	-40	+85	℃

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

6.2 DC Electrical Characteristics

Digital Supply Voltage	VCI	2.5	3.3	3.6	V	
Digital interface supple Voltage	IOVCC	1.65	1.8	3.3	V	
Normal mode Current consumption	IDD	--	8	--	mA	
Level input voltage	V_{IH}	0.7IOVCC		IOVCC	V	
	V_{IL}	-0.3		0.3IOVCC	V	
Level output voltage	V_{OH}	0.8IOVCC		IOVCC	V	
	V_{OL}	GND		0.2IOVCC	V	

6.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 6 chips White LED

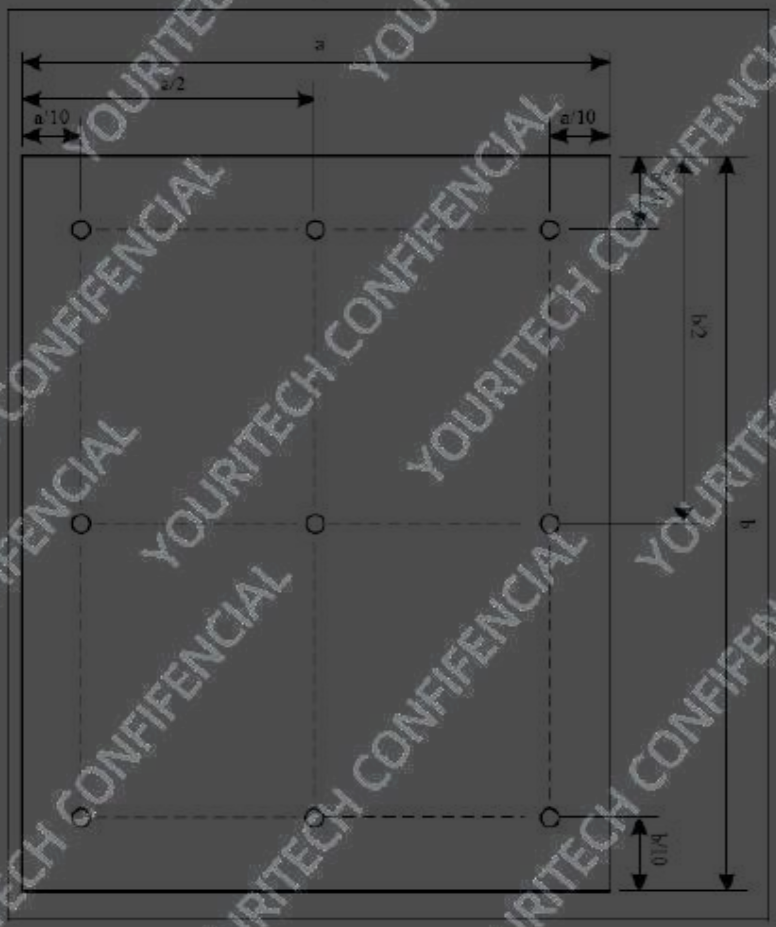
Forward Current	I_F	15	20	--	mA	
Forward Voltage	V_F	--	19.2	--	V	
LCM Luminance	LV	370	420	--	cd/m2	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.

LED(B/L) CIRCUIT

NOTE 3：Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

7. AC Characteristic

7.1 DBI Type B Timing Characteristics

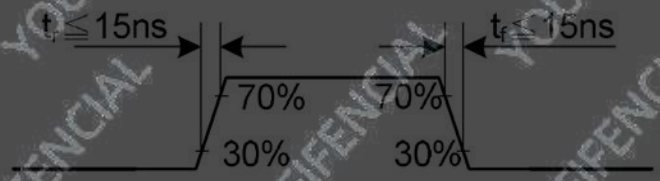
			ec			
DCX	t_{ast}	Address setup time	0	--	ms	
	t_{hat}	Address hold time (Write/Read)	0	--	us	
CSX	t_{chw}	CSX "H" pulse width	0	--	ns	
	t_{cs}	Chip Select setup time (Write)	15	--	%	
	t_{rcs}	Chip Select setup time (Read ID)	45	--	ns	
	t_{rcsfm}	Chip Select setup time (Read FM)	355	--	ns	
	t_{csf}	Chip Select Wait time (Write/Read)	0	--	ns	
WRX	t_{wc}	Write cycle	40	--	ns	
	t_{wrh}	Write Control pulse H duration	15	--	ns	
	t_{wrl}	Write Control pulse L duration	15	--	ns	
RDX(FM)	t_{rcfm}	Read Cycle (FM)	450	--	ns	When read from Frame Memory
	t_{rdhfm}	Read Control H duration (FM)	90	--	ns	
	t_{rdlfm}	Read Control L duration (FM)	355	--	ns	
RDX(ID)	t_{rc}	Read cycle (ID)	160	--	ns	When read ID data

	t_{rdh}	Read Control pulse H duration	90	--	ns	
	t_{rdl}	Read Control pulse L duration	45	--	ns	
DB[23:0], DB[17:0], DB[15:0], DB [8:0], DB [7:0]	t_{dst}	Write data setup time	10	--	ns	For maximum, CL=30pF For minimum, CL=8pF
	t_{dht}	Write data hold time	10	--	ns	
	t_{rat}	Read access time	--	40	ns	
	t_{ratfm}	Read access time	--	340	ns	
	t_{rod}	Read output disable time	20	80	ns	

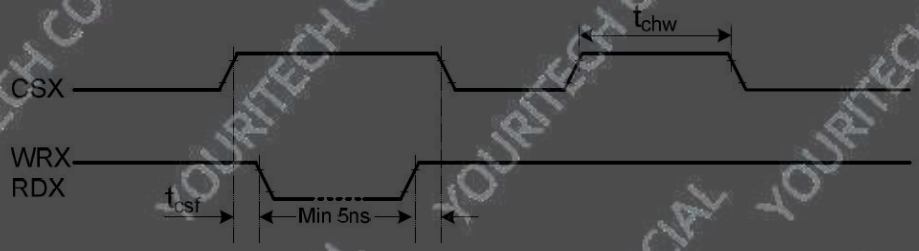
Note: 1. Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V

2. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.

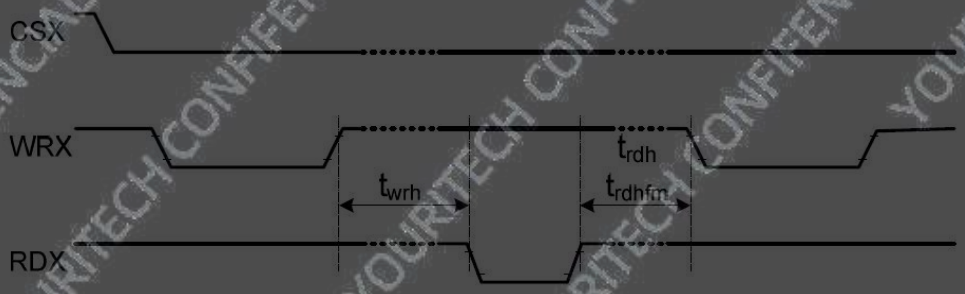
3. Input signal rising time and falling time:



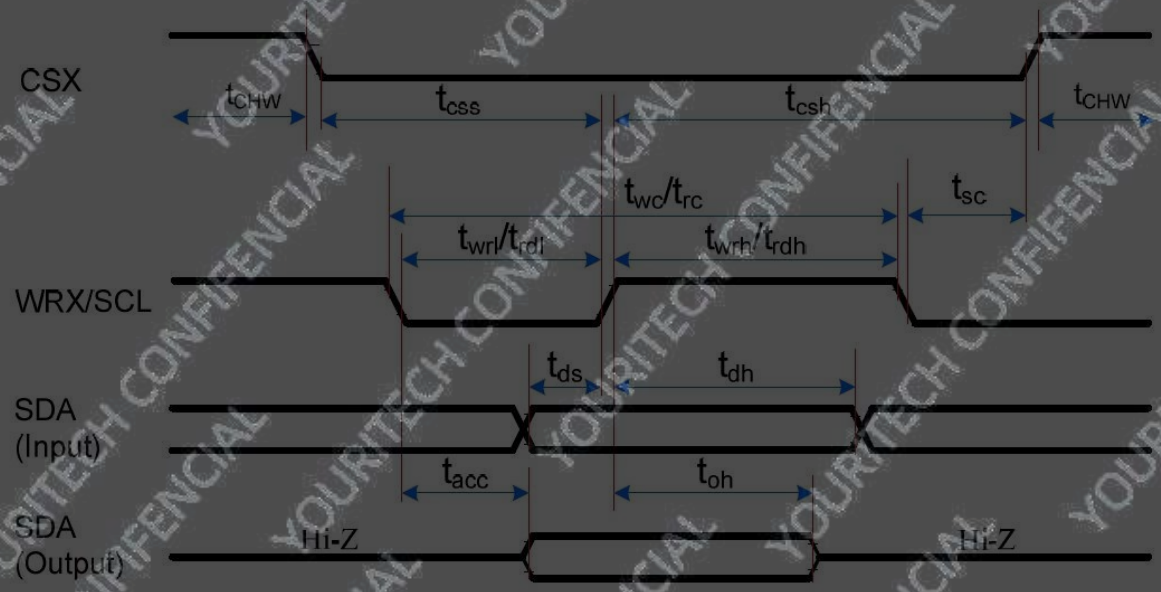
4.The CSX timing:



5. The Write to Read or the Read to Write timing:



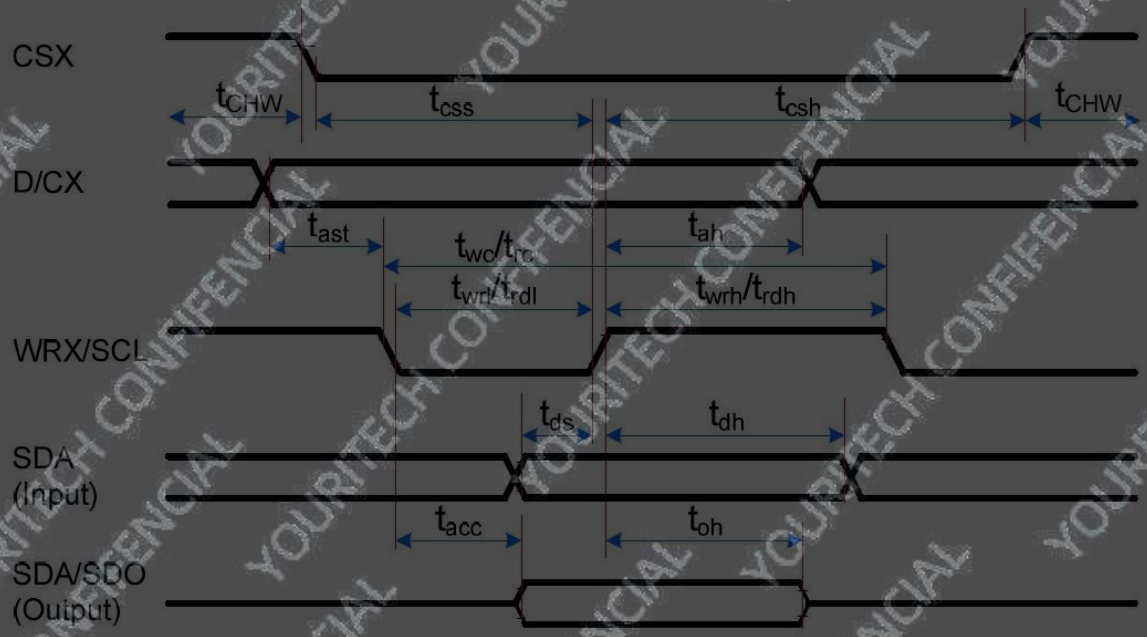
7.2 DBI Type C Option 1 (3-Line SPI System) Timing Characteristics



			p			
CSX	t_{sc}	SCL-CSX	15	--	ns	
	t_{chw}	CSX H Pulse Width	40	--	ns	
	t_{css}	Chip select time (Write)	60	--	ns	
	t_{csh}	Chip select hold time (Read)	65			
SCL	t_{wc}	Serial clock cycle (Write)	66	--	ns	
	t_{wrhf}	SCL H pulse width (Write)	15	--	ns	
	t_{wrl}	SCL L pulse width (Write)	15	--	ns	
	t_{rc}	Serial clock cycle (Read)	150	--	ns	
	t_{rdh}	SCL H pulse width (Read)	60	--	ns	
	t_{rdl}	SCL L pulse width (Read)	60	--	ns	
SDA (Input)	t_{ds}	Read cycle (ID)	10	--	ns	
	t_{dh}	Read Control pulse H duration	10	--	ns	
SDA/SDO (Output)	t_{acc}	Write data setup time	10	50	ns	For maximum CL=30pF
	t_{od}	Write data hold time	15	50	ns	

NOTES: Ta = -30 to 70 °C, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns

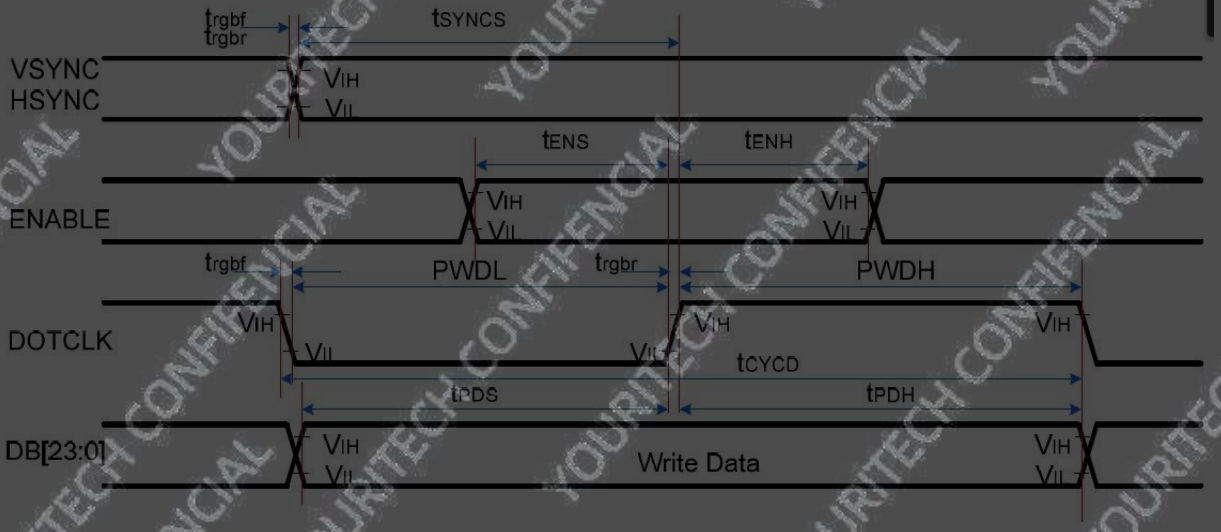
7.3 DBI Type C Option 3 (4-Line SPI System) Timing Characteristics



CSX	t_{css}	Chip select time (Write)	15	--	ns	
	t_{csh}	Chip select hold time (Read)	15	--	ns	
	t_{chw}	CS H pulse width	40	--	ns	
SCL	t_{wc}	Serial clock cycle (Write)	50	--	ns	
	t_{wrhf}	SCL H pulse width (Write)	10	--	ns	
	t_{wrl}	SCL L pulse width (Write)	10	--	ns	
	t_{rc}	Serial clock cycle (Read)	150	--	ns	
	t_{rdh}	SCL H pulse width (Read)	60	--	ns	
	t_{rdl}	SCL L pulse width (Read)	60	--	ns	
D/CX	t_{as}	D/CX setup time	10	--	ns	
	t_{ah}	D/CX hold time (Write/Read)	10	--	ns	
SDA (Input)	t_{ds}	Read cycle (ID)	10	--	ns	
	t_{dh}	Read Control pulse H duration	10	--	ns	
SDA/SDO (Output)	t_{acc}	Write data setup time	10	50	ns	For maximum CL=30pF
	t_{od}	Write data hold time	15	50	ns	For minimum CL=8pF

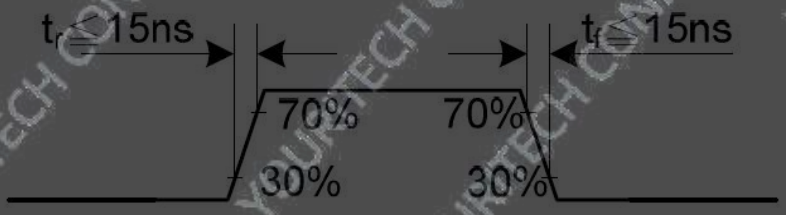
1. *Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V, T = 10+/-0.5ns.*
2. *Does not include signal rising and falling times.*

7.4 DPI (Display Parallel 16-/18-/24-bit interface) Timing Characteristics



			p			
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	--	ns	16-/18-/24-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	--	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	--	ns	
	t_{ENH}	ENABLE hold time	15	--	ns	
DB[23:0]	t_{POS}	Data setup time	15	--	ns	
	t_{POH}	Data hold time	15	--	ns	
DOTCLK	PWDH	DOTCLK high-level period	20	--	ns	
	PWDL	DOTCLK low-level period	20	--	ns	
	t_{CYCD}	DOTCLK cycle time	50	--	ns	
	t_{rgbr},t_{rgbr}	DOTCLK,HSYNC,VSYNC rise/fall time	--	15	ns	

NOTES: Ta = -30 to 70 °C, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns



7.5 Reset input timing

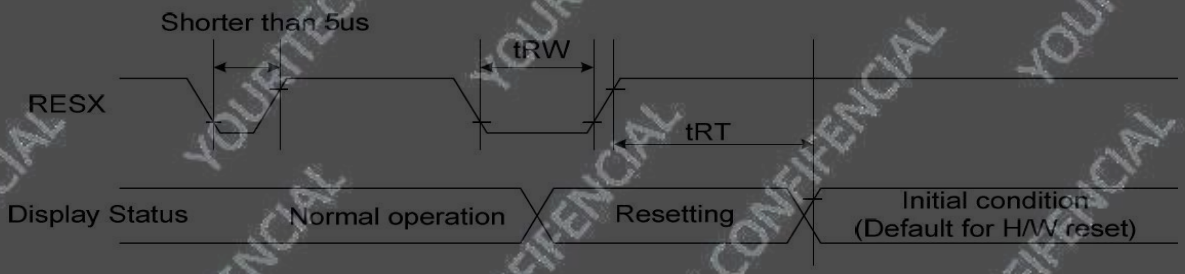


Table 39: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).
2. According to the Table 40, a spike due to an electrostatic discharge on the RESX line does not cause irregular system reset.

Table 40: Reset Description

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Reset period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains the blank state in the Sleep In mode.) and then return to the default condition for the Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

5. When Reset is applied during the Sleep In Mode.
6. When Reset is applied during the Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. The Sleep Out command also cannot be sent in 120msec.

8. CTP Specification

8.1 Electrical Characteristics

8.1.1 Absolute Maximum Rating

Power Supply Voltage	VDD	2.7	3.6	V	--
I/O Digital Voltage	VDDIO	1.8	3.6	V	--
Operating temperature	T_{OP}	-30	+85	℃	--
Storage temperature	T_{ST}	-40	+85	℃	--

8.1.2 DC Electrical Characteristics (Ta=25℃)

(Ambient temperature:25℃, AVDD=2.8V, VDDIO=1.8V or VDDIO=AVDD)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V		0.7 x IOVCC	--	IOVCC	
Input low -level voltage	VIL	V		-0.3	--	0.3 x IOVCC	
Output high -level voltage	VOH	V	IOH=3mA	0.7 x IOVCC	--	--	
Output low -level voltage	VOL	V	IOL=4.5mA	--	--	0.3 x IOVCC	
I/O leakage current	ILI	uA	Vin=0~VDD3	-1	--	1	
Current consumption （Normal operation mode）	Iopr	mA	VDD3 = 3V Ta=25℃	--	11	--	
Current consumption （Monitor mode）	Imon	mA	VDD3 = 3V Ta=25℃	--	0.43	--	
Current consumption （Sleep mode）	Islp	uA	VDD3 = 3V Ta=25℃	--	42	--	
Step-up output voltage	VDD5	V	VDD3= 2.8V		0.25		
Step-up output voltage	VDD10	V	VDD3= 2.8V		0.5		
Power Supply voltage	VDD3	V		2.7	--	3.6	

Notes: This sample data is intended for design guidance only. Values shown are typical for a 15Tx × 24Rx sensor configured at 80 Hz report rate.Actual current will depend on the particular sensor design and firmware options.

8.1.3 AC Characteristics

8.2 POWER ON/Reset Sequence

Figure 3-4 Power Cycle requirement

Figure 3-5 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

Table 3-5 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	5	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	--	200	ms
Trst	Reset time	1	--	ms

8.3 I2C Timing

FT5436 supports the I2C interfaces, which can be used by a host processor or other devices.

The I2C is always configured in the Slave mode. The data transfer format is shown in **Figure 2-4.**

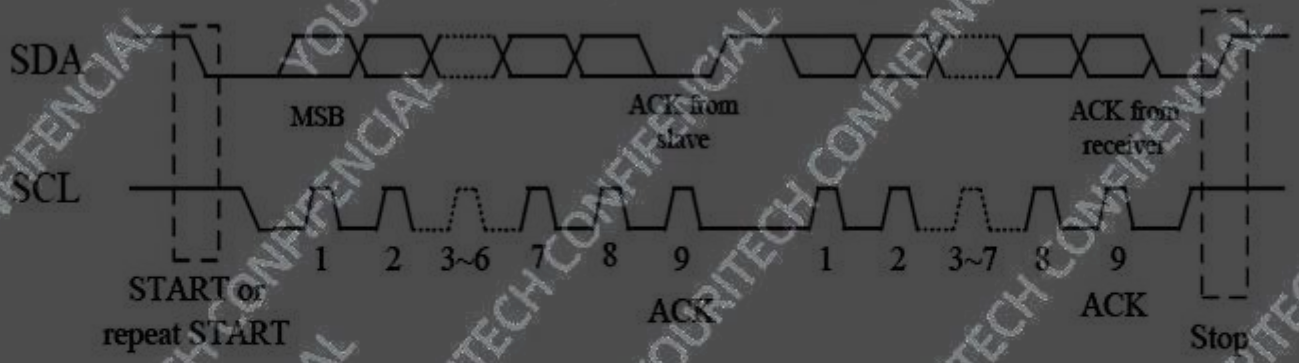


Figure 2-4 I2C Serial Data Transfer Format

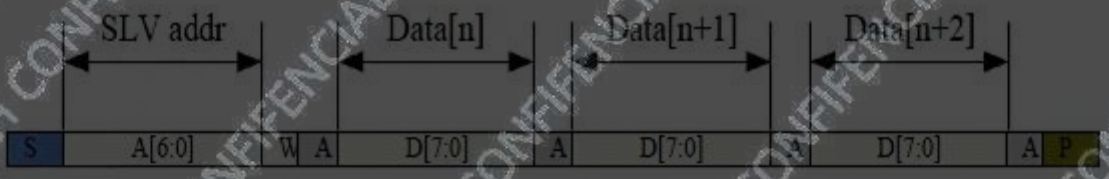


Figure 2-5 I2C master write, slave read

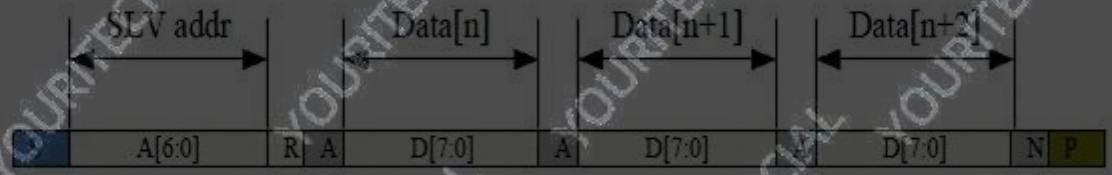


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/ W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	0	400	KHz
Bus free time between a STOP and START condition	1.3		us
Hold time (repeated) START condition	0.6		us
Data setup time	100		ns
Setup time for a repeated START condition	0.6		us
Setup Time for STOP condition	0.6		us

9. LCD Module Out-Going Quality Level

9.1 VISUAL & FUNCTION INSPECTION STANDARD

9.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

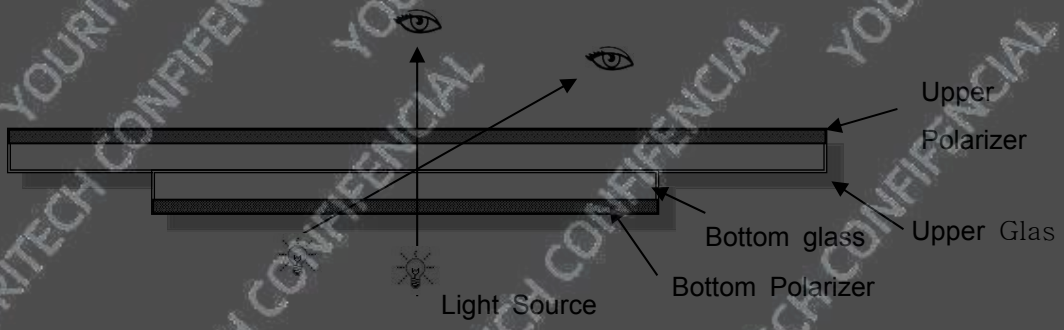
Temperature : 25±5℃

Humidity : 65%±10%RH

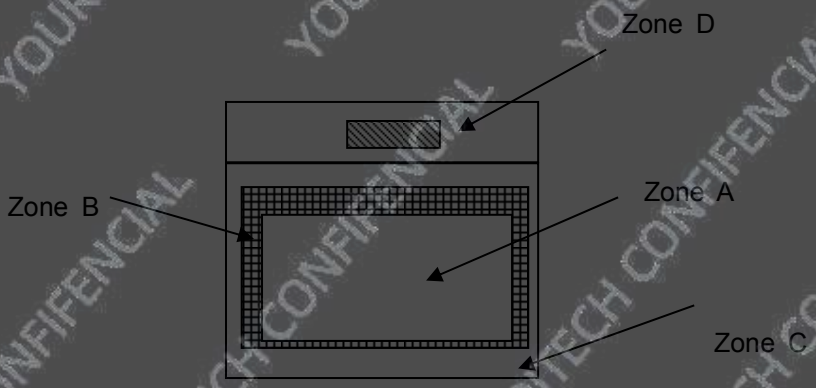
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



9.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or ap pearance after assembly by customer

9.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ

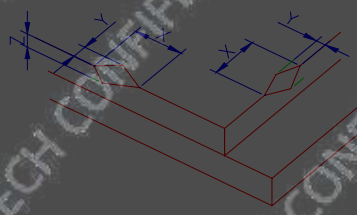
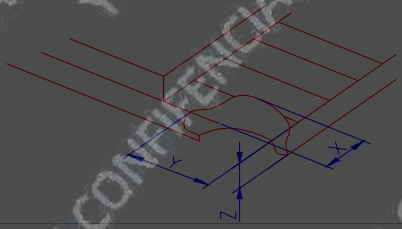
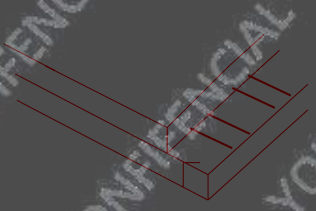
AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

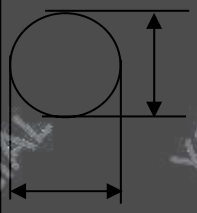
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot , Dim spot,Polarizer Bubble ; Polarizer accidented spot.	
6	Soldering appearance	Good soldering , Peeling off is not allowed.	
7	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

9.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0

Spot defect



Φ=(X+Y)/2

① light dot（LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.10	Ignore		Ignore
0.10<Φ≤0.20	3(distance≧10mm)		
0.20<Φ≤0.25	2		
Φ>0.3	0		

②Dim spot（LCD/TP/Polarizer dim dot, light leakage、dark spot）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.1	Ignore		Ignore
0.10<Φ≤0.20	3(distance≧10mm)		
0.20<Φ≤0.25	2		
Φ>0.3	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.3<Φ≤0.5	2(distance≧10mm)		
Φ>0.5	0		

④Pixel bad points（light dot，Dim dot, color dot）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.1	Ignore		Ignore
0.15<Φ≤0.2	2(distance≧10mm)		
Φ>0.2	0		

⑤ Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.3<Φ≤0.4	3(distance≧10		
0.4<Φ≤0.5	2		
Φ>0.5	0		

<table>
<tr><td>3.0</td><td>Line defect (LCD/ TP /Polarizer backligh t black/white line, scratch, stain)</td><td>
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Length(m m)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.03</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.04</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.04<W≤0.05</td><td>L≤2.0</td><td colspan="2">N≤1</td></tr>
<tr><td>0.05<W</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td></tr>
<tr><td>4.0</td><td>Electronic Comp onents SMT</td><td>Not allow missing parts , solderless connection , cold solder joint , mism atch , The positive and negative polarity opposite</td></tr>
<tr><td>5.0</td><td>Display color& B rightness</td><td>1. Color : Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness : Measuring the brightness of White screen, The measure ment standard according to the datasheet or Samples.</td></tr>
<tr><td>6.0</td><td>LCD Mura</td><td>By 5% ND filter invisible.</td></tr>
</table>

<table>
<tr><td>7.0</td><td>CTP Related</td><td>CTP Cover sensor acc idented black/white spot</td><td>
<table>
<tr><td rowspan="2">Size Φ(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.1<Φ≤0.2</td><td colspan="2">3 （distance≧10mm）</td></tr>
<tr><td>0.20<Φ≤0.25</td><td colspan="2">2</td></tr>
<tr><td>Φ＞0.3</td><td colspan="2">0</td></tr>
</table>
</td></tr>
</table>

CTP Cover scratch

Width(mm)	Ignore (mm)	Acceptable Qty		
		A	B	C
Φ≤0.05	Ignore	Ignore		
0.05<W≤0.06	L≤4.0	N≤3		
0.07<W≤0.08	L≤3.0	N≤2		
0.08<W	Define as spot defect			

CTP Cover Pinhole/ Lack of ink

Size (mm) \ Zone	Acceptable Qty
	C
Φ≤0.1	Ignore
0.1<Φ≤0.2	3(distance≧10mm)
0.25<Φ≤0.3	2
Φ>0.35	0

CTP Bonding bubble/ accidented spot

Size Φ(mm)	Acceptable Qty	
	A	B
Φ≤0.1	Ignore	
0.15<Φ≤0.2	3(distance≧10mm)	
0.2<Φ≤0.25	2	
Φ>0.25	0	

Assembly deflection

beyond the edge of backlight ≤0.2mm

TP cover broken

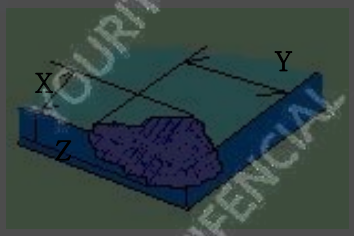
X：length

Y：width

Z：height

X	Y	Z
X≤0.5mm	Y≤0.5mm	Z<cover thickness

* Circuitry broken is not allowed.



		TP cover broken X : length Y : width Z : height	X: X≤0.3mm Y: Y≤0.3mm Z: Z<LCD thickness * Circuitry broken is not allowed.	

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

10. Reliability Test Result

10.1 Condition

Item	Condition	Inspection after test
High Temperature Operating	85℃,96HR	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-30℃, 96HR	
High Temperature Storage	85℃, 96HR	
Low Temperature Storage	-40℃, 96HR	
High Temperature & High Humidity Storage	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-30℃,30 min ↔ 85℃,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

Remark:

1.The test samples should be applied to only one test item.

2.Sample size for each test item is 5~10pcs.

3.For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.

4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

11. Cautions and Handling Precautions

11.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

11.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.