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MODEL NO : ET026LQ01-KMODEL VERSION: 01SPEC VERSION : 1.0ISSUED DATE: 2017-12-05☒ Preliminary Specification☐ Final Product Specification

Customer : _____

Approved by	Notes

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Record of Revision

[illegible]

1 General Specifications

Feature		Spec
Display Spec.	Size	2.6 inch
	Resolution	320 x RGB x 240
	Technology Type	a-Si
	Pixel Configuration	RGB Vertical Stripe
	Pixel pitch(mm)	0.165(H)*0.165(V)
	Display Mode	Transmissive/ Normally White
	Viewing Direction	12 o'clock
Mechanical Characteristics	LCM (W x H x D) (mm)	60.3*51.15*2.6
	Active Area(mm)	52.8*39.6
	With /Without TSP	Without TSP
	LED Numbers	4 LEDS
	Driver IC	ILI9342C
	Weight (g)	TBD
Electrical Characteristics	Interface	MCU/RGB
	Color Depth	262K

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180 degree shift.

Note 2: Requirements on Environmental Protection: Q/S0002

Note 3: LCM weight tolerance: $\pm 5\%$

2 Input/Output Terminals

NO.	SYMBOL	DISCRIPTION					I/O
1	GND	Ground.					P
2	GND	Ground.					P
3	IOVCC	Supply voltage(1.65-3.3V)					P
4	VCI	Supply voltage(3.3V).					P
5	IM3	Interface Selection					I
6	IM2						
7	IM0	IM3	IM2	IM0	Interface type	DB Pin in use	
		0	0	0	DBI Tyb_ 8-bit interface	DB7-DB0	
		0	1	0	DBI Tyb_ 16-bit interface	DB15-DB0	
		0	0	1	DBI Tyb_ 9-bit interface	DB8-DB0	
		0	1	1	DBI Tyb_ 18-bit interface	DB17-DB0	
		1	0	1	3-Wire 9 BIT data serial interface.	SDA SCL CS	
8	SDA	1	1	1	4-Wire 8 BIT data serial interface	SDA SCL CS RS	I
		Serial input signal.The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VCI or GND.					
9	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.					I
10	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use					I
11	DOTCLK	Dot clock signal for RGB interface operation Fix this pin at VCI or GND when not in use.					I
12	ENABLE	Data enable signal for RGB interface operation. fix this pin at VCI or GND when not in use.					I
13	RD	Serves as a read signal and MCU read data at the rising edge. fix this pin at VCI or GND when not in use.					I
14	WR(SPI-RS)	(WR): Serves as a write signal and writes data at the rising edge. 4-line system (RS): Serves as command or parameter select. Fix to IOVCC or GND level when not in use.					I
15	RS(SPI-SCL)	This pin is used to select “Data or Command” in the parallel interface. When RS = '1', data is selected. When RS = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. If not used, this pin should be connected to IOVCC or GND. RS_SCL1 is equal to RS(SCL).					I

16	CS	Chip select input pin ("Low" enable). This pin can be permanently fixed "Low" in MPU interface mode only. CSX1 is equal to CSX.	I
17	RESET	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low. RESX1 is equal to RESX.	I
18-35	DB17-DB0	18-bit parallel bi-directional data bus for MCU system and RGB interface mode Fix to GND level when not in use	I/O
36	LEDK1	Cathode pin OF backlight	P
37	LEDK2	Cathode pin OF backlight	P
38	LEDK3	Cathode pin OF backlight	P
39	LEDK4	Cathode pin OF backlight	P
40	LEDA	Anode pin of backlight	P
41	XR	Touch panel Right Glass Terminal	A/D
42	YU	Touch panel Top Film Terminal	A/D
43	XL	Touch panel LIFT Glass Terminal	A/D
44	YD	Touch panel Bottom Film Terminal	A/D
45	GND	Ground.	P

3 Absolute Maximum Ratings

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	V _{CI}	-0.3	4.2	V
Digital interface supply Voltage	IOVCC	-0.3	3.3	V
Operating temperature	T _{OP}	-20	+70	°C
Storage temperature	T _{ST}	-30	+80	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

4 Electrical Characteristics

4.1 Driving TFT LCD Panel

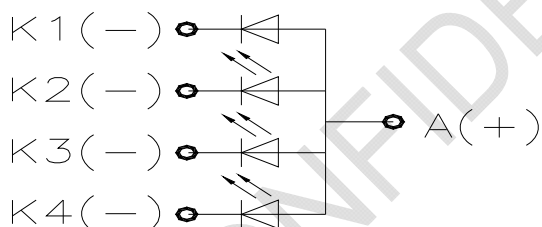
Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	V _{CI}	2.5	2.8	3.3	V	
Digital interface supply Voltage	IOVCC	1.65	1.8	3.3	V	
Normal mode Current consumption	I _{DD}	--	3	--	mA	
Level input voltage	V _{IH}	0.7IOVCC		IOVCC	V	
	V _{IL}	GND		0.3IOVCC	V	
Level output voltage	V _{OH}	0.8IOVCC		IOVCC	V	
	V _{OL}	GND		0.2IOVCC	V	

4.2 Backlight Unit

The backlight system is an edge-lighting type with 4 LED. The characteristics of the LED are shown in the following tables.

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Backlight forward voltage	V_F	-	3.2	-	V	4 LEDs
Backlight forward current	I_F	-	20	-	mA	
LED life time	-	50000	-	-	Hrs	

Note 1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: $T_a=25\pm3\text{ }^{\circ}\text{C}$, typical IL value indicated in the above table and the $f_L=50\text{k Hz}$ until the brightness becomes less than 50%.

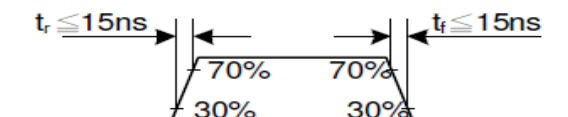


BLU CIRCUIT DIAGRAM

5.1 Display Parallel 8/9/16/18-bit Interface Timing Characteristics (8080 system)

Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	For maximum CL=30pF For minimum CL=8pF
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchwh	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $IOVCC = 1.65\text{V}$ to 2.8V , $VCI = 2.6\text{V}$ to 3.3V , $GND = 0\text{V}$.



5.2 Reset input timing

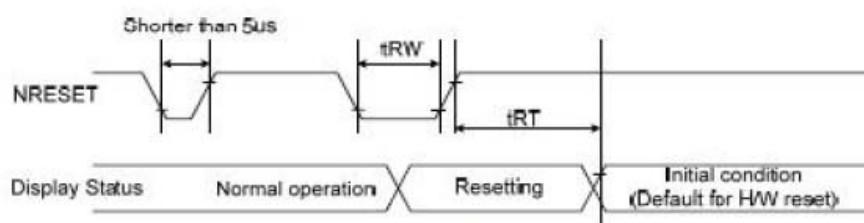


Figure 102 Reset Timing

Table 41 Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5(note 1,5) 120 (note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 43.

Table 42 Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

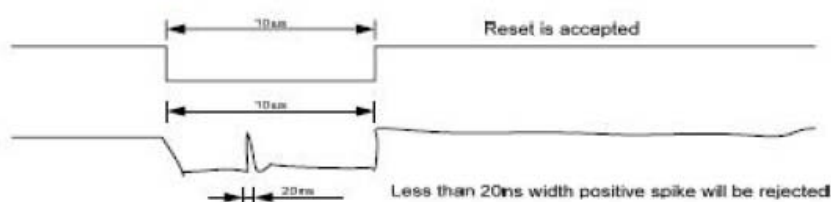
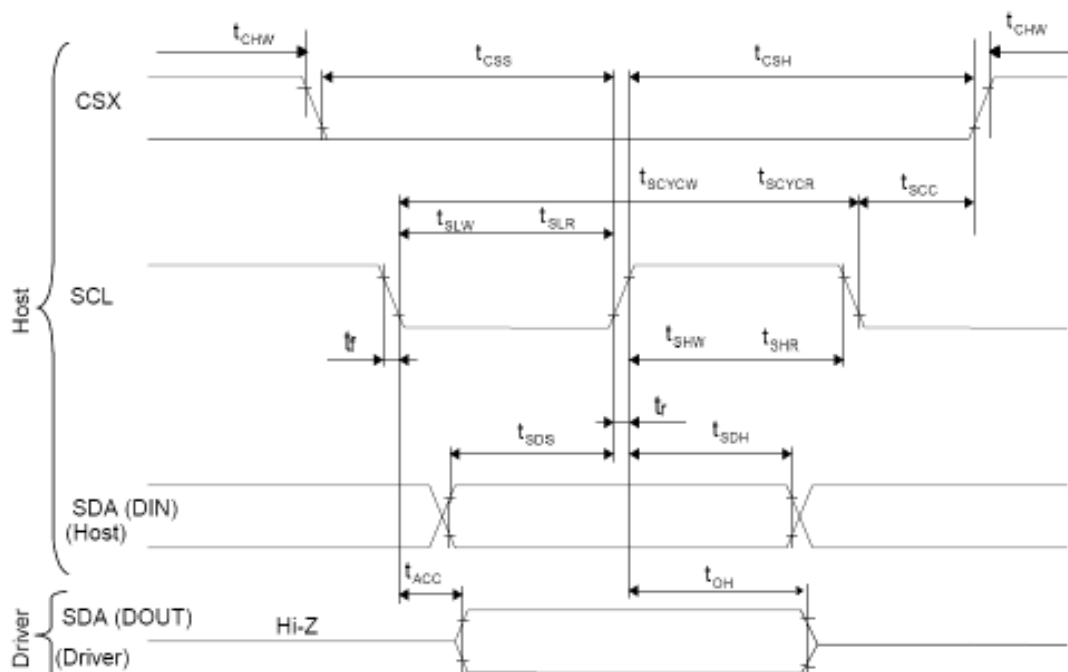


Figure 103 Positive Noise Pulse during Reset Low

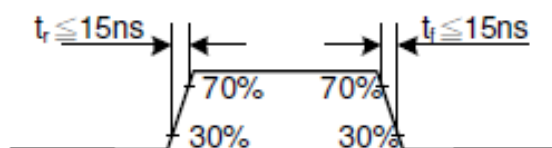
5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

5.3 Display Serial Interface Timing Characteristics (3-line SPI system)

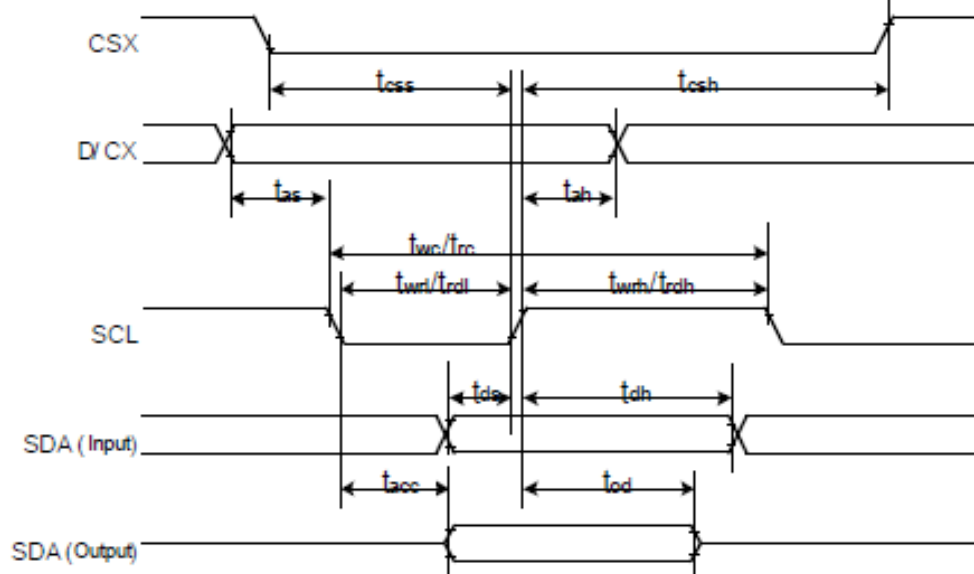


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	35	-	ns	
	tslw	SCL "L" Pulse Width (Write)	35	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	15	50	ns	
CSX	tsccl	SCL-CSX	20	-	ns	
	tchwl	CSX "H" Pulse Width	40	-	ns	
	tcssl	CSX-SCL Time(write)	30	-	ns	
	tcschl		30	-	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 2.8V, VCI=2.6V to 3.3V, AGND=GND=0V

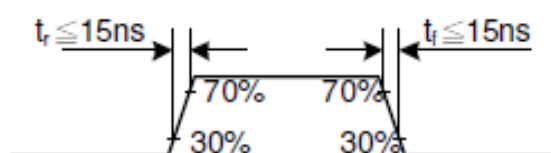


5.4 Display Serial Interface Timing Characteristics (4-line SPI system)

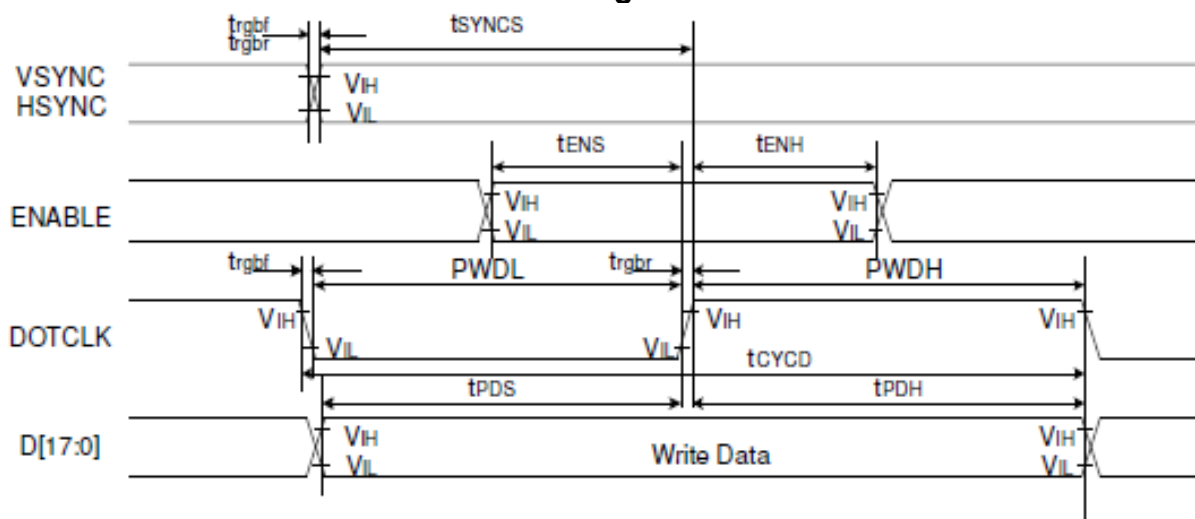


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t_{css}	Chip select time (Write)	30	-	ns	
	t_{csh}	Chip select hold time (write)	30	-	ns	
SCL	t_{wc}	Serial clock cycle (Write)	100	-	ns	
	t_{wrh}	SCL "H" pulse width (Write)	35	-	ns	
	t_{wrl}	SCL "L" pulse width (Write)	35	-	ns	
	t_{rc}	Serial clock cycle (Read)	150	-	ns	
	t_{rdh}	SCL "H" pulse width (Read)	60	-	ns	
	t_{rdl}	SCL "L" pulse width (Read)	60	-	ns	
D/CX	t_{as}	D/CX setup time	10	-		
	t_{ah}	D/CX hold time (Write / Read)	10	-		
SDA (Input)	t_{ds}	Data setup time (Write)	30	-	ns	
	t_{dh}	Data hold time (Write)	30	-	ns	
SDA (Output)	t_{acc}	Access time (Read)	-	50	ns	For maximum CL=30pF
	t_{od}	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: $T_a = 25^\circ\text{C}$, $IOVCC=1.65\text{V to }2.8\text{V}$, $VCI=2.6\text{V to }3.3\text{V}$, $AGND=GND=0\text{V}$

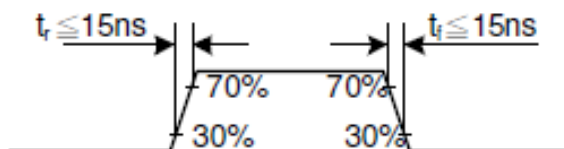


5.5 Parallel 16/18BIT RGB Interface Timing Characteristics

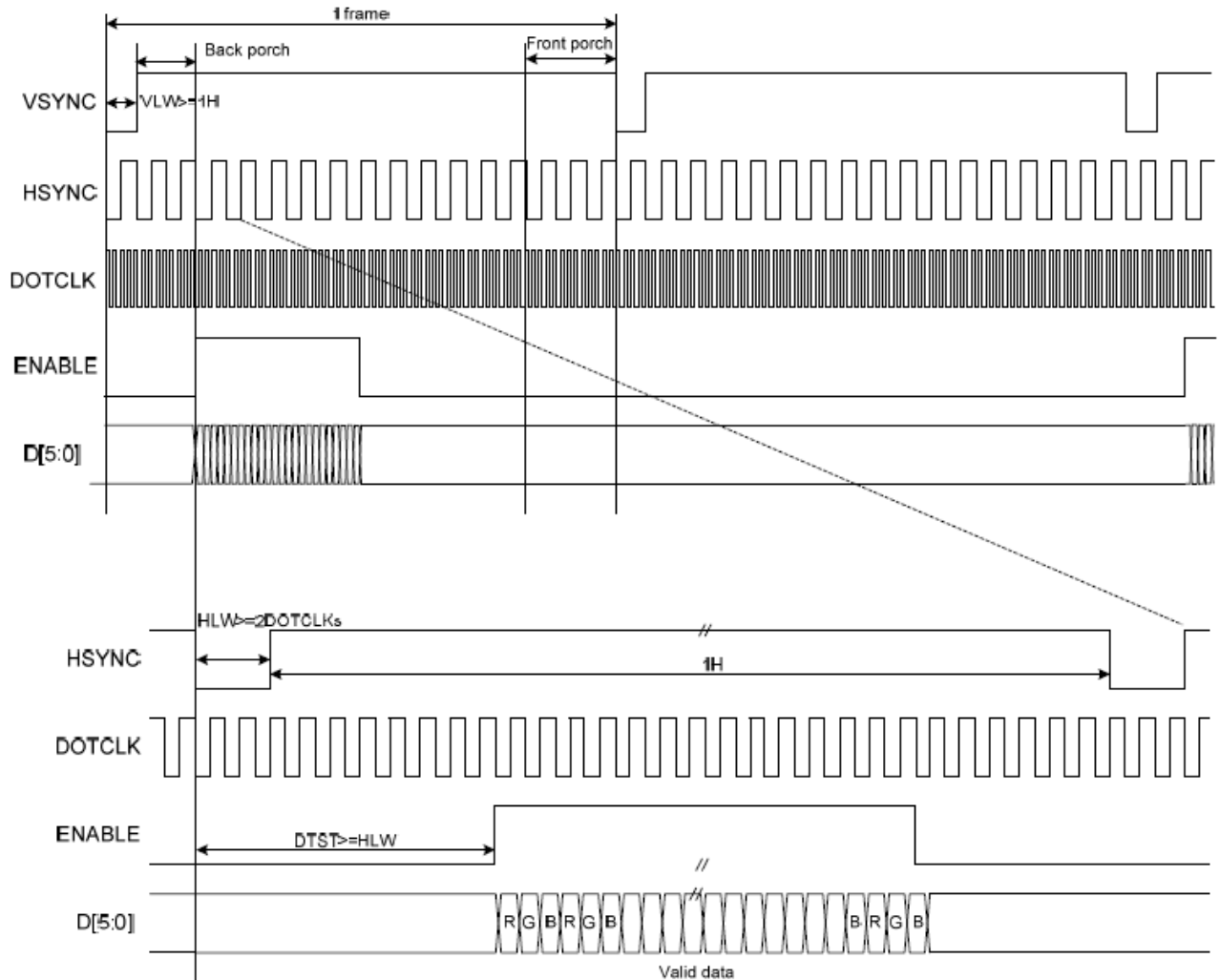


Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	33	-	ns	
	PWDL	DOTCLK low-level period	33	-	ns	
	t_{CYCD}	DOTCLK cycle time(18 bit)	100	-	ns	
	$t_{rgr}, t_{grb}, t_{rbg}$	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	6-bit bus RGB interface mode
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	25	-	ns	
	PWDL	DOTCLK low-level pulse period	25	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	$t_{rgr}, t_{grb}, t_{rbg}$	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

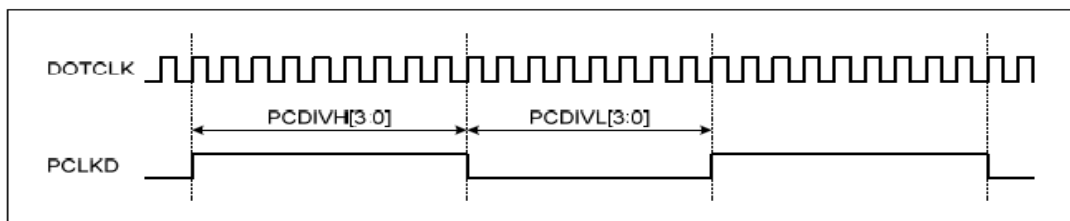
Note: $T_a = -30$ to 70°C , $IOVCC=1.65\text{V}$ to 2.8V , $VCI=2.6\text{V}$ to 3.3V , $AGND=GND=0\text{V}$



5.6 RGB Interface Timing



VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time

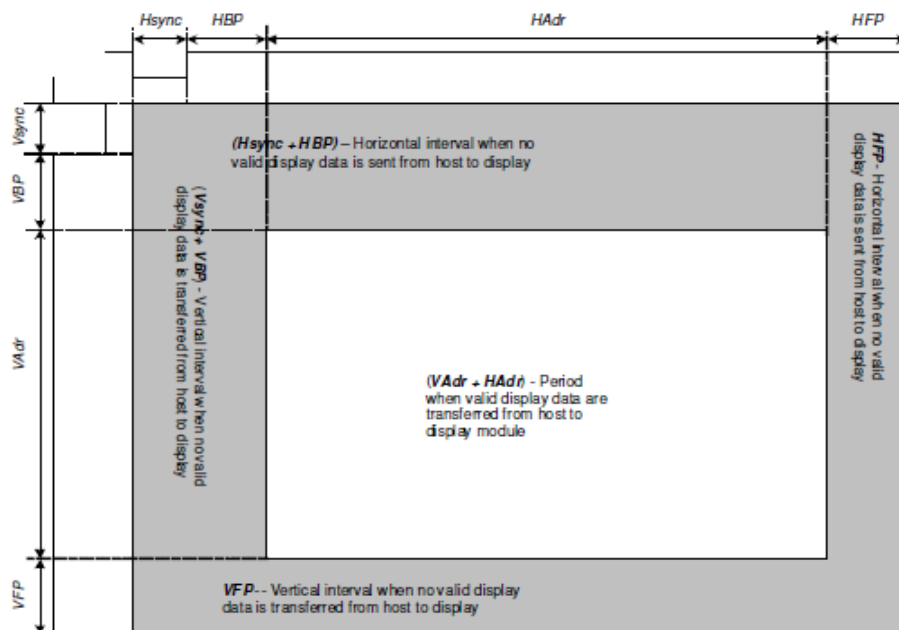


Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (B0h)" command.

Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Back Porch(By pass mode)*	HBP(BP)		58	68	200	DOTCLK
Horizontal Address	HAdr		-	320	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	240	-	Line
Vertical Front Porch	VFP		3	4	-	Line

6 Optical Characteristics

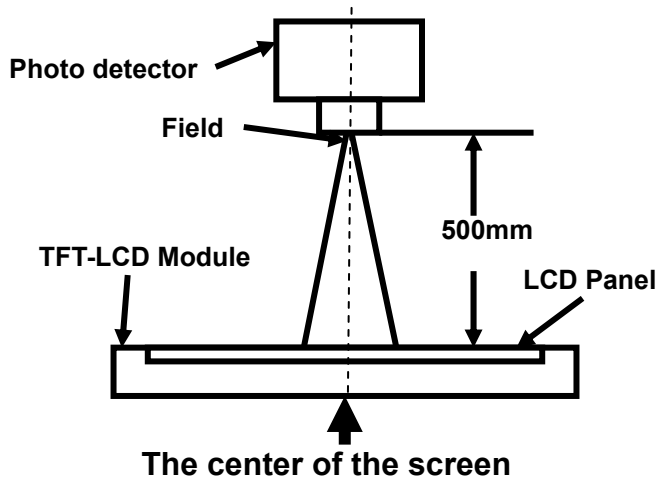
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	-	50	-	Degree	Note2,3
		θB		-	50	-		
		θL		-	45	-		
		θR		-	50	-		
Contrast Ratio		CR	θ=0°	-	400	-		Note 3
Response Time		T _{ON}	25℃	-	30	-	ms	Note 4
		T _{OFF}						
Chromaticity	White	x	Backlight is on	0.278	0.298	0.318		Note 1,5
		y		0.294	0.314	0.334		
	Red	x						Note 1,5
		y						
	Green	x						Note 1,5
		y						
	Blue	x						Note 1,5
		y						
Uniformity		U		75	80	--	%	Note 6
Reflection Ratio (With Polarizer)		R (θ=φ=0°)			2		%	
Luminance		L		250	300	-	cd/m ²	Note 7

Test Conditions:

1. $I_F = 20$ mA, and the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

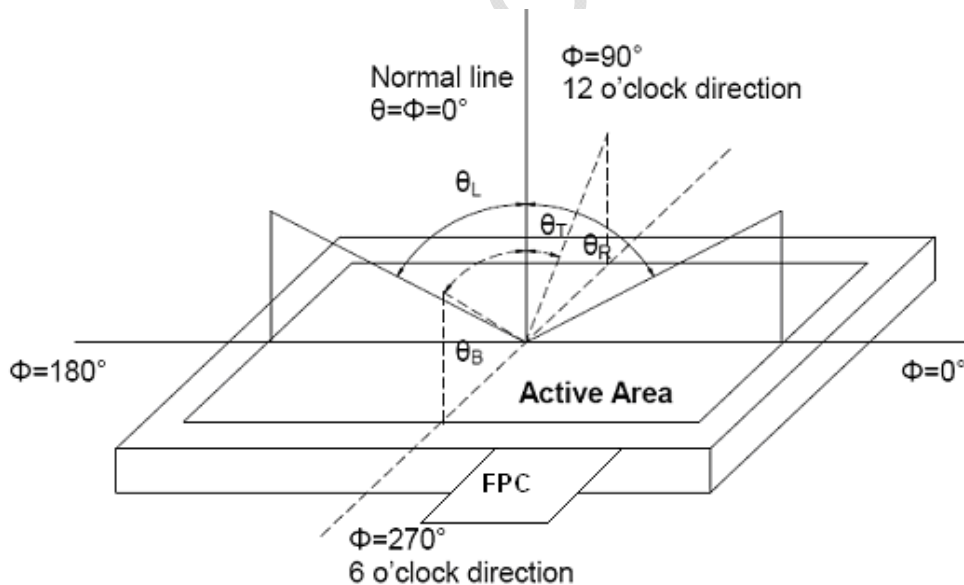
Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD.



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

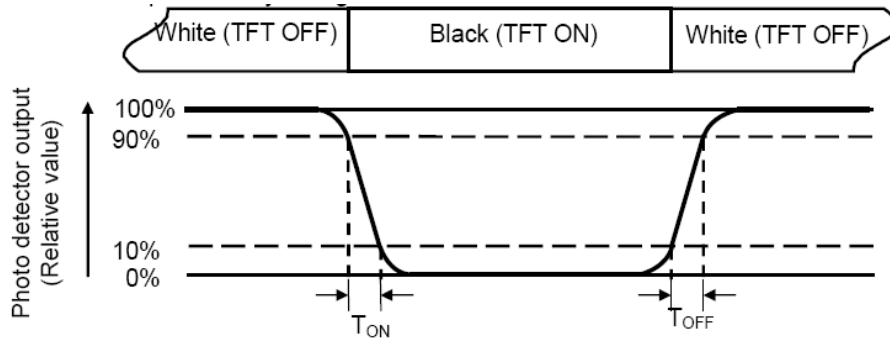
"White state ": The state is that the LCD should drive by V_{white} .

"Black state": The state is that the LCD should drive by V_{black} .

V_{white} : To be determined V_{black} : To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

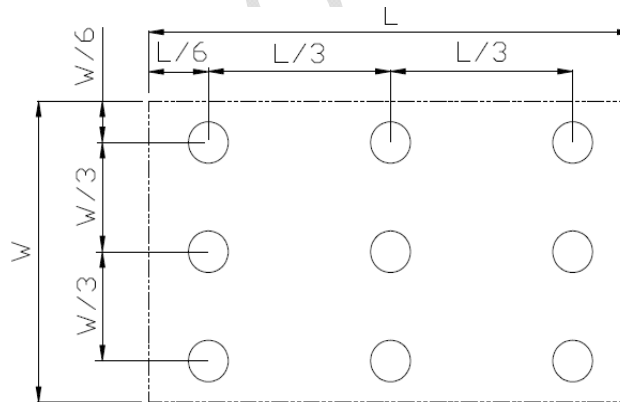
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity (U)} = L_{\min} / L_{\max}$$

L-----Active area length W----- Active area width



$L_{\max}$: The measured Maximum luminance of all measurement position.

$L_{\min}$: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

7 Environmental / Reliability Test

No	Test Item	Condition	Remarks
1	High Temperature Operation	70℃, 120Hours	IEC60068-2-1:2007 GB2423.2-2008
2	Low Temperature Operation	-20℃, 120 Hours	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	80℃, 120 Hours	IEC60068-2-1:2007 GB2423.2-2008
4	Low Temperature Storage	-30℃, 120 Hours	IEC60068-2-1:2007 GB2423.1-2008
5	Storage at High Temperature and Humidity	40℃, 90%RH, 120 Hours	IEC60068-2-78 :2001 GB/T2423.3—2006
6	Thermal Shock (non-operation)	-10℃ , 30min.<=> 60℃ , 30min. 10 Cycles	Start with cold temperature, End with high temperature, IEC60068-2-14:1984,G B2423.22-2002
7	ESD	Voltage:±8KV R:330 ohm,C:150pF Air discharge,10 times	IEC61000-4-2:2001 GB/T17626.2-2006
8	Vibration Test	10 => 55 =>10 => 55 => 10 Hz, within 1 minute;Amplitude:1.5mm. 15 minutes for each Direction (X,Y,Z)	IEC60068-2-6:1982 GB/T2423.10—1995
10	Package Drop Test	Packed, 100CM free fall 6 sides, 1 corner, 3edges	IEC60068-2-32:1990 GB/T2423.8—1995

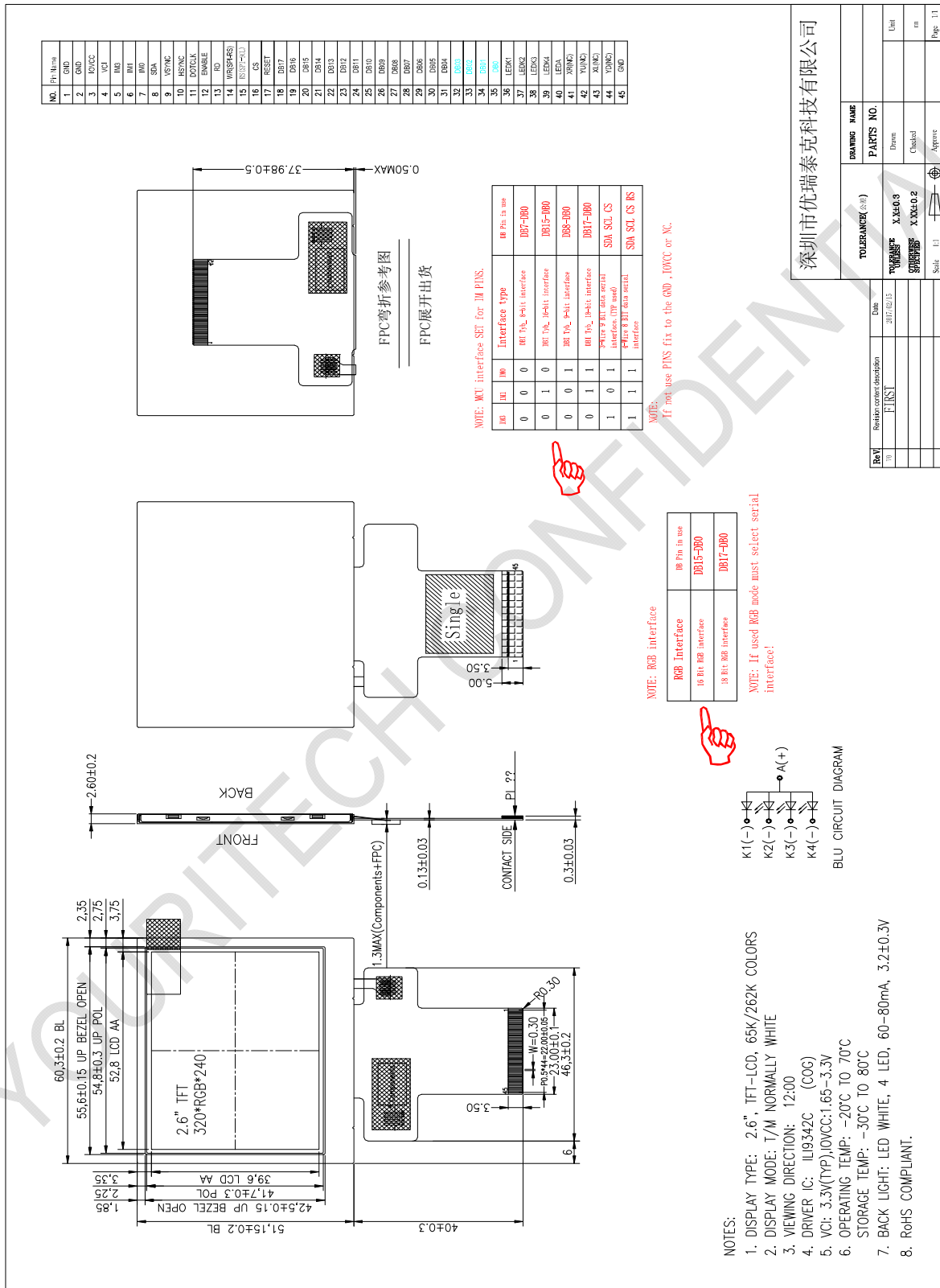
Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample.

Note3: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

8.Outline Dimension



9 Packing Drawing

TBD

10 Precautions for Use of LCD Modules

a) Handling Precautions

- i. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- ii. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.
- iii. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- iv. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- v. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:
 - Isopropyl alcohol
 - Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
 - Ketone
 - Aromatic solvents
- vi. Do not attempt to disassemble the LCD Module.
 - vii. If the logic circuit power is off, do not apply the input signals.
 - viii. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1 Be sure to ground the body when handling the LCD Modules.

10.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

b) Storage precautions

- i. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

- ii. The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ~ 40℃ Relatively humidity: ≤80%

- iii. The LCD modules should be stored in the room without acid, alkali and harmful gas.

c) Transportation Precautions

- i. The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.