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SPECIFICATION
FOR
LCM Module

MODULE:	ET026QE02-K
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2018.01.09
1.1	Second Update	2022.03.08

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
2018.01.09	V1.0	ALL	FIRST ISSUE
2022.03.08	V1.1	ALL	Second Update

Contents

1.Basic Specifications

*** Description**

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses a morphous silicon TFT as a switching device. This module is composed of a transflective type TFT-LCD Panel, driver circuit,back-light unit. The resolution of a 2.6'TFT-LCD contains 320x432 pixels, and can display up to 65K/262K colors.

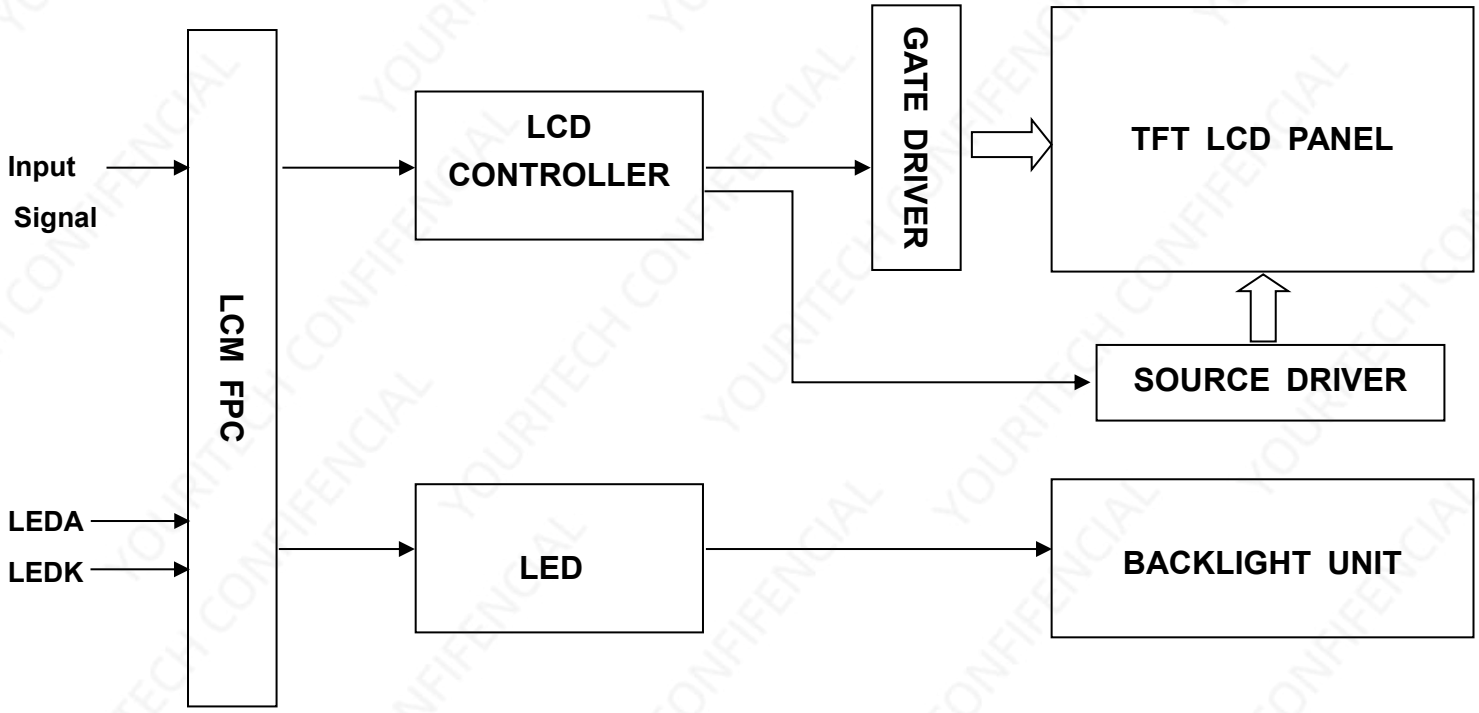
1.1 TFT Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	39.84(H)*53.78（V） (2.6 inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	320(RGB)*432	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.1245(H)*0.1245(V)	mm	-
Viewing angle	ALL	o'clock	-
Controller IC	ILI9488	-	-
Interface	one data lane MIPI Interface		
Display mode	Normally Black /Transflective	-	-
Operating temperature	-30～+85	℃	-
Storage temperature	-40～+85	℃	-

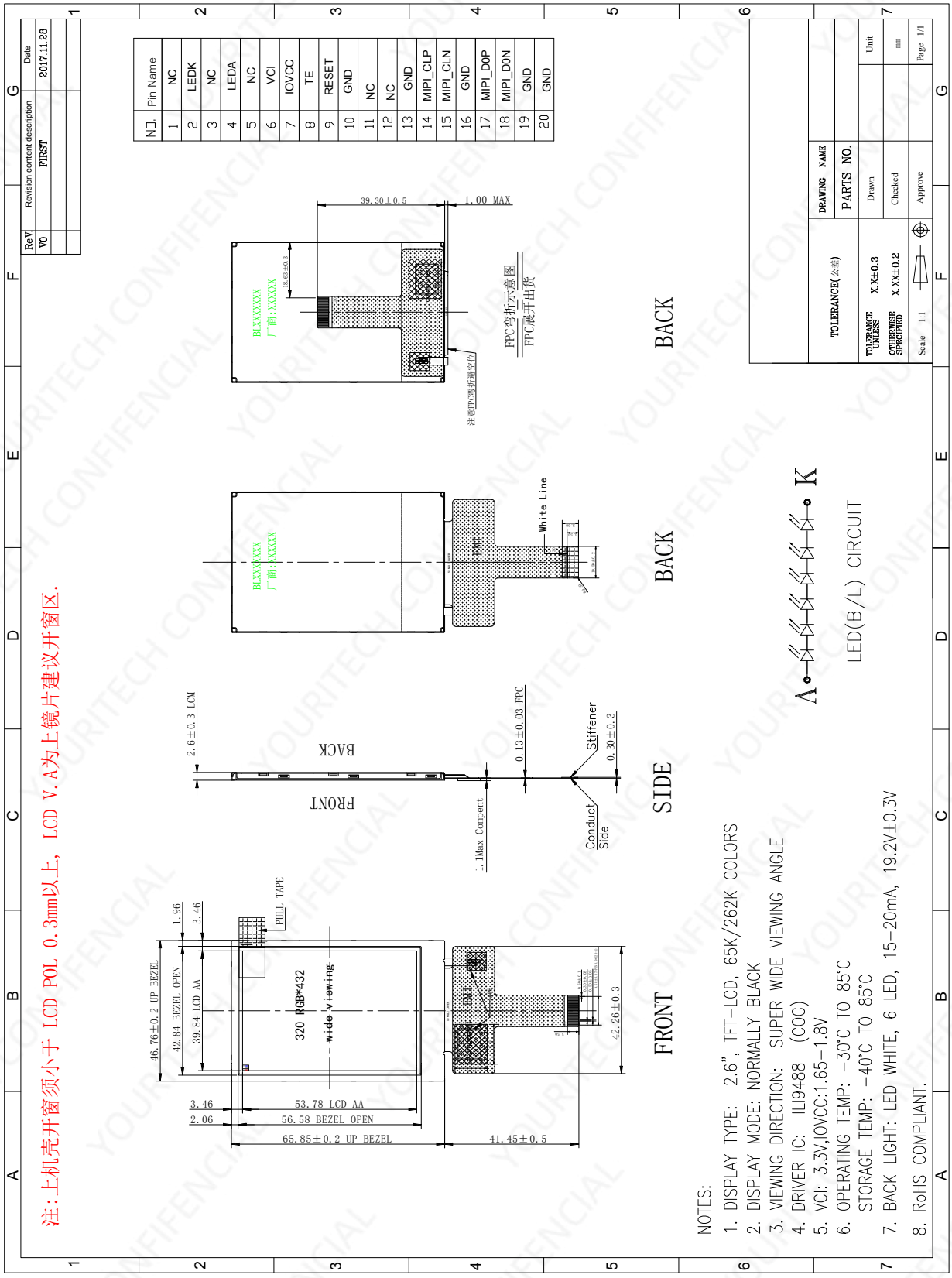
1.2 Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		46.76		mm	-
	Vertical(V)		65.85		mm	-
	Depth(D)		2.6		mm	-
Weight			14		g	-

2. Block Diagram



3. Outline dimension



4. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	NC	NC	
2	LEDK	Cathode pin of backlight.	P
3	NC	NC	
4	LEDA	Anode pin of backlight.	P
5	NC	NC	
6	VCI	Supply Voltage (3.3V).	P
7	IOVCC	I/O power supply voltage.(1.8V)	P
8	TE	-Tearing effect output Leave the pin to open when not in use.	O
9	RESET	- The external reset input. Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.	I
10	GND	Ground.	P
11	NC	NC	I/O
12	NC	NC	I/O
13	GND	Ground.	P
14	MIPI_CLP	MIPI DSI differential clock pair (DSI-CLK+/-)..	I
15	MIPI_CLN		I
16	GND	Ground.	P
17	MIPI_D0P	MIPI DSI differential data pair (DSI-Dn+/-).	I/O
18	MIPI_D0N		I/O
19	GND	Ground.	P
20	GND	Ground.	P

5. LCD Optical Characteristics

5.1 Optical specification

5.1.1 Transmissive mode

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	note
Contrast Ratio		CR	Θ=0 Normal viewing angle	100	150	--		Note1
Response time	Rising	$T_{R+}T_F$		--	25	50	msec	Note1
	Falling							
Color gamut		S(%)		40	58	--	%	
Color Filter Chromacicity	White	W_X		0.261	0.311	0.361		
		W_Y		0.287	0.337	0.387		
	Red	R_X		0.456	0.506	0.556		
		R_Y		0.270	0.320	0.370		
	Green	G_X		0.289	0.339	0.389		
		G_Y		0.500	0.550	0.600		
	Blue	B_X		0.123	0.173	0.223		
		B_Y		0.072	0.122	0.172		
Viewing angle	Hor.	$Θ_{21}$	CR>10	60	80	--	deg	Note1
		$Θ_{22}$		60	80	--		
	Ver.	$Θ_{12}$		60	80	--		
		$Θ_{11}$		60	80	--		
Option View Direction		Free						

5.1.2 Reflective mode (Not driving the back light condition)

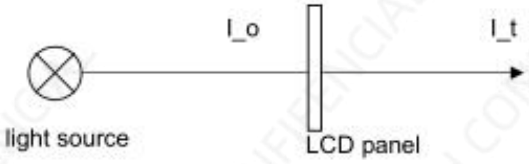
Item	Symbol	Specifications			unit	Note
Reflection Ratio （With Polarizer）	R （θ＝ϕ=0°）	1	2	-	%	Here the data are design value.
Reflective Contrast Ratio	Cr （θ=0°）	-	5	-		Note1
Viewing angle (Cr≥ 2)*	Θ21	-	45	-	deg	
	Θ22	-	45	-		
	Θ12	-	45	-		
	Θ11	-	45	-		

Note1：The polarizers are SRCG31APN2HC5(Top) and SRCH31APT2(Bottom)

5.3 Measuring Equipment

[1]Transmittance (T%)

The transmittance of the panel including polarizers is measured with electrical driving.



The Transmittance is defined as:

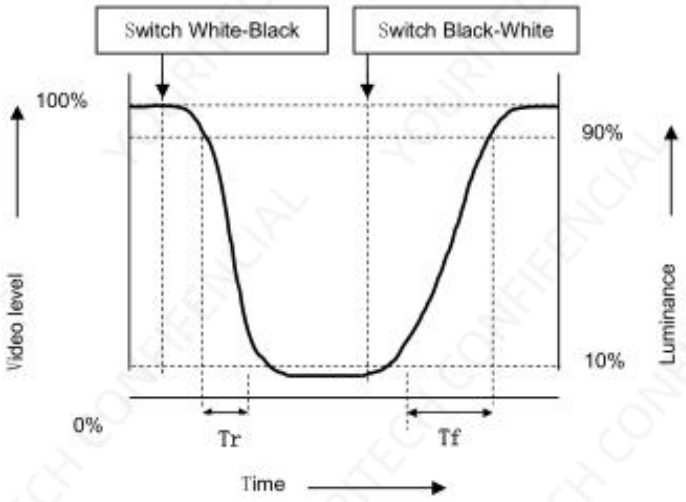
$$Tr = \frac{I\_t}{I\_o} \times 100\%$$

here,

I_o: the brightness of the light source.
I_t : the brightness after panel transmission.

[2] Response Time(Tr、Tf)

The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.

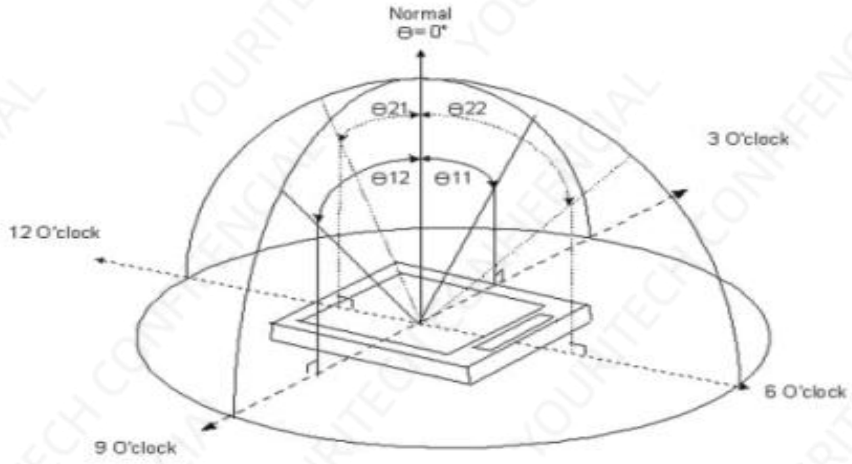


[3] Contrast ratio (Cr)

The contrast ratio (Cr), measured on a module, is the ratio between the luminance (L_w) in a full white area (R=G=B=1) and the luminance (L_d) in a dark area (R=G=B=0):

$$Cr = \frac{L\_w}{L\_d}$$

[4]Viewing angle diagram



[5] Definition of color gamut

Measuring machine:CFT-01. NTSC'S Primaries: R(x,y,Y)、G(x,y,Y)、B(x,y,Y).

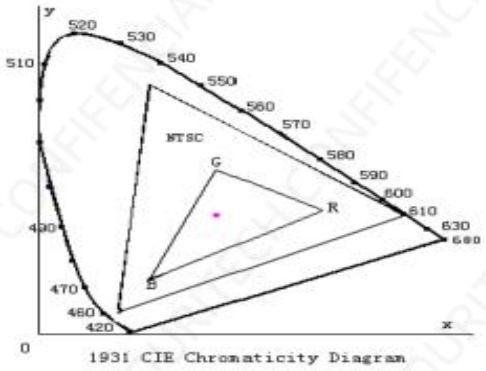


Fig. 1931 CIE chromaticity diagram

Color gamut: $S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$

6. Electrical Characteristics

6.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Logic Power Supply Voltage	IOVCC	-0.3	3.6	**V**
Analog Positive Power Supply	VSP	-0.3	+6.6	**V**
Operating temperature	T_{OP}	-30	+85	℃
Storage temperature	T_{ST}	-40	+85	℃

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

6.2 DSI DC Characteristics

DSI is using different state codes which are depending on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined on the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	Low (LP)
LP-10	High (LP)	High (LP)
LP-11	High (LP)	High (LP)

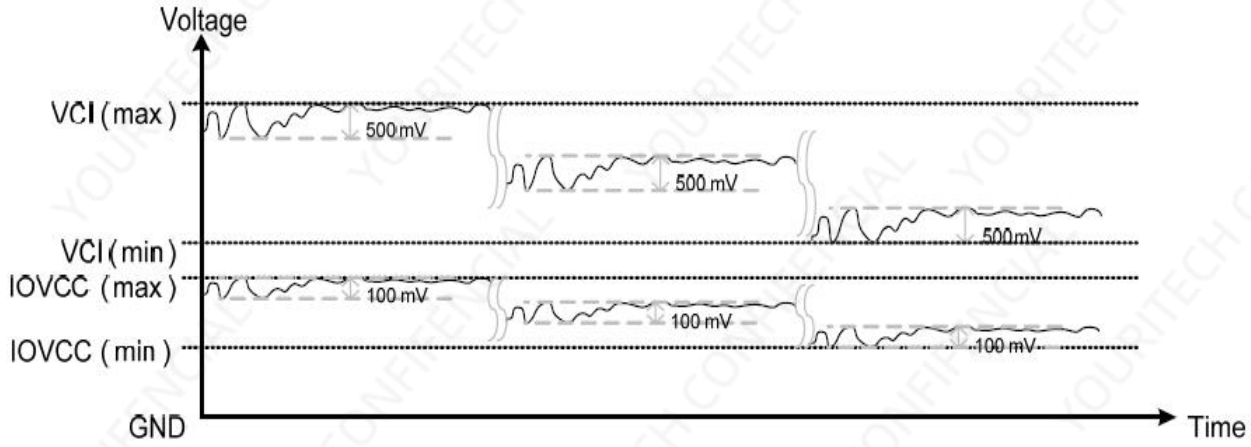
Note: Ta=-30℃ to 70℃ (to +85℃ no damage)

6.2.1 DC Characteristics for Power Lines

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Analog power supply voltage	VCI	Operating voltage	2.5	2.8/3.3	3.3	V	--
Digital interface supple Voltage	IOVCC	I/O supply voltage	1.65	1.8	3.3	V	--
Normal mode Current consumption	IDD	VCI+IOVCC	--	13	26	mA	
Analog power supply voltage noise	V_{VCI_NOISE}	Noise Range, 0 to 30kHz, Pulse Wave with Duty Cycle (50%/50%)	--	--	100	mV	--
	V_{IOVCC_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	--	--	500	mV	--
I/O power supply voltage noise	V_{IOVCC_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	--	--	100	mV	--

Note:

1. Ta=-30℃ to 70℃ (to +85℃ no damage)
2. These values are not symmetric amplitude, which centersm3g points are IOVCC or VCI. See examples as reference purposes, when V_{VCI_NOISE} and V_{IOVCC_NOISE} are maximums, below.



Noise on Power Supply Lines

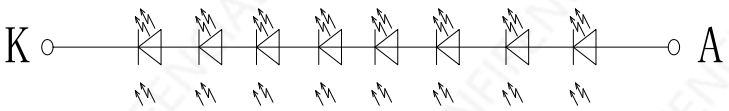
6.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 8chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	15	20	--	mA	
Forward Voltage	V_F	--	19.2	--	V	
LCM Luminance	L_V	450	500	--	cd/m2	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

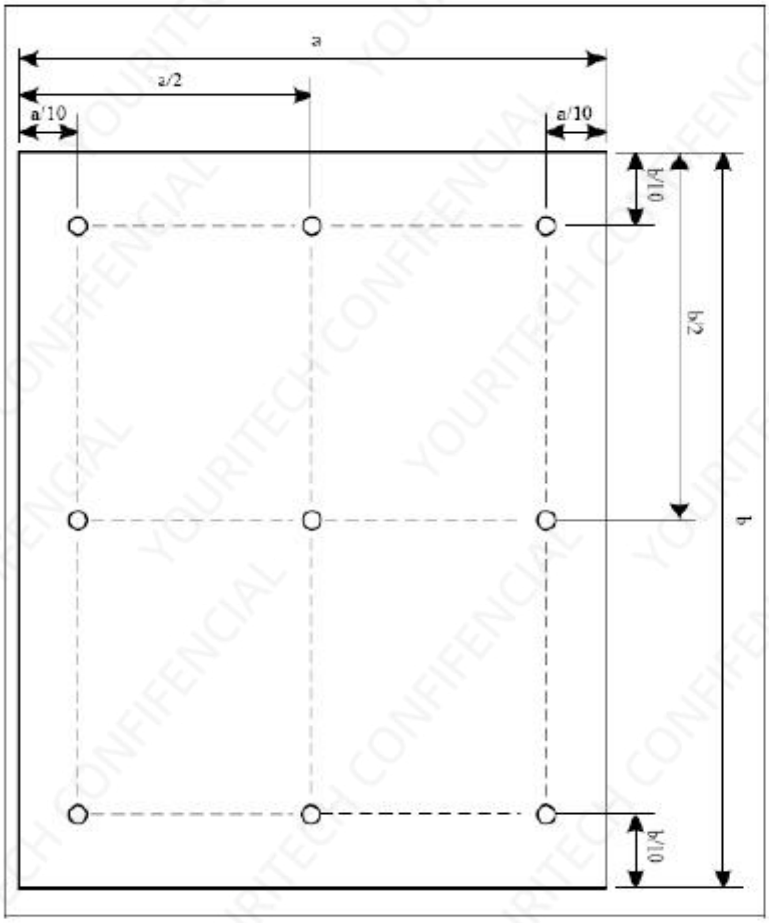
Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 160mA. The constant current driving method is suggested.



LED(B/L) CIRCUIT

NOTE 3：Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

7. Timing Characteristics of the DSI

7.1 High Speed Mode – Clock Channel Timing

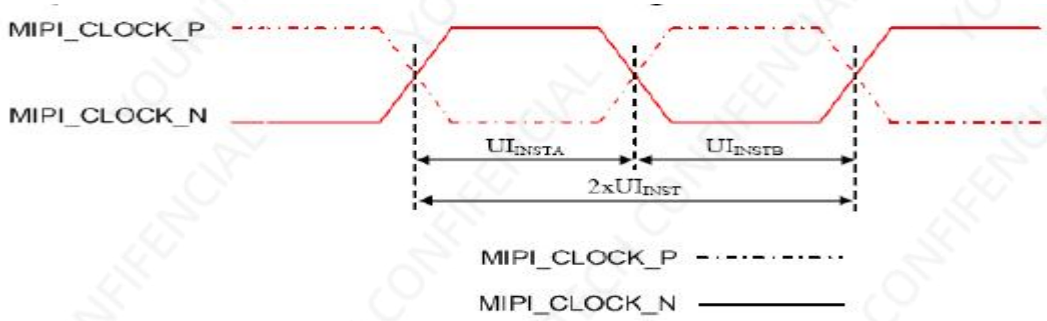


Figure *DSI Clock Channel Timing

Table * DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
MIPI_CLOCK_P/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
MIPI_CLOCK_P/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. See Table 45 for the minimum value of 24 UI per Pixel.

Table *Clock Channel Speed Limited

Data type	One Lanes speed	Unit
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	500M	bps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	500M	bps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	500M	bps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	500M	bps

7.2 High Speed Mode – Data Clock Channel Timing

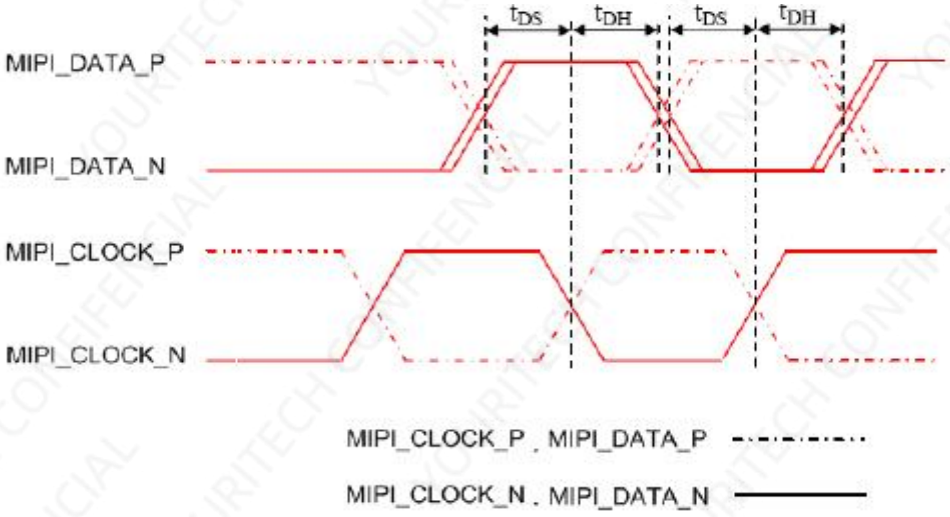


Figure* DSI Clock Channel Timing

Table *DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
MIPI_DATA_P/N	t_{DS}	Data to Clock Setup time	0.15xUI	-	ps
MIPI_DATA_P/N	t_{DH}	Clock to Data Hold Time	0.15xUI	-	ps

7.3 High Speed Mode – Rise and Fall Timings

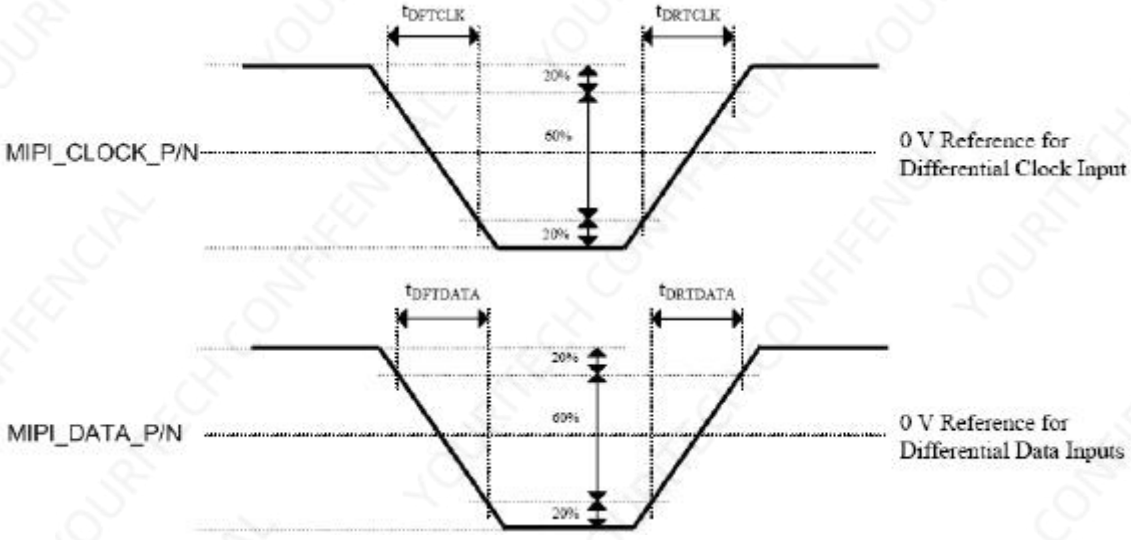


Figure *Rising and Falling Timings on Clock and Data Channels

Table *Rising and Falling Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification			
			Min	Typ	Max	Unit
Differential Rise Time for Clock	t_{DRTCLK}	MIPI_CLOCK_P/N	-	-	900	ps
Differential Rise Time for Data	$t_{DRTDATA}$	MIPI_DATA_P/N	-	-	900	ps
Differential Fall Time for Clock	t_{DFTCLK}	MIPI_CLOCK_P/N	-	-	900	ps
Differential Fall Time for Data	$t_{DFTDATA}$	MIPI_DATA_P/N	-	-	900	ps

Note: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPID-Phy standard.

7.4 Low Speed Mode – Bus Turn Around

Low Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the display module (ILI9488) sequence are illustrated below for reference purpose.

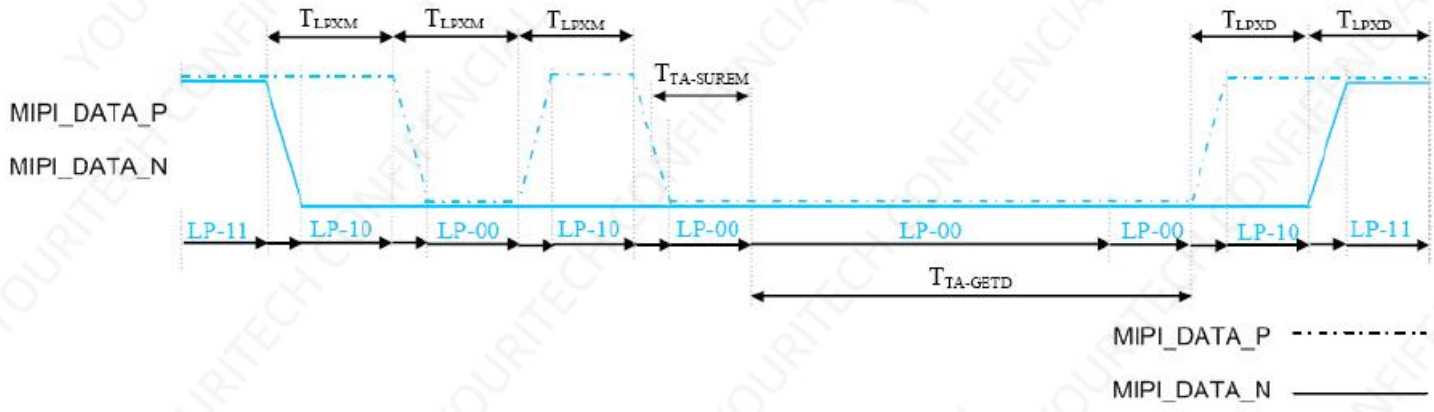


Figure *BTA from the MCU to the Display Module

Low Power Mode and its State Periods on the Bus Turnaround (BTA) from the display module (ILI9488) to the MCU sequence are illustrated below for reference purpose.

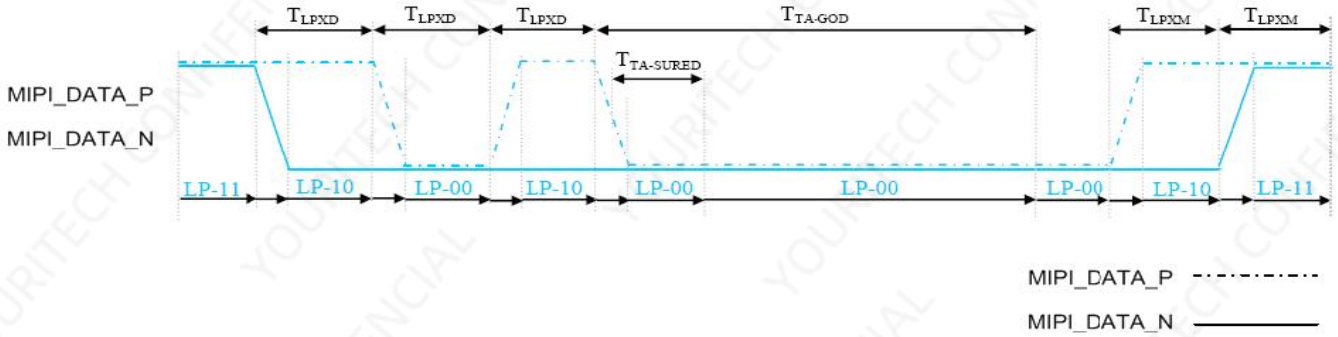


Figure* BTA from the Display Module to the MCU

Table *Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
Input (MIPI_DATA_P/N)	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9488)	50	75	ns
Output (MIPI_DATA_P/N)	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9488_ ➔ MCU)	50	75	ns
Input (MIPI_DATA_P/N)	$T_{TA-SUREM}$	Time-out before the ILI9488 starts driving	T_{LPXM}	$2xT_{LPXM}$	ns
Output (MIPI_DATA_P/N)	$T_{TA-SURED}$	Time-out before the MCU starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table *Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
Input (MIPI_DATA_P/N)	$T_{TA-GETD}$	Time to drive LP-00 by the ILI9488	$5xT_{LPXD}$	ns
Output (MIPI_DATA_P/N)	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MCU	$4xT_{LPXD}$	ns

7.5 Data Lanes from Low Power Mode to High Speed Mode

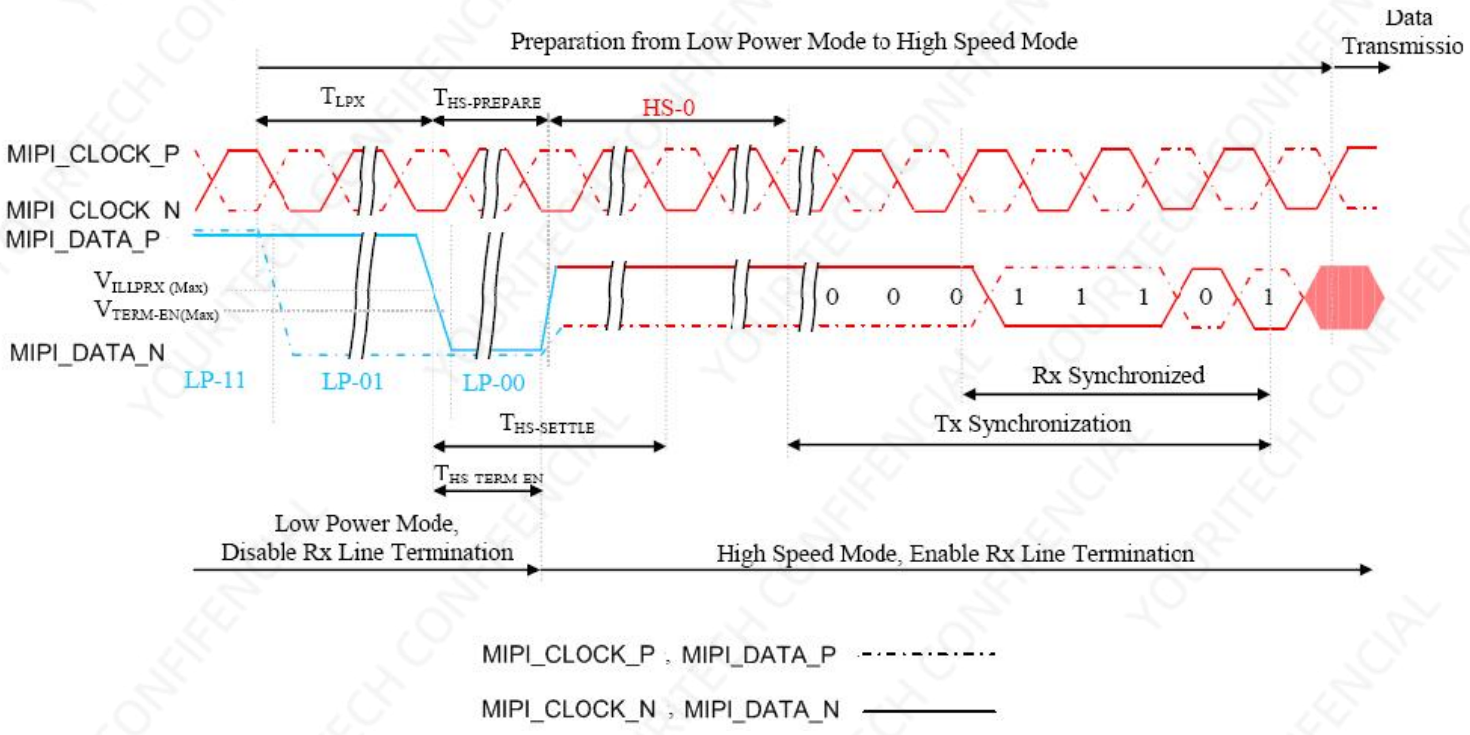
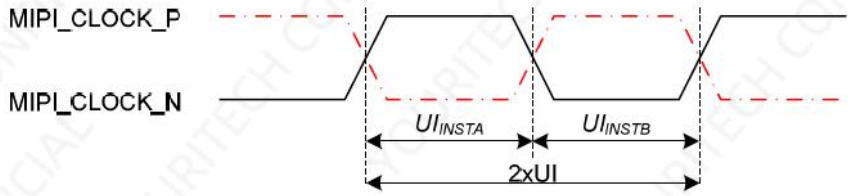


Figure* Data Lanes – Low Power Mode to High Speed Mode Timings

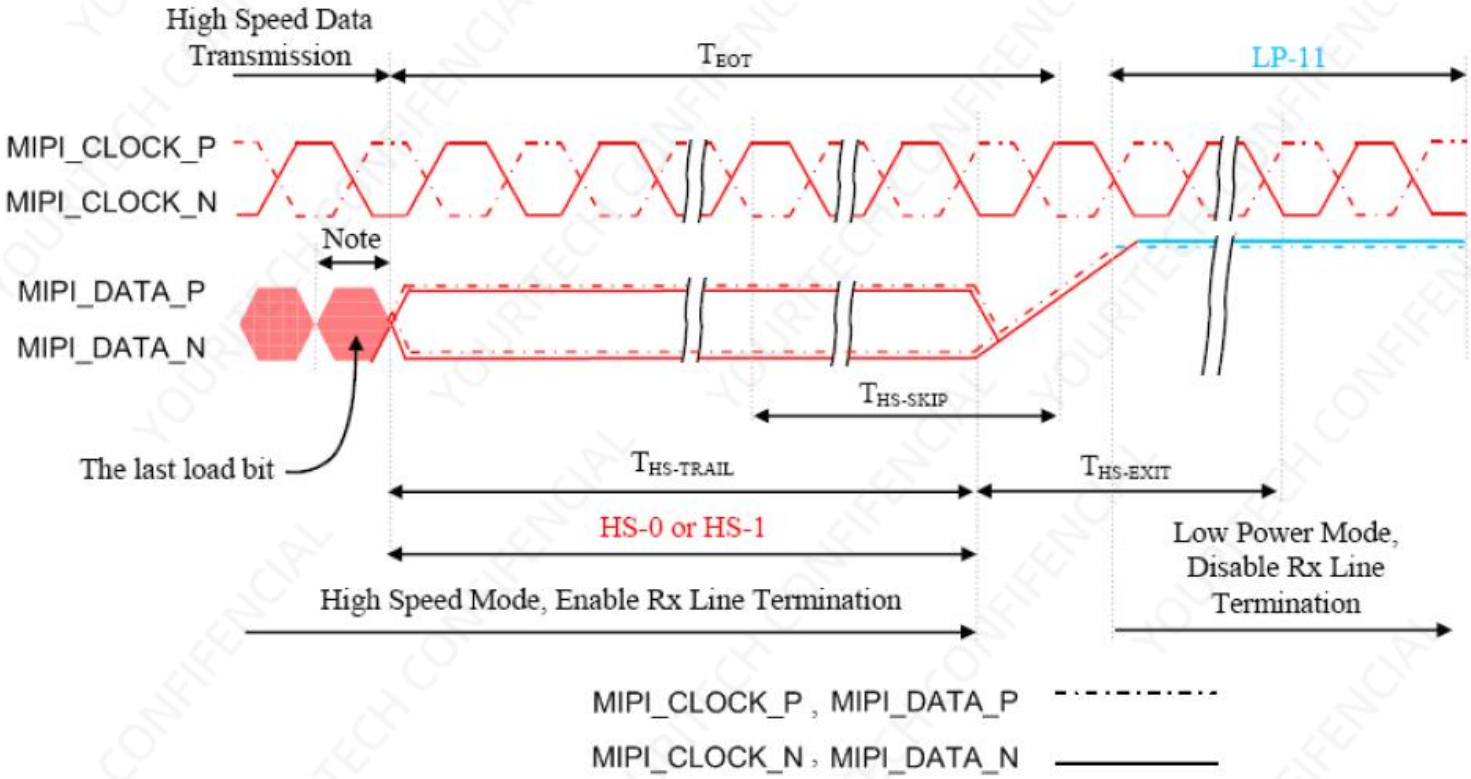
Table *Data Lanes – Low Power Mode High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
Input (MIPI_DATA_P/N)	T_{LPX}	Length of any Low Power State Period	50	-	ns
Input (MIPI_DATA_P/N)	$T_{HS-PREPARE}$	Time to Drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
Input (MIPI_DATA_P/N)	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when D_n crosses V_{ILMAX}	-	35+4xUI	ns

Note: $UI = UI_{INSTA} = UI_{INSTB}$



7.6 Data Lanes from Low Power Mode to High Speed Mode



Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Figure *Data Lanes – High Speed Mode to Low Power Mode Timings

Table* Data Lanes – High Speed Mode to Low Power Timings

Signal	Symbol	Description	Min	Max	Unit
Input (MIPI_DATA_P/N)	$T_{HS-SKIP}$	Time-out at the ILI9488 to Ignore Transition Period of EoT	40	50+4xUI	ns
Input (MIPI_DATA_P/N)	$T_{HS-EXIT}$	Time to Driver LP-11 after HS burst	100	-	ns

7.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

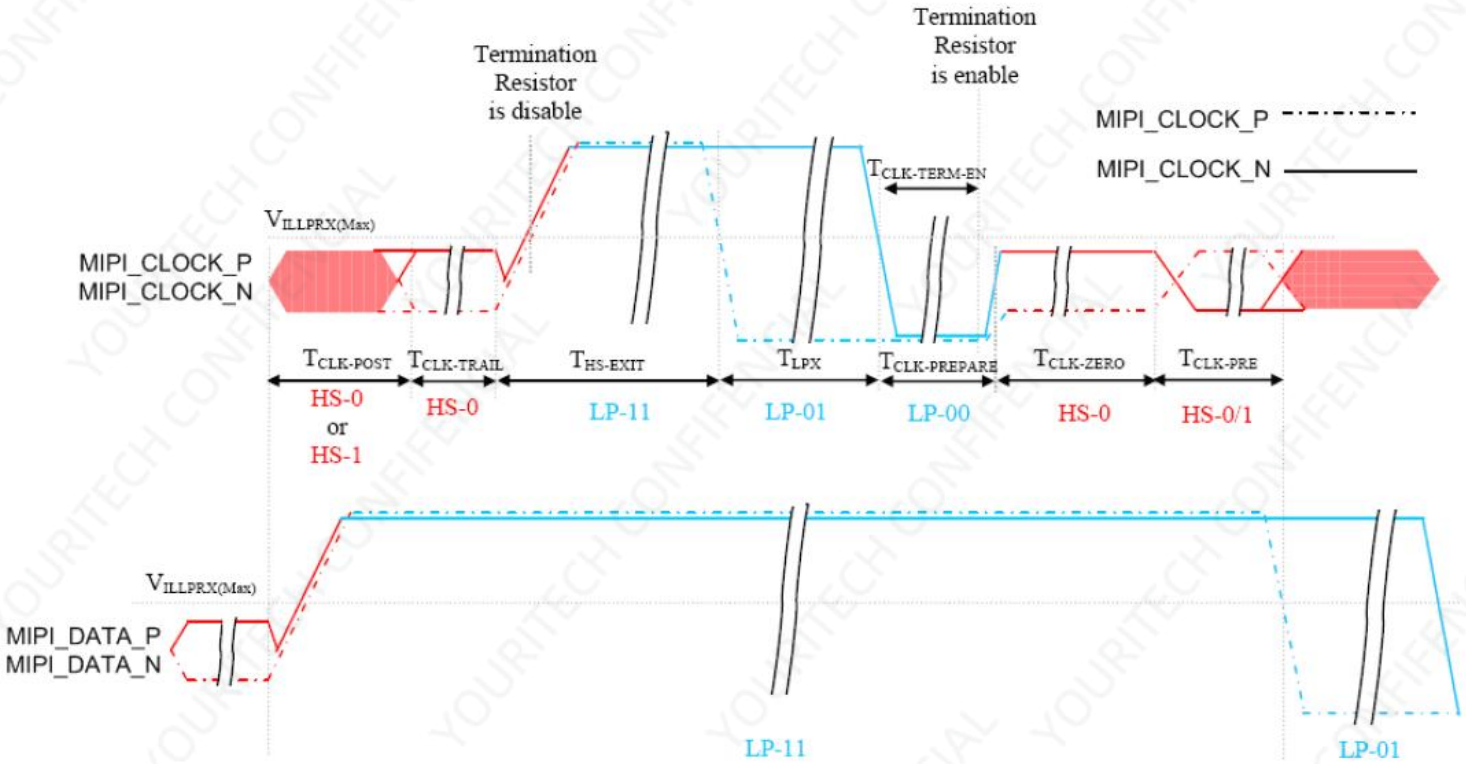
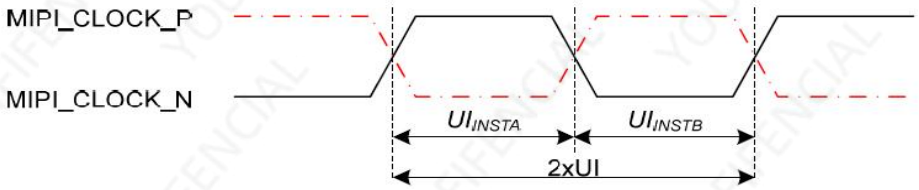


Figure* Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Table * Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
Input (MIPI_CLOCK_P/N)	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
Input (MIPI_CLOCK_P/N)	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
Input (MIPI_CLOCK_P/N)	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
Input (MIPI_CLOCK_P/N)	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
Input (MIPI_CLOCK_P/N)	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
Input (MIPI_CLOCK_P/N)	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
Input (MIPI_CLOCK_P/N)	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

Note: $UI = UI_{INSTA} = UI_{INSTB}$



7.8 Timing for DSI video mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	FCLK	--	(9)	--	MHz
Horizontal display area	HDISP	--	320	--	Clock
Horizontal Sync. Width	hpw	1	2	--	Clock
Horizontal Sync. Back Porch	hbp	1	8	-	Clock
Horizontal Sync. Front Porch	hfp	1	6	--	Clock
Vertical display area	VDISP	--	432	--	Line
Vertical Sync. Width	vs	1	2	--	Line
Vertical Sync. Back Porch	vbp	1	8	--	Line
Vertical Sync. Front Porch	vfp	1	4	--	Line
Frame-Rate		--	60	--	Hz

7.9 Reset input timing

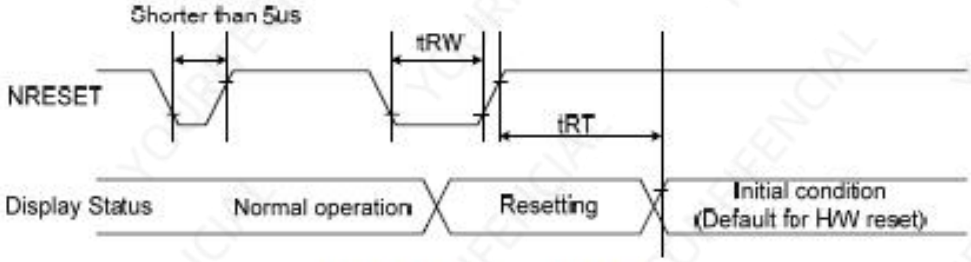


Figure 102 Reset Timing

Table 41 Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5(note 1,5)	ms
				120 (note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 43.

Table 42 Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

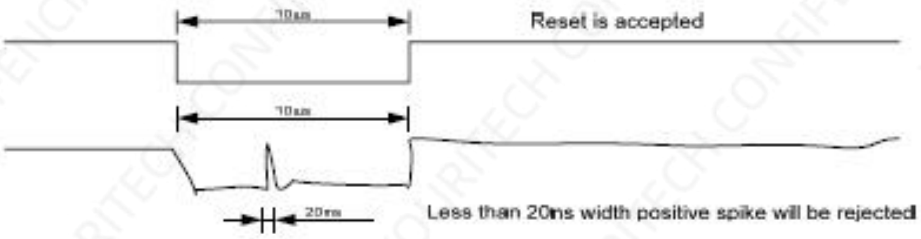


Figure 103 Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

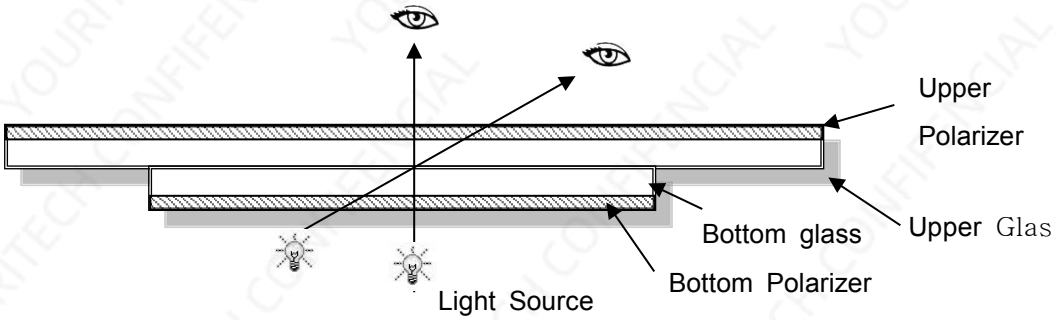
Temperature : 25±5℃

Humidity : 65%±10%RH

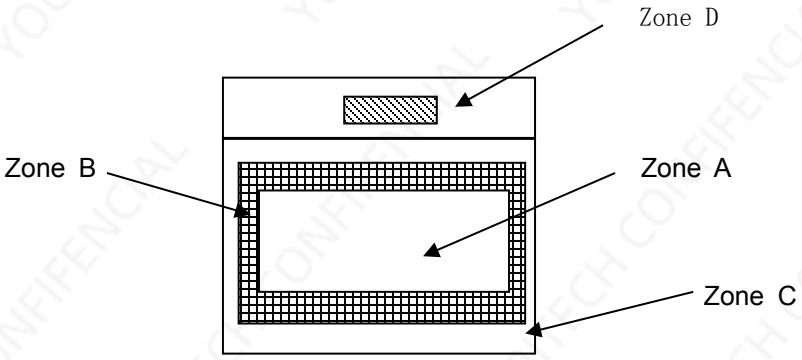
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



8.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer

Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ
AQL:

Major defect	Minor defect
0.65	1.5

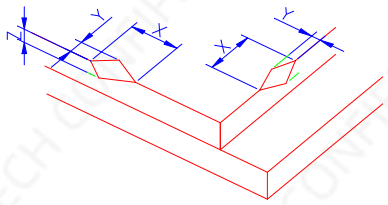
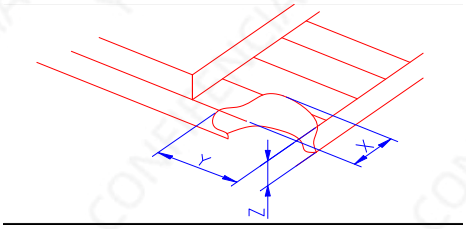
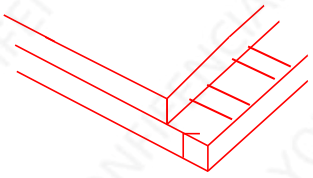
LCD: Liquid Crystal Display , LCM: Liquid Crystal Module,

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc…	Major
2	Missing	Missing components and etc…	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed,deformation and etc…	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot,Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

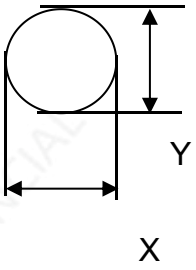
b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

8.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0

Spot defect



Φ=(X+Y)/2

① light dot（ black/white spot , pinhole, stain，etc.）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧6mm)		
0.25<Φ≤0.4	2(distance≧6mm)		
Φ>0.4	0		

② Dim spot（light leakage、dent、dark spot，etc）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧6mm)		
0.25<Φ≤0.4	2(distance≧6mm)		
Φ>0.4	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance≧6mm)		
Φ>0.5	0		

④Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	3(distance≧6mm)		
Φ>0.4	0		

3.0 LCD Pixel defect

Pixel bad points

Item	Zone A	Acceptable Qt
Bright dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Dark dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm
Total bright and dark dot		N≤4

Note:

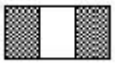
A) Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

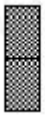
C) 2 dot adjacent = 1 pair = 2 dots

Picture:

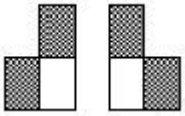
2 dot adjacent



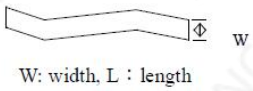
2 dot adjacent



2 dot adjacent (vertical)



2 dot adjacent (slant)

<table>
<tr><td>4.0</td><td>Line defect (LCD /Polarizer backlight black/white line, scratch, stain)
 

N：Count</td><td>
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Length(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.03</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.04</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.04<W≤0.05</td><td>L≤2.0</td><td colspan="2">N≤1</td></tr>
<tr><td>W>0.05</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td></tr>
<tr><td>5.0</td><td>Electronic Components SMT.</td><td>Not allow missing parts，solderless connection，cold solder joint，mismatch，The positive and negative polarity opposite</td></tr>
<tr><td>6.0</td><td>Display color& Brightness.</td><td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td></tr>
<tr><td>7.0</td><td>LCD Mura/Waving/ Hot spot</td><td>Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.</td></tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

9. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	85℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-30℃, 96HR	
High Temperature Storage	85℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Storage	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-10℃,30 min ↔ 60℃,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

Remark:

1.The test samples should be applied to only one test item.

2.Sample size for each test item is 5~10pcs.

3.For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.

4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

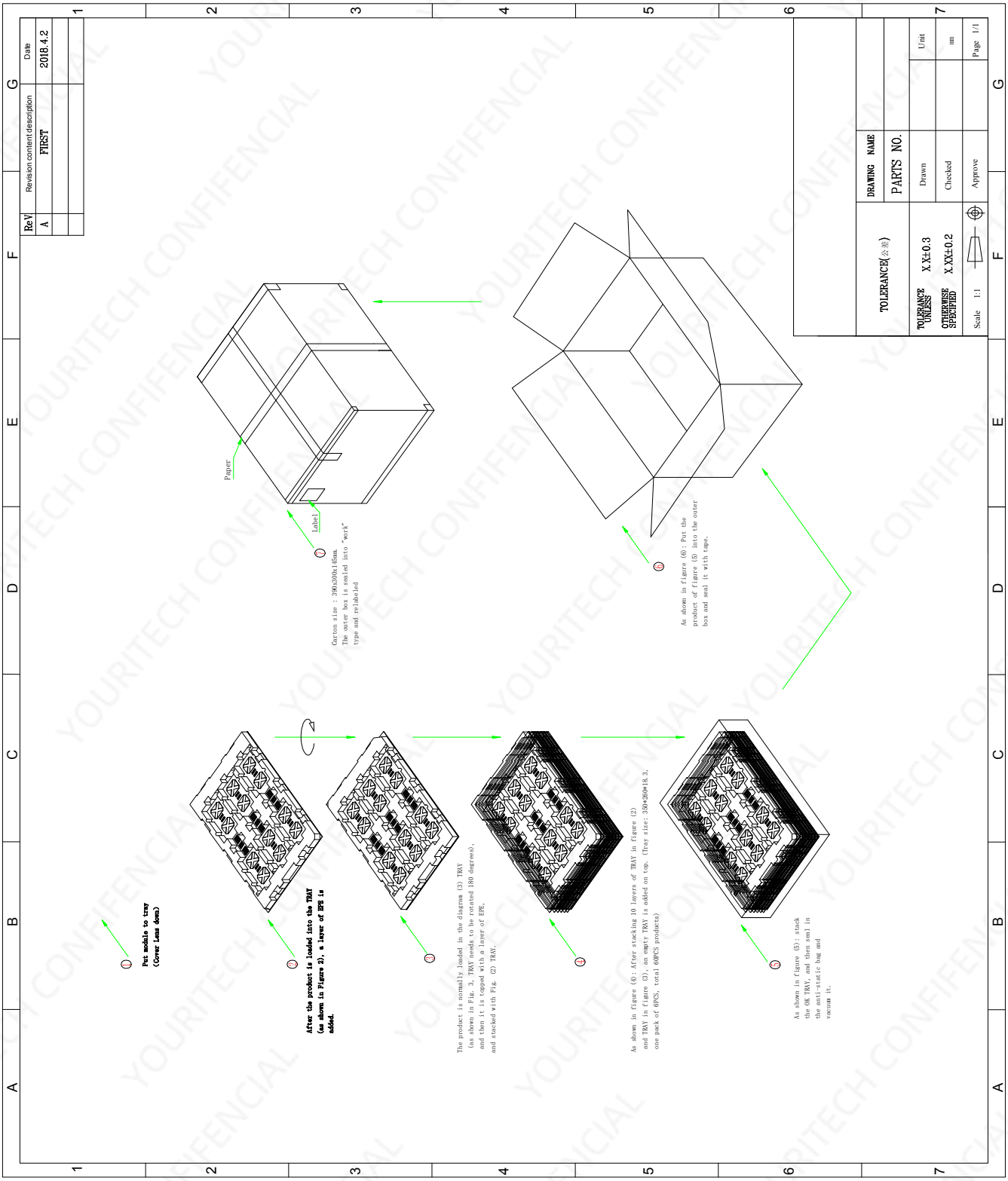
(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

11. Packing


Rev
Revision content description
Date
A
FIRST
2018.4.2
TOLERANCE(公差)
TOLERANCE UNLESS OTHERWISE SPECIFIED
X.X±0.3
X.XX±0.2
DRAWING NAME
PARTS NO.
Drawn
Checked
Approve
Scale 1:1
Unit
mm
Page 1/1
Paper
Label
Carton size : 390x300x145mm.
The outer box is sealed into "work" type and relabeled
As shown in figure (6): Put the product of figure (5) into the outer box and seal it with tape.
Put models to tray
(Cover Lens down)
After the product is loaded into the TRAY
(as shown in Figure 2), a layer of EPE is added.
The product is normally loaded in the diagram (3) TRAY
(as shown in Fig. 3, TRAY needs to be rotated 180 degrees),
and then it is topped with a layer of EPE,
and stacked with Fig. (2) TRAY.
As shown in figure (4): After stacking 10 layers of TRAY in figure (2)
and TRAY in figure (3), an empty TRAY is added on top. (Tray size: 330*260*18.3;
one pack of 6PCS, total 60PCS products)
As shown in figure (5): stack
the OK TRAY, and then seal in
the anti-static bag and
vacuum it.