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MODEL NO : ET026QV01-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-11-02

□**Preliminary Specification**

■**Final Product Specification**

Customer :_____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots240xRGBx320.
As to basic specification of the driver IC, refer to the IC (Sitronix:ST7789V) specification and data book.
All material & processing of the LCD module should be Lead Free.

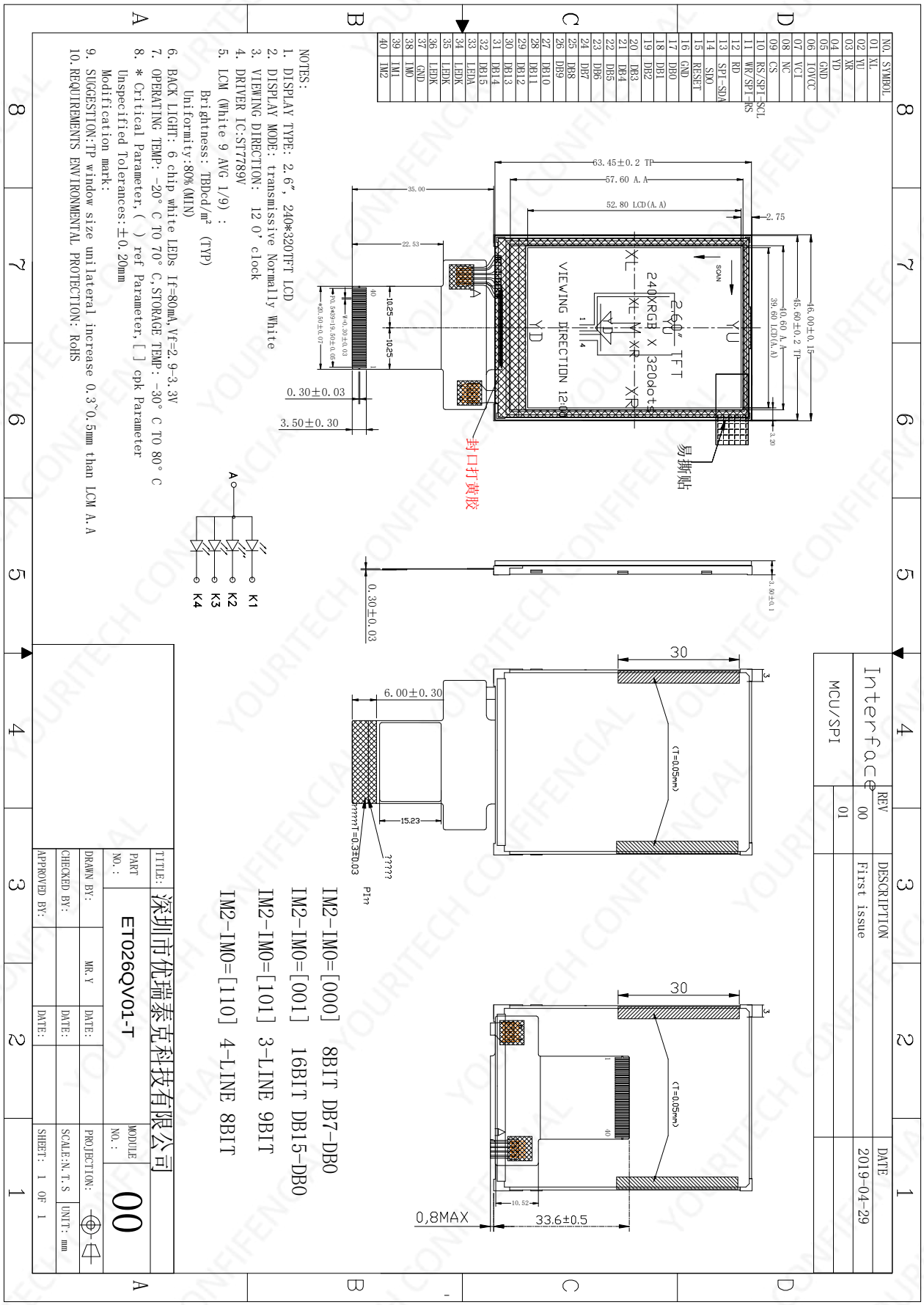
1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;
12 O'CLOCK
240dot-segment and 320 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
16lane RGB interface

1.3 Applications:

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally black	--
Drive element	TFT active matrix	--
Number of pixels	240*3RGB(H)X320(V)	Dots
Pixel arrangement	RGB Vertical stripe	--
Pixel Pitch (W*H)	0.165(H) X 0.165(V)	mm
Active area	39.60(H) x 52.80(V)	mm
Viewing direction	12 O'CLOCK	-
TFT Driver IC	ST7789	
TFT interface	16lane RGB interface	-
LCM Size (W*H*T)	46.00(H) x 64.00(V) x3.50(T)	mm
Approx. Weight	TBD	g
Touch structure		
Touch Driver IC		
Touch Interface		


NO. SYMBOL
01 XL
02 YU
03 XR
04 YD
05 GND
06 IOVCC
07 VCI
08 NC
09 CS
10 RS/SPI_SCL
11 WR/SPI_RS
12 RD
13 SPI-SDA
14 SDO
15 RESET
16 GND
17 DB0
18 DB1
19 DB2
20 DB3
21 DB4
22 DB5
23 DB6
24 DB7
25 DB8
26 DB9
27 DB10
28 DB11
29 DB12
30 DB13
31 DB14
32 DB15
33 LEDA
34 LEDK
35 LEDK
36 LEDK
37 GND
38 IM0
39 IM1
40 IM2
63.45±0.2 TP
57.60 A.A
52.80 LCD(A.A)
35.00
22.53
2.75
46.00±0.15
45.60±0.2 TP
40.60 A.A
39.60 LCD(A.A)
3.20
2.60" TFT
240XRGB x 320dots
VIEWING DIRECTION 12:00
SCAN
XL
YU
XR
YD
0.30±0.03
3.50±0.30
封口打黄胶
易撕贴
3.30±0.1
30
6.00±0.30
15.23
(T=0.05mm)
????T=0.3±0.03
P1??
10.52
0.8MAX
33.6±0.5
K1
K2
K3
K4
NOTES:
1. DISPLAY TYPE: 2.6", 240*320TFT LCD
2. DISPLAY MODE: transmissive Normally White
3. VIEWING DIRECTION: 12 O' clock
4. DRIVER IC:ST7789V
5. LCM (White 9 AVG 1/9) :
Brightness: TBDcd/m² (TYP)
Uniformity:80%(MIN)
6. BACK LIGHT: 6 chip white LEDs IF=80mA,Vf=2.9-3.3V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
Unspecified Tolerances:±0.20mm
Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10.REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS
IM2-IM0=[000] 8BIT DB7-DB0
IM2-IM0=[001] 16BIT DB15-DB0
IM2-IM0=[101] 3-LINE 9BIT
IM2-IM0=[110] 4-LINE 8BIT
Interface
MCU/SPI
REV 00 01
DESCRIPTION First issue
DATE 2019-04-29
TITLE: 深圳市优瑞泰克科技有限公司
PART NO.: ET026QV01-T
MODULE NO.: 00
DRAWN BY: MR.Y
CHECKED BY:
APPROVED BY:
DATE:
PROJECTION:
SCALE:N.T.S
UNIT: mm
SHEET: 1 OF 1

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
Humidity	RH	-	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.5	2.8	3.3	V
Supply Voltage for(DC/DC)	AVDD				V
Supply Voltage for(DC/DC)	AVEE				V

4.2 Back-Light Unit Characeristics

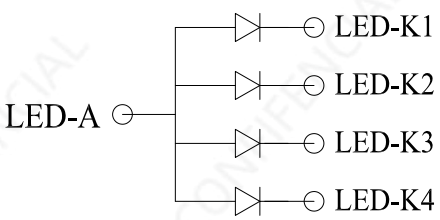
The back-light system is an edge-lighting type with 4 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	2.9	--	3.3	V	-
Forward current	I_F	--	80	-	mA	-
Luminance(With LCD+CTP)	Lv		200	--	cd/m^2	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	Functional	Notes
1	XL	Touch panel coordinate in the Left	
2	YU	Touch panel coordinate in the Up	
3	XR	Touch panel coordinate in the Right	
4	YD	Touch panel coordinate in the Down	
5	GND	gound	
6	IOVCC	POWER SUPPLY（1.8V/2.8V）	
7	VCI	PINPOWER SUPPLY（2.8V）	
8	NC	NC	
9	CS	CHIP SELECT	
10	RS/SPI-SCL	COMMAND AND DATA REGISTER SELECT PIN	
11	WR/SPI-RS	WRITE SIGNAL	
12	RD	READ SIGNAL	
13	SDA	Serial data input/output pin.	
14	SDO	Serial data output pin.	
15	RESET	RESET PIN	
16	GND	gound	
17-32	DB0~DB15	Data bus.	
33	LEDA	POWER SUPPLY+ FOR BACKLIGHT ANODE	
34-36	LEDK	POWER SUPPLY- FOR BACKLIGHT cathode	
37	GND	gound	
38-40	IM0-IM2	IM2-IM0=[000] 8BIT DB7-DB0 IM2-IM0=[001] 16BIT DB15-DB0 IM2-IM0=[101] 3-LINE 9BIT IM2-IM0=[110] 4-LINE 8BIT	

6. Timing Characteristics

Power ON/OFF Sequence

VDDI and VDD can be applied in any order.

In CABC function application, VDDI power on need delay 5ms after VDD has been supplied.

VDD and VDDI can be power down in any order.

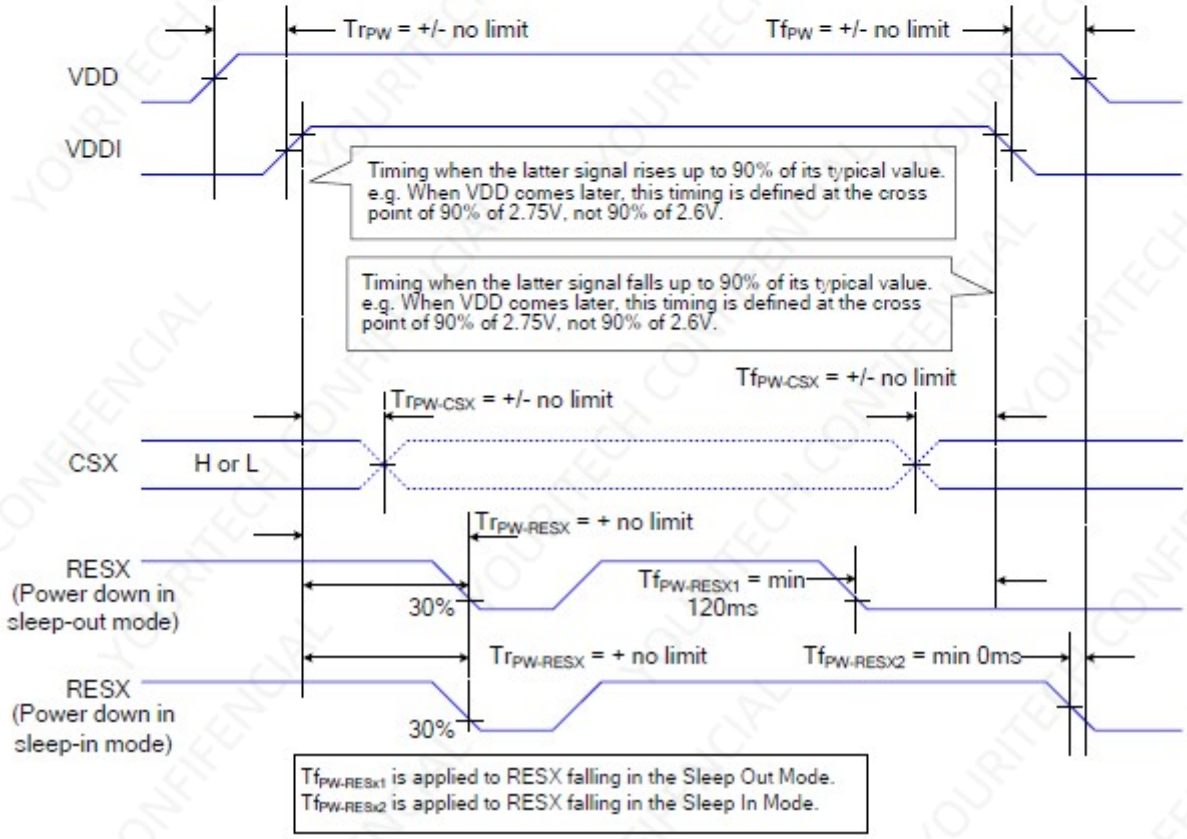
During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



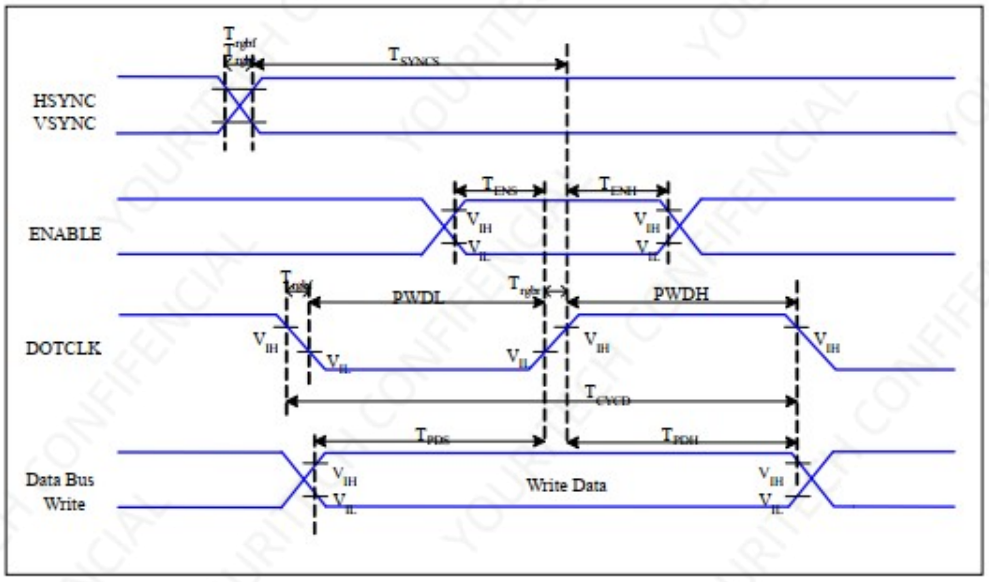


Figure 6 RGB Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

Table 7 18/16 Bits RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	35	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	35	-	ns	
	T_{ENH}	Enable Hold Time	35	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	35	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	35	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	80	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	10	ns	
DB	T_{PDS}	PD Data Setup Time	35	-	ns	
	T_{PDH}	PD Data Hold Time	35	-	ns	

Serial Interface Characteristics (3-line serial):

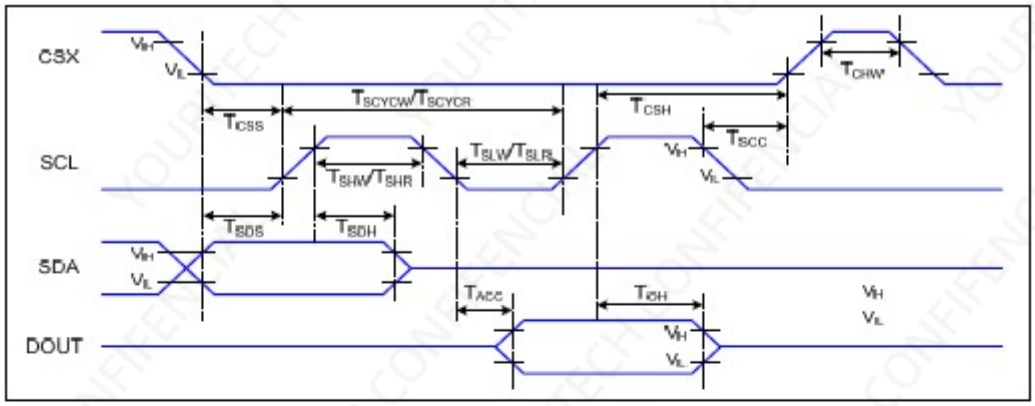


Figure 4 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

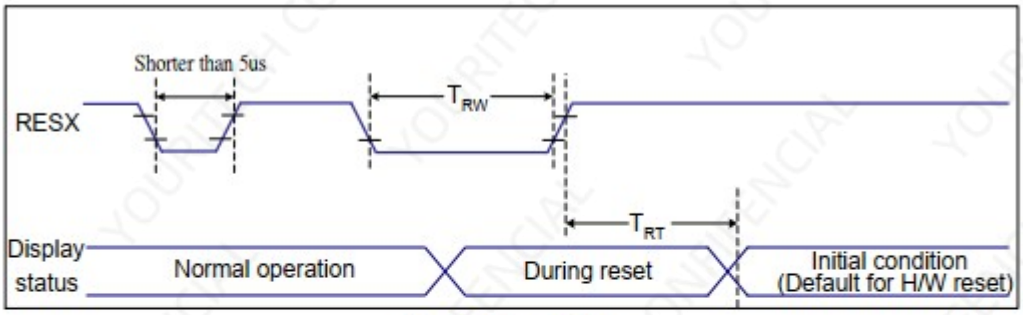


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 8 Reset Timing

Notes:

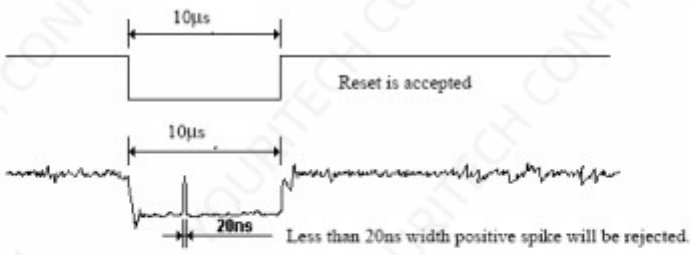
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (without Polarizer)		T(%)	—	—	13.8	—	—	
Contrast Ratio		CR	Θ=0 Normal viewing angle	400	500	—	—	(1)(2)
Response time	Rising	T_R	—	—	4	8	msec	(1)(3)
	Falling	T_F	—	—	12	24		
Color gamut		S(%)			60		%	
Color chromaticity (CIE1931)	White	W_x		0.283	0.303	0.323		(1)(4) CF glass
		Wy		0.305	0.325	0.345		
	Red	Rx		0.606	0.626	0.646		
		Ry		0.314	0.334	0.354		
	Green	Gx		0.257	0.277	0.297		
		Gy		0.529	0.549	0.569		
	Blue	Bx		0.122	0.142	0.162		
		By		0.102	0.122	0.142		
Viewing angle	Hor.	Θ_L	CR>10	35	45	—		
		Θ_R		35	45	—		
	Ver.	Θ_U		35	45	—		
		Θ_D		10	20	—		
Optima View Direction		12 O'clock						(5)

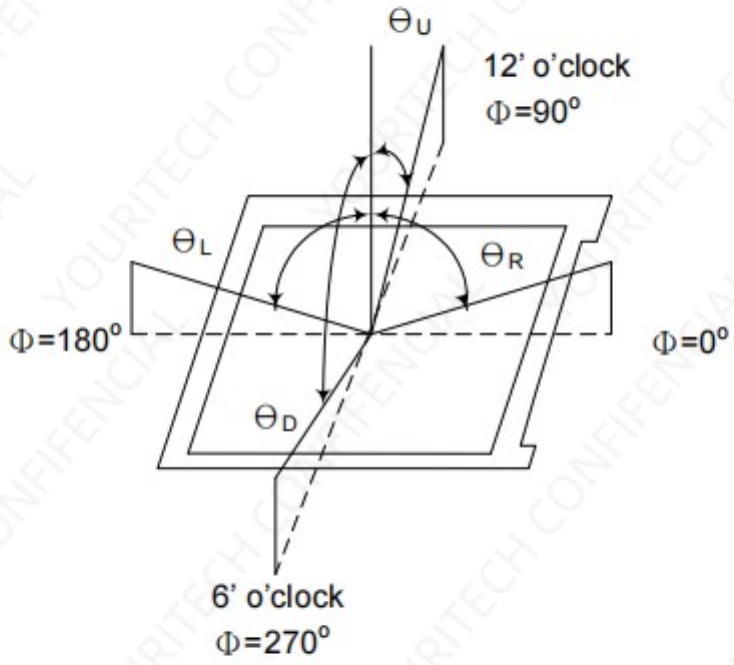
Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : 25±2°C
- 15min. warm-up time.

Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

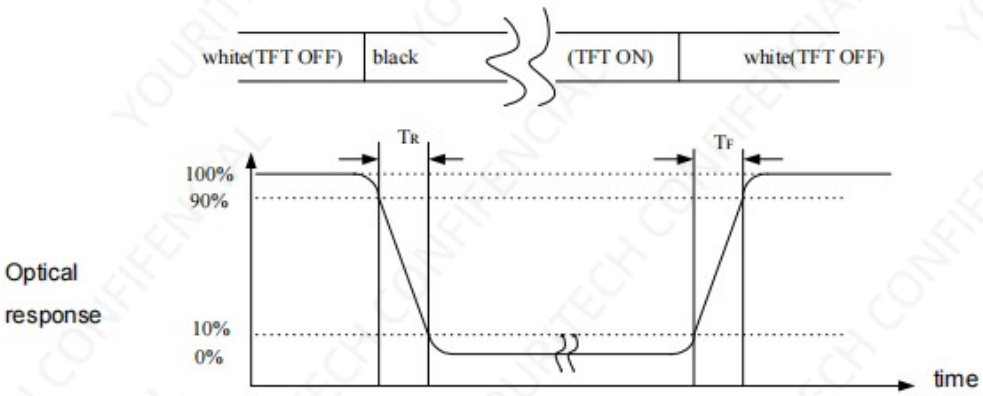
Note (1) Definition of Viewing Angle :



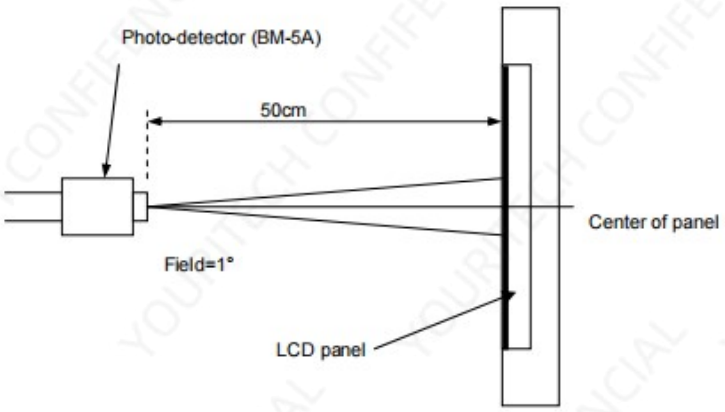
Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

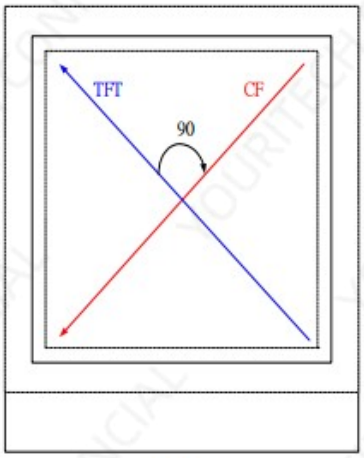
Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different view direction.



TFT Face up

8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~60℃（30min），50 cycles	

9. Packing Method----TBD

- END -