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Product Specifications

Customer	Standard
Description	ePaper Displa
Model Name	ET027EP02-J
Date	2025/06/26
Revision	1.0

	Design Engineering		
	Approval	Check	Design

Content

1. Over View

ET027EP02-J is a reflective electrophoretictechnology display module onan active matrix TFT substrate. The panelis capable of displaying black, white, yellow and redimages depending onthe associatedlookuptable used. The circuitry onthe panelincludes anintegrated gate and source driver,timing controller, oscillator, DC-DC boost circuit, and memoryto storethe frame buffer andlookuptables, and additional circuitryto control VCOM andBORDER settings.

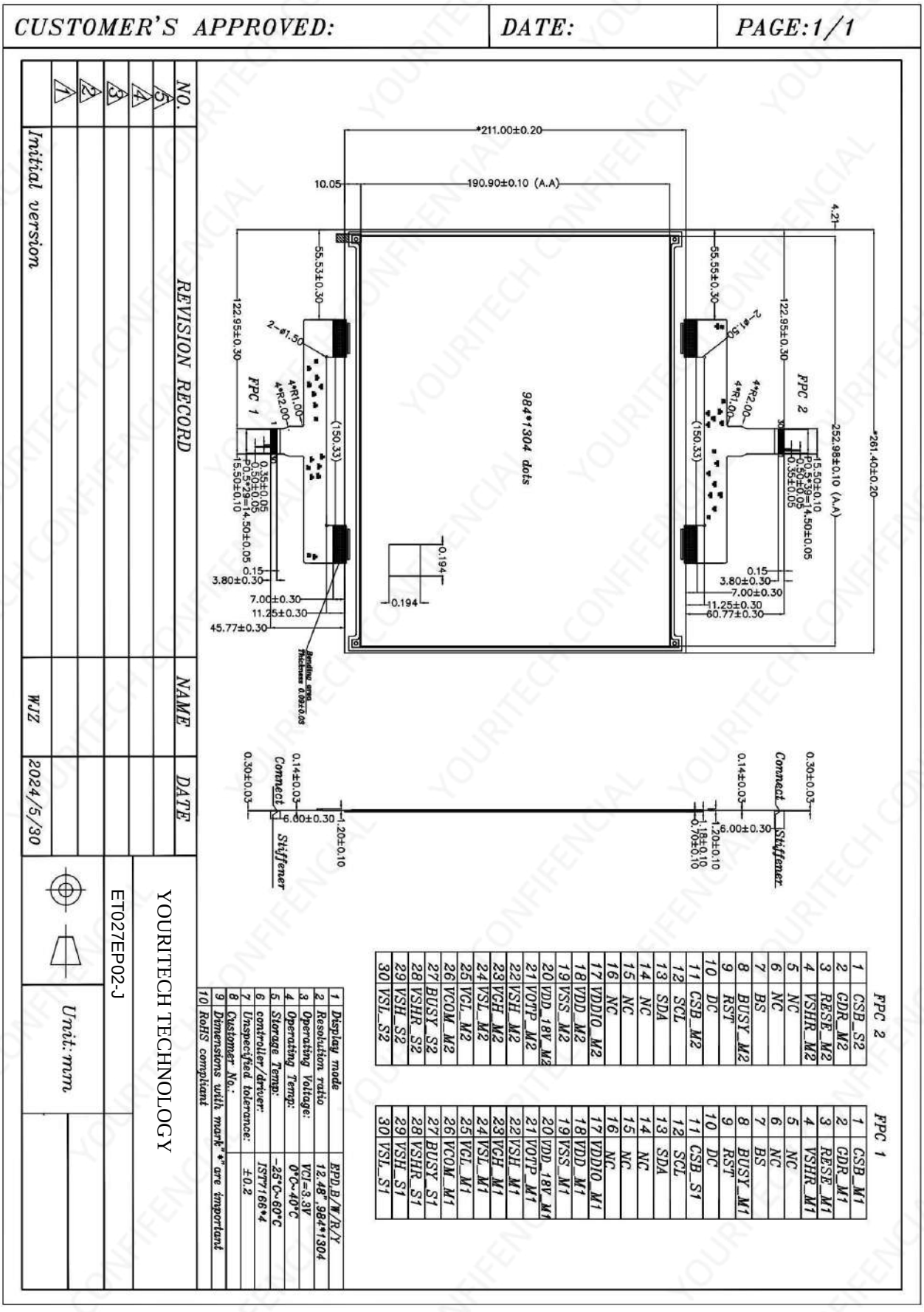
2. Features

- Highlight Red and Yellow color
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I^2C signal master interface to read external temperature sensor
- Available in COG package

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	12.48	Inch	
Display Resolution	1304(H)×984(V)	Pixel	Dpi:130
Active Area	252.98(H)×190.90(V)	mm	
Pixel Pitch	0.194×0.194	mm	
Pixel Configuration	Square		
Outline Dimension	261.4(H)×211(V) ×1.2(D)	mm	
Weight	128.64±0.5	g	

4. Mechanical Drawing of EPD module



FPC 2	
1	CSB_S2
2	GDR_M2
3	RESE_M2
4	VSHR_M2
5	NC
6	NC
7	BS
8	BUSY_M2
9	RST
10	DC
11	CSB_M2
12	SCL
13	SDA
14	NC
15	NC
16	NC
17	VDDIO_M2
18	VDD_M2
19	VSS_M2
20	VDD_18V_M2
21	VOTP_M2
22	VSH_M2
23	VCH_M2
24	VSL_M2
25	VCL_M2
26	VCOM_M2
27	BUSY_S2
28	VSHR_S2
29	VSH_S2
30	VSL_S2

FPC 1	
1	CSB_M1
2	GDR_M1
3	RESE_M1
4	VSHR_M1
5	NC
6	NC
7	BS
8	BUSY_M1
9	RST
10	DC
11	CSB_S1
12	SCL
13	SDA
14	NC
15	NC
16	NC
17	VDDIO_M1
18	VDD_M1
19	VSS_M1
20	VDD_18V_M1
21	VOTP_M1
22	VSH_M1
23	VCH_M1
24	VSL_M1
25	VCL_M1
26	VCOM_M1
27	BUSY_S1
28	VSHR_S1
29	VSH_S1
30	VSL_S1

5. Input /Output Pin Assignment

FPC-1 pin out list

No.	Single	Type	Description	Remark
1	CSB_M1	I	Serial communication chip select	
2	GDR_M1	O	This pin is N-MOS gate control	
3	RESE_M1	P	Current sense input for control loop	
4	VSHR_M1	P	Positive source voltage for Red	
5	NC		Not Connected.	
6	NC		Not Connected.	
7	BS	I	Input interface setting. Select 3 wire/4 wire SPI interface	
8	BUSY_M1	O	This pin indicates the driver status	
9	RST	I	Global reset pin. Low reset	
10	DC	I	Serial communication Command/Data input	
11	CSB_S1	I	Serial communication chip select	
12	SCL	I	Serial communication clock input	
13	SDA	I/O	Serial communication data input	
14	NC		Not Connected.	
15	NC		Not Connected.	
16	NC		Not Connected.	
17	VDDIO_M1	P	IO voltage supply	
18	VDD_M1	P	Digital/Analog power	
19	VSS_M1	P	Digital ground	
20	VDD_18V_M1	P	1.8V voltage input &output	
21	VOTP_M1	P	OTP program power	
22	VSH_M1	P	Positive source voltage	
23	VGH_M1	P	Positive gate voltage	
24	VSL_M1	P	Negative source voltage	
25	VGL_M1	P	Negative gate voltage	
26	VCOM_M1	O	VCOM output	
27	BUSY_S1	O	This pin indicates the driver status	
28	VSHR_S1	P	Positive source voltage for Red	
29	VSH_S1	P	Positive source voltage	
30	VSL_S1	P	Negative source voltage.	

FPC-2 pin out list

No.	Single	Type	Description	Remark
1	CSB_S2	I	Serial communication chip select	
2	GDR_M2	O	This pin is N-MOS gate control	
3	RESE_M2	P	Current sense input for control loop	
4	VSHR_M2	P	Positive source voltage	
5	NC		Not Connected.	
6	NC		Not Connected.	
7	BS	I	Input interface setting. Select 3 wire/4 wire SPI interface	
8	BUSY_M2	O	This pin indicates the driver status	
9	RST	I	Global reset pin. Low reset	
10	DC	I	Serial communication Command/Data input	
11	CSB_M2	I	Serial communication chip select	
12	SCL	I	Serial communication clock input	
13	SDA	I/O	Serial communication data input	
14	NC		Not Connected.	
15	NC		Not Connected.	
16	NC		Not Connected.	
17	VDDIO_M2	P	IO voltage supply	
18	VDD_M2	P	Digital/Analog power	
19	VSS_M2	P	Digital ground	
20	VDD_18V_M2	P	1.8V voltage input &output	
21	VOTP_M2	P	OTP program power	
22	VSH_M2	P	Positive source voltage	
23	VGH_M2	P	Positive gate voltage	
24	VSL_M2	P	Negative source voltage	
25	VGL_M2	P	Negative gate voltage	
26	VCOM_M2	O	VCOM output	
27	BUSY_S2	O	This pin indicates the driver status	
28	VSHR_S2	P	Positive source voltage for Red	
29	VSH_S2	P	Positive source voltage	
30	VSL_S2	P	Negative source voltage.	

Note: I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output,I/O: Input / Output. PS: Power Setting, C: Capacitor pin.

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VDD,VDDIO	-0.3 to +5.0	V
Logic Input voltage	VI	-0.3 to VDDIO+0.3	V
Operating Temp range	TOPR	0 to +40	º C
Storage Temp range	TSTG	-25 to +60	º C
Optimal Storage Temp	TSTGo	23±2	º C
Optimal Storage Humidity	HSTGo	55±10	%RH

Note:

VDDIO/VDD1/2/3/5/VDDLI/VDDLO and VGH/VGL/VDH/VDL/VDHR/VCOMDC/VCOMAC are based on VSS1/2/3/4/5 = 0V.

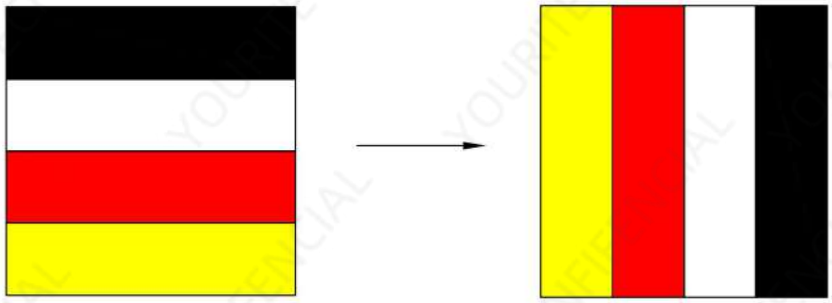
If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently.

It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

6.2 Panel DC Characteristics

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{IO}	-	VIO	2.3	3.3	3.6	V
Core logic voltage	V_{DD}		VDD	2.3	3.3	3.6	V
High level input voltage	V_{IH}	-	-	$0.8V_{IO}$	-	V_{IO}	V
Low level input voltage	V_{IL}	-	-	VSS1	-	$0.2V_{IO}$	V
High level output voltage	V_{OH}	IOH = 1mA	-	$0.8V_{IO}$	-	V_{IO}	V
Low level output voltage	V_{OL}	IOL = -1mA	-	VSS1	-	$0.2V_{IO}$	V
Typical power	P_{TYP}	V_{DD} =3.3V	-	-	201.3	-	mW
Deep sleep mode	P_{STPY}	V_{DD} =3.3V	-	-	0.003	-	mW
Typical operating current	Iopr_V_{DD}	V_{DD} =3.3V	-	-	61	-	mA
Image update time	-	25 ℃	-	-	26	-	sec
Deep Sleep Current	Ist_V_{DD}	Pattern no update, OSC off, VDD1/2/3/5=3.0V, Ta=25 ℃	-	-	8		uA

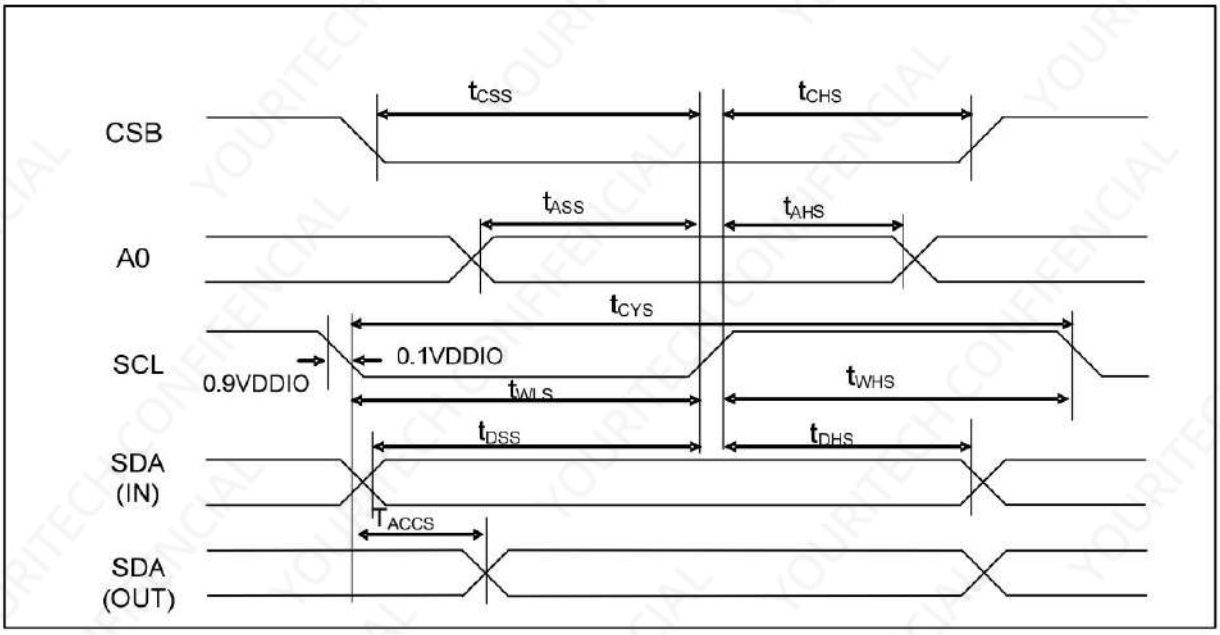
Notes: 1. The typical power is measured with following transition from horizontal 4 scale pattern to vertical 4 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by YOURITECH.
4. Electrical measurement：Multimeter

6.3 AC Characteristics

Serial Interface Characteristics



SPI Write(VDDIO=2.3 to 3.6V, Ta = -30 to +85°C)

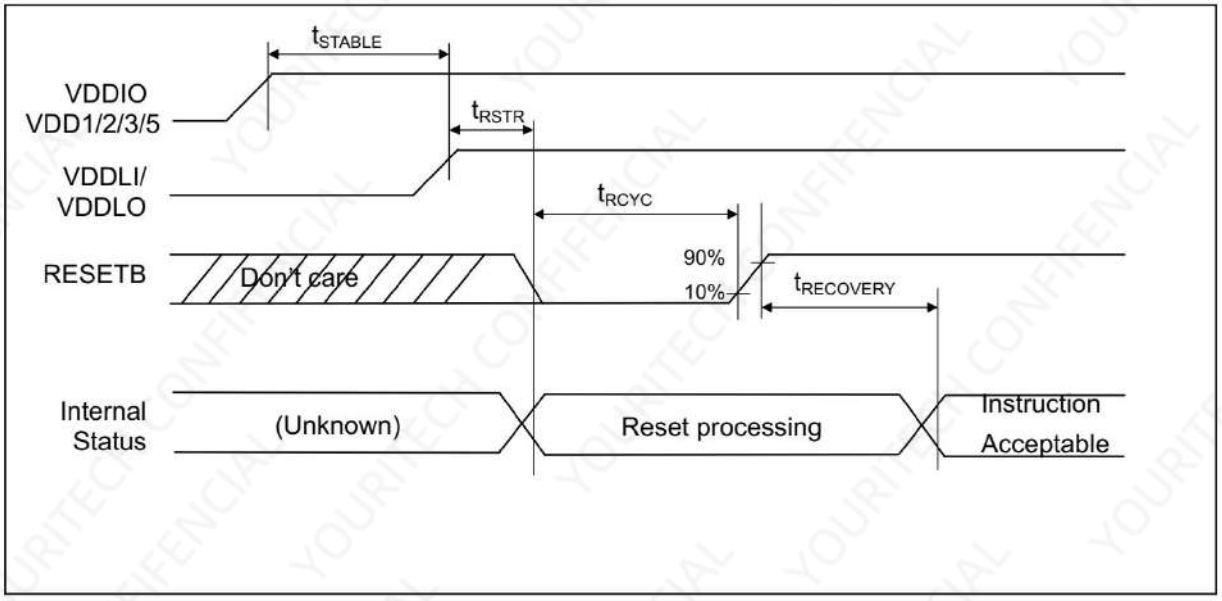
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCL high pulse width SCL low pulse width	SCL	tcys twhs twls	50 25 25	- - -	- - -	ns	
Address setup time Address hold time	A0	tass tahs	5 5	- -	- -	ns	
Data setup time Data hold time	SDA	tdss tdhs	30 30	- -	- -	ns	
CSB setup time CSB hold time	CSB	tcss tchs	60 65	- -	- -	ns	

SPI Read (VDDIO=2.3 to 3.6V, Ta = -30 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCL high pulse width SCL low pulse width	SCL	tcys twhs twls	600 150 400	- - -	- - -	ns	
Address setup time Address hold time	A0	tass tahs	90 90	- -	- -	ns	
Read access time	SDA	taccS	-	-	200	ns	
CSB setup time CSB hold time	CSB	tcss tchs	400 150	- -	- -	ns	

Note: All signal Rising time and falling Time <15ns

Reset Input Timing



(VDDIO=2.3 to 3.6V, VDD1/2/3/5 = 2.3 to 3.6V, Ta = -30 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
VDDIO/VDD1/2/3/5 stable time	VDDIO VDD1/2/3/5	tSTABLE	10	-	-	ms	With external Cap (*1)
Reset start time	RESETB	tRSTR	0	-	-	us	
Reset cycle time	RESETB	tRCYC	1	-	-	ms	
Reset recovery time	RESETB	tRECOVERY	1	-	-	ms	(*2)

NOTE

*1. tSTABLE depending on different capacitance of Capconnect to VDDLI/VDDLO(external stabilizing capacitor), and It should be re-adjusted for different capacitance of the Cap connect to VDDLI/VDDLO.

*2. After reset 1ms, it must check that the BSUY_N signal is high before the first instruction can be executed.

7. Command Table

R00H(PSR): Panel setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PSR	W	0	0	0	0	0	0	0	0	0	(00H)
1st Parameter	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	1	(CFH)
2nd Parameter	W	1	LUT_EN	0	FOPT	VCMZ	1	TIEG	NORG	VC_LUTZ	(09H)

1st Parameter:

Bit7-6	Resolution setting
00b	Display resolution is 600x448
01b	Display resolution is 640x480
10b	Display resolution is 720x540
11b	Display resolution is 800x600 (default)

Bit5	Power switch operation mode
0	Power switching time in the period of frame scanning.(default).
1	Power switching time in the external period before frame scanning.

Bit3	UD function(*1)
0	Scandown; First line=Gn,Gn-1, ... G2, Last line=G1
1	Scanup; First line=G1,G2, ... ,Gn-1, Last line=Gn.(default)

Bit2	SHL function(*2)
0	Shift left; First data=Sn,Sn-1, ... ,S2, Last data=S1.
1	Shift right; First data=S1,S2, ... ,Sn-1, Last data=Sn.(default)

Bit1	SHD_N function(*3)
0	Booster OFF, register data are kept,and Source/Border/VCOM are kept 0V or floating
1	Booster ON.(default)

2nd Parameter:

Bit0	VC_LUTZ function
0	NO effect.
1	After refreshing display,the output of VCOM is set to floating automatically(default)

Bit1	NORG function
0	NO effect.(default)
1	After refreshing display,VCOM is tied to GND before power off

Bit2	TIEG function
0	NO effect.(default)
1	After power off booster,VGL will be tied to GND.

Bit4	VCMZ function
0	NO effect.(default)
1	VCOM is always floating.

Bit5	FOPT function
0	Scan 1 frame after waveform finished (Default)
1	No Scan after waveform finished and switch the source channel output to HiZ

Bit7	LUT_EN
0	LUT from OTP(default)
1	LUT from register

Priority of VCOM setting: VCMZ > NORG > FOPT > VC_LUTZ

FOPT setting is part of refreshing display.

FOPT: Power off floating.

Notes:

1. Non-select gate line keep at VGL for DSP/DRF and AMV
2. Inactive source line follow LUT for DSP/DRF
3. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD off. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

R01H(PWR): Power Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWR	W	0	0	0	0	0	0	0	0	1	(01H)
1st Parameter	W	1	-	-	-	-	V_MODE	VSC_EN	VS_EN	VG_EN	(07H)
2nd Parameter	W	1	-	-	-	-	-	-	VG[1]	VG[0]	(00H)
3rd Parameter	W	1	-	VDHR [6]	VDHR [5]	VDHR [4]	VDHR [3]	VDHR [2]	VDHR [1]	VDHR [0]	(00H)
4th Parameter	W	1	-	VDH [6]	VDH [5]	VDH [4]	VDH [3]	VDH [2]	VDH [1]	VDH [0]	(00H)
5th Parameter	W	1		VDL[6]	VDL [5]	VDL [4]	VDL [3]	VDL [2]	VDL [1]	VDL [0]	(00H)
6th Parameter	W	1		VDHR1 [6]	VDHR1 [5]	VDHR1 [4]	VDHR1 [3]	VDHR1 [2]	VDHR1 [1]	VDHR1 [0]	(00H)

Power mode switch mapping:

Mode 0 : 0V & +15V & -15V & VDHR (+3V~+15V)

Mode 1 : 0V & VDH (+3V~+15V) & VDL (-3V~-15V) & VDHR1 (+3V~+15V)

1st Parameter:

Bit3	Initial source power mode.
0	Mode0. (default)
1	Mode1.

Bit2	Source LV power selection.
0	External source LV power from VDHR pins.
1	Internal DC/DC function for generate VDHR.

Bit1	Source power selection.
0	External source power from VDH/VDL pins.
1	Internal DC/DC function for generate VDH/VDL.

Bit0	Gate power selection.
0	External gate power from VGH/VGL pins.
1	Internal DCDC function for generate VGH/VGL.

2nd Parameter:

Bit1-0	VGH & VGL Voltage Level.
00	VGH=20v, VGL=-20v(default)
01	VGH=17v, VGL=-17v
10	VGH=15v, VGL=-15v
11	VGH=10v, VGL=-10v

3rd & 4th Parameter: Internal VDHR/VDH power selection (Default value: 0000000b)

5th & 6th Parameter: Internal VDL/VDHR1 power selection (Default value: 0000000b)

Bit6-0	Internal VDH selection.	Internal VDL selection.	Bit6-0	Internal VDH selection.	Internal VDL selection.
0000000	3V	-3V	0110010	8.0V	-8.0V
0000001	3.1V	-3.1V	...	...	...
0000010	3.2V	-3.2V	0111100	9.0V	-9.0V
0000011	3.3V	-3.3V	...	...	...
0000100	3.4V	-3.4V	1000110	10.0V	-10.0V
0000101	3.5V	-3.5V	...	...	...
0000110	3.6V	-3.6V	1010000	11.0V	-11.0V
0000111	3.7V	-3.7V	...	...	...
0001000	3.8V	-3.8V	1011010	12.0V	-12.0V
0001001	3.9V	-3.9V	...	...	...
0001010	4.0V	-4.0V	1100100	13.0V	-13.0V
0001011	4.1V	-4.1V	...	...	...
0001100	4.2V	-4.2V	1101110	14.0V	-14.0V
0001101	4.3V	-4.3V	...	...	...
0001110	4.4V	-4.4V	1111000	15.0V	-15.0V
0001111	4.5V	-4.5V			
0010000	4.6V	-4.6V			
...	...	...			
0010100	5.0V	-5.0V			
...	...	...			
0011110	6.0V	-6.0V			
...	...	...			
0101000	7.0V	-7.0V			
...	...	...			

Notes:

1. VGH-VDH/VGH-VDHR/VGH-VDHR1 ≧ 2v
2. VGL-VDL ≧ -2v

R02H(POF): Power OFF Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
POF	W	0	0	0	0	0	0	0	1	0	(02H)
1st Parameter	W	1	-	-	-	-	-	-	-	0	(00H)

After power off command, driver will power off base on power off sequence. After power off command, BUSY_N signal will become "0".

Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register will keep until VDD become off.

SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

R03H(POFS): Power on/off Sequence Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PFS	W	0	0	0	0	0	0	0	1	1	(03H)
1st Parameter	W	1	T_VDPG_OFF				T_VDS_OFF				(00H)

1st Parameter:

Bit3-0	Power off sequence of VDH and VDL
0000b	20ms(default)
0001b	40ms
0010b	60ms
0011b	80ms
1111b	320ms

Bit7-4	Power off sequence of VGH and VGL
0000b	20ms(default)
0001b	40ms
0010b	60ms
0011b	80ms
1111b	320ms

R04H(PON):Power ON Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PON	W	0	0	0	0	0	0	1	0	0	(04H)

After power on command, the driver will power ON base on Power ON sequence.

After power on command and all power sequence are ready (based on PWR command), then BUSY_N signal will become "1".

This command only active when BUSY_N="1".

R06H(BTST): Booster Soft Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
LUT0	W	0	0	0	0	0	0	1	1	0	(06H)
1st Parameter	W	1	BT_PHA1	BT_PHA0	0	0	0	0	0	0	(00H)
2st Parameter	W	1	BT_PHB1	BT_PHB0	0	0	0	0	0	0	(00H)
3st Parameter	W	1	BT_PHC1	BT_PHC0	0	0	0	0	0	0	(00H)

Control of Power On time.

D7-D6	BT_PHA/B/C perild
00	10ms (default)
01	20ms
10	30ms
11	40ms

R07H(DSLP): Deep Sleep Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DSLP	W	0	0	0	0	0	0	1	1	1	(07H)
1st Parameter	W	1	1	0	1	0	0	1	0	1	(A5H)

After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be excited if check code = 0xA5.

R10H(DTM): Data Start Transmission Register

`	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DTM	W	0	0	0	0	1	0	0	0	0	(10H)
2-bit mode											
1st Parameter	W	1	Pixel1		Pixel2		Pixel3		Pixel4		(00H)
⋮	W	1	⋮ ⋮		⋮ ⋮		⋮ ⋮		⋮ ⋮		(00H)
Nth Parameter	W	1	Pixel(n-3)		Pixel(n-2)		Pixel(n-1)		Pixel(n)		(00H)

NOTE:"-" Don't care, can be set to VDD or GND level. "X": Dummy data, it would not be stored in frame buffer.

This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (R12H). Then the chip will start to send data for panel.

Pixel[1~n][1:0](2-bit mode):

`	Source Driver Output			
ImageData	DDX=1(Default)		DDX=0	
Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select
00	Gray0	ogray00	Gray3	ogray03
01	Gray1	ogray01	Gray2	ogray02
10	Gray2	ogray02	Gray1	ogray01
11	Gray3	ogray03	Gray0	ogray00

Data mapping example:

When DDX=1, Pixel[1:0]=01 -> Gray level select = Gray1, follow LUT data output from IP output port "ogray01".

When DDX=0, Pixel[1:0] = 11 -> Gray level select = Gray 0, follow LUT data output from IP output port "ogray00".

R11H(DSP): DataStop Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DSP	W	0	0	0	0	1	0	0	0	1	(11H)
1st Parameter	R	1	data_flag	-	-	-	-	-	-	-	(00H)

To stop data transmission,this command must be issued to check the data_flag.

1st Parameter:

Bit7	Data flag of receiving user data.
0	Driver didn't receive all the data.
1	Driver has already received all the one frame data.

After "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.

This command only active when BUSY_N = "1".

R12H(DRF): Display Refresh Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DRF	W	0	0	0	0	1	0	0	1	0	(12H)
1st Parameter	W	1	-	-	-	-	-	-	-	AC/DCVCOM	(00H)

While user sent this command,driver will refresh display(data/VCOM) base on SRAM data and LUT.

AC/DCVCOM: AC,DC VCOM select.

0: ACVCOM,VCOM will follow LUT when updating image. (default)

1: DCVCOM,VCOM will always be VCOMDC when updating image

After display refresh command, BUSY_N signal will become "0"

This command only active when BUSY_N = "1".

R17H(AUTO): Auto Sequence Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Auto Sequence	W	0	0	0	0	1	0	1	1	1	(17H)
	W	1	1	0	1	0	0	1	0	1	(A5H)

The command can enable the internal sequence to execute several commands continuously.

The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO(0x17)+Code(0xA5)=(PON → DRF → POF)

AUTO(0x17)+Code(0xA7)=(PON → DRF→ POF → DSLP)

R30H(PLL): PLL Control Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PLL	W	0	0	0	1	1	0	0	0	0	(30H)
1st Parameter	W	1	-	-	-	-	Dyna	FR[2]	FR[1]	FR[0]	(02H)

The command controls the PLL clock frequency.The PLL structure must support the following frame rates:

Bit3	Dynamic frame rate (EInk use only)
0	Disable(default)
1	Enable

FR[2:0]	Framerate
000	12.5 Hz
001	25 Hz
010	50 Hz (default)
011	65 Hz
100	75 Hz
101	85 Hz
110	100 Hz
111	120 Hz

R40H(TSC): Temperature Sensor Command Register

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TSC	W	0	0	1	0	0	0	0	0	0	(40H)
1st Parameter	R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	(00H)
2nd Parameter	R	1	D2	D1	D0	-	-	-	-	-	(00H)

This command indicates the temperature value.

BUSY_N become low after TSC command. When BUSY_N become high, Parameter can be read.

This command only active when BUSY_N="1"

Temperature boundary: -25C~60C

TS[7:0]/D[10:3]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
...	...
1111_1110	-2
1111_1111	-1

TS[7:0]/D[10:3]	Temperature (°C)
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
...	...
0011_1011	59
0011_1100	60

R41H(TSE): Temperature Sensor Enable Register

`	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TSE	W	0	0	1	0	0	0	0	0	1	(41H)
1st Parameter	W	1	0	-	-	-	TO[3]	TO[2]	TO[1]	TO[0]	(00H)

This command indicates the driver IC temperature sensor enable and calibration function.

Bit3-0	Temperature level	Bit3-0	Temperature level
0000	+0℃(Default)	1000	-4℃
0001	+0.5℃	1001	-3.5℃
...	...	...	...
0111	+3.5℃	1111	-0.5℃

Bit[3:0]: Reserve one temperature offset TO[3:0] for calibration

1. TO[3]: mean "+" or "-" while 0 is "+"; 1 is "-"

2. TO[2:0]: mean temperature offset value

R44H(GPI Sensing): GPIO Input Register

`	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Check Panel Glass	W	0	0	1	0	0	0	1	0	0	(44H)
	W	1	-	-	-	-	-	-	-	GPIS	(00H)

This command will indicate status of GPI

GPIS : 0 detected low logic on GPIO

1 detected high logic on GPIO

R50H(CDI): VCOM and DATA Interval Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
CDI	W	0	0	1	0	1	0	0	0	0	(50H)
1st Parameter	W	1	VBD[2]	VBD[1]	VBD[0]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	(97H)

This command can set 2 kinds of parameters,1.VCOM to data output interval(CDI) 2.Border pin output.

VBD[2:0]: Border data selection (from LUT output by IP port border_w[1:0]).

This register will make border pin output being mapped to a certain grayscale.

DDX[0]	VBD[2:0]	Gray level select	IP setting for Border LUT select
0	000	Floating	N/A
	001	Gray3	border_buf=011
	010	Gray2	border_buf=010
	011	Gray1	border_buf=001
	100	Gray0	border_buf=000
1 (Default)	000	Gray0	border_buf=000
	001	Gray1	border_buf=001
	010	Gray2	border_buf=010
	011	Gray3	border_buf=011
	100	Floating(Default)	N/A

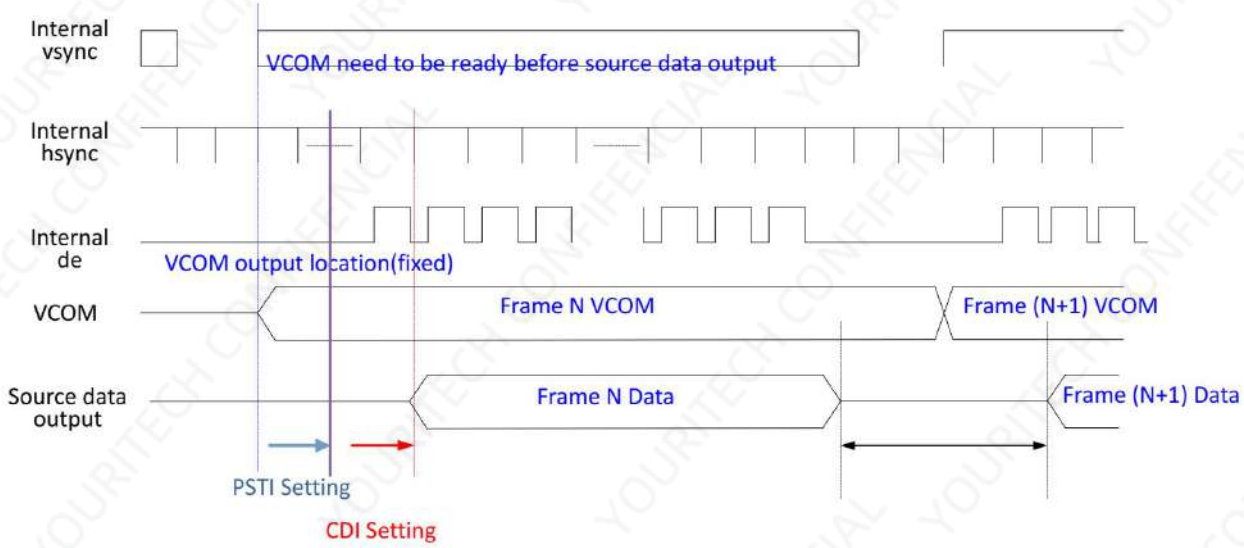
Border output voltage level: The level selection is based on mapping LUT data.

Ex: Gray 1 waveform is mapping to 15V, without VCOM offset,the real output on Border pin shall be 15V+VCOMDC.

Border output will follow FOPT definition being defined in R00h.

This command indicates the interval of Vcom and data output.When setting the vertical backporch, the total blanking will be kept as a default value (count by HSYNC)

Bit3	Bit2	Bit1	Bit0	VCOM and data interval
0	0	0	0	17 hsync
0	0	0	1	16 hsync
0	0	1	0	15 hsync
0	0	1	1	14 hsync
0	1	0	0	13 hsync
0	1	0	1	12 hsync
0	1	1	0	11 hsync
0	1	1	1	10 hsync (Default)
1	0	0	0	9 hsync.
1	0	0	1	8 hsync
1	0	1	0	7 hsync
1	0	1	1	6 hsync
1	1	0	0	5 hsync
1	1	0	1	4 hsync
1	1	1	0	3 hsync
1	1	1	1	2 hsync



R51H(LPD): Lo wer Power Detection Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
LPD	W	0	0	1	0	1	0	0	0	1	(51H)
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	(01H)

This command indicates the input power condition. Host can read this data to understand the battery condition.

When LPD="1",system input power is normal.

When LPD="0",Low power input (VDD<2.5V,selected by LVD_SEL[1:0] in command LVSEL)

Bit0	LPD
0	Lowpowerinput.
1	Normalstatus.(Default)

This command only active when BUSY_N="1".

R60H (TCON): TCON setting Register

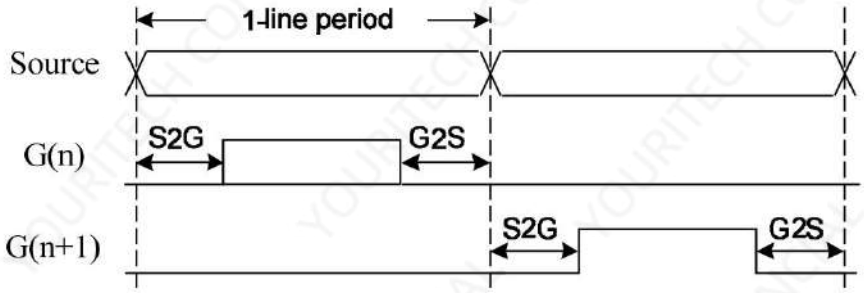
Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TSC	W	0	0	1	1	0	0	0	0	0	(60H)
1st Parameter	W	1	-	-	S2G[5]	S2G[4]	S2G[3]	S2G[2]	S2G[1]	S2G[0]	(02H)
2nd Parameter	W	1	-	-	G2S[5]	G2S[4]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	(02H)

The command define as Non-overlap period of gate and source and as below:

S2G[5:0] or G2S[5:0]	Period
0	1unit
1	2unit
2	3unit(Default)
3	4unit
4	5unit
5	6unit
6	7unit
7	8unit
8	9unit
9	10unit
10	12unit
11	14unit
12	16unit
13	18unit
....	...
63	118unit

1 unit = 500ns

Gon_T= 1 line period – S2G –G2S, minimum Gon_T = 2 units. If(1line period – S2G –G2S) <2 units , Gon_T = 2 units



R61H(TRES): Resolution Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TRES	W	0	0	1	1	0	0	0	0	1	(61H)
1st Parameter	W	1	0	0	0	0	0	0	HRES(9)	HRES(8)	(00H)
2nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	(00H)
3rd Parameter	W	1	0	0	0	0	0	0	VRES(9)	VRES(8)	(00H)
4th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	(00H)

Note: HRES ≦ Horizontal line of PSR, VRES ≦Vertical line of PSR.

No matter what value being set in D1 and D0 of 1st parameter(HRES[1] and HRES[0]), the register shall be kept as 0

When using register:

Horizontal display resolution = HRES

Vertical display resolution = VRES

Channel disable calculation:

GD: First G active=G0; LAST active GD = first active+VRES[9:0]-1

SD: First active channel:=S0; LAST active SD = first active+HRES[9:2]*4-1

R65H(GSST): GATE/SOURCE START SETTING

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GSST	W	0	0	1	1	0	0	1	0	1	(65H)
1st Parameter	W	1	0	0	0	0	0	0	HST (9)	HST (8)	(00H)
2nd Parameter	W	1	HST (7)	HST (6)	HST (5)	HST (4)	HST (3)	HST (2)	0	0	(00H)
3rd Parameter	W	1	0	0	0	0	0	0	VST (9)	VST (8)	(00H)
4th Parameter	W	1	VST (7)	VST (6)	VST (5)	VST (4)	VST (3)	VST (2)	VST (1)	VST (0)	(00H)

This command defines resolution start gate/source position.

HST[9:2]:Horizontal Display Start Position (Source)

VST[9:0]:Vertical Display Start Position (Gate)

R70H(REV): Chip Revision Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
REV	W	0	0	1	1	1	0	0	0	0	(70H)
1st Parameter	R	1	REV0[7]	REV0[6]	REV0[5]	REV0[4]	REV0[3]	REV0[2]	REV0[1]	REV0[0]	(0EH)
2nd Parameter	R	1	REV1[7]	REV1[6]	REV1[5]	REV1[4]	REV1[3]	REV1[2]	REV1[1]	REV1[0]	(04H)
3rd Parameter	R	1	REV2[7]	REV2[6]	REV2[5]	REV2[4]	REV2[3]	REV2[2]	REV2[1]	REV2[0]	(01H)

1st Parameter:

Bit7-0	REV0
-	EInk internal number

2nd Parameter:

Bit7-0	REV1
-	EInk internal number

3rd Parameter:

Bit7-0	REV2
-	Increased each revision

R80H(AMV): Auto Measurement VCOM Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
AMV	W	0	1	0	0	0	0	0	0	0	(80H)
1st Parameter	W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	AMVX	AMVS	AMV	AMVE	(00H)

This command is to set the configuration of VCOM sensing.

This command only active when BUSY_N="1"

1st Parameter:

Bit7-6	The sensing points of sampling time
00	2(default)
01	4
10	8
11	16

Sampling time= the last quarter of sensing time (T)

VCOM = average of N points. N=2,4,8,16

Bit5-4	The sensing time of VCOM detection
00	5s(default)
01	10s
10	15s
11	20s

Bit3	XON setting for all Gate ON of AMV
0	Gate scan normally during Auto Measure VCOM period.(default)
1	All Gate ON during Auto Measure VCOM period.

Bit2	AMVS setting for Source output of AMV
0	Source output 0V during Auto Measure VCOM period.(default)
1	Source output VSPL during Auto MeasureVCOM period.

Bit1	Analogy signal
0	Get VCOM value by R81H(default)
1	Gate scan only. Measure VCOM externally by probing the VCOM pad.

Bit0	Auto Measure VCOM setting
0	Auto measure VCOM disble (default)
1	Auto measure VCOM enable

R81H(VV): VCOM Value Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VV	W	0	1	0	0	0	0	0	0	1	(81H)
1st Parameter	R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	(00H)

This command gets Vcom value.

1st Parameter:

Bit6-0	VCOM value
0000000	0V
0000001	-0.05V
0000010	-0.10V
⋮	⋮
1010000	-4.00V
Others	-

R82H(VDCS): VCM_DC Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VDCS	W	0	1	0	0	0	0	0	1	0	(82H)
1st Parameter	W	1	OTP_VCM	VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	(00H)

This command set the VCOMDC value. Driver will base on this value for VCM_DC.

1st Parameter:

Bit7	Follow OTP VCOM value in OTP mode
0	IP output value(default)
1	From the setting register

Bit6-0	VCOM value
0000000	0V(default)
0000001	-0.05V
0000010	-0.10V
⋮	⋮
1010000	-4.00V
Others	-

R90H(PGM): Program Mode

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Ente rProgram Mode	W	0	1	0	0	1	0	0	0	0	(90H)

After this command is issued,the chip would enter the program mode.

After the programming procedure completed,a hardware reset is necessary for leaving program mode

R91H(APG): Active Program

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Active Program OTP	W	0	1	0	0	1	0	0	0	1	(91H)

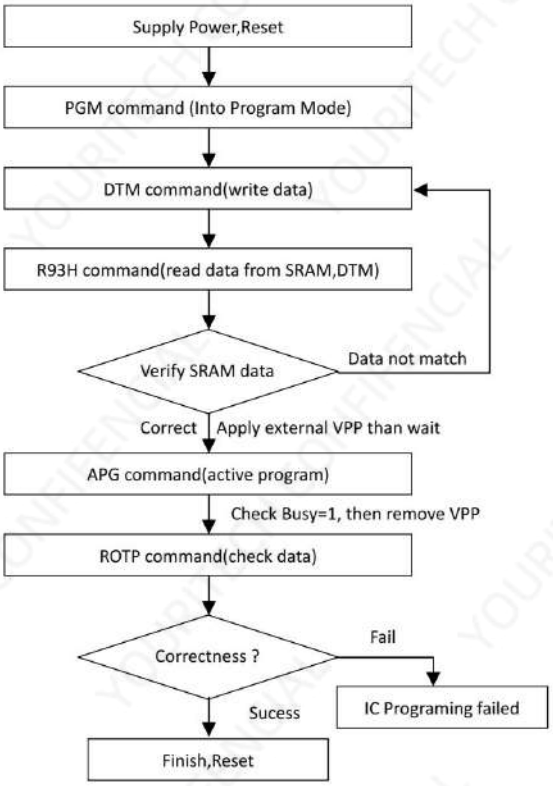
After this command is transmitted,the programming state machine would be activated.

The BUSY_N flag would fall to 0 until the programming is completed.

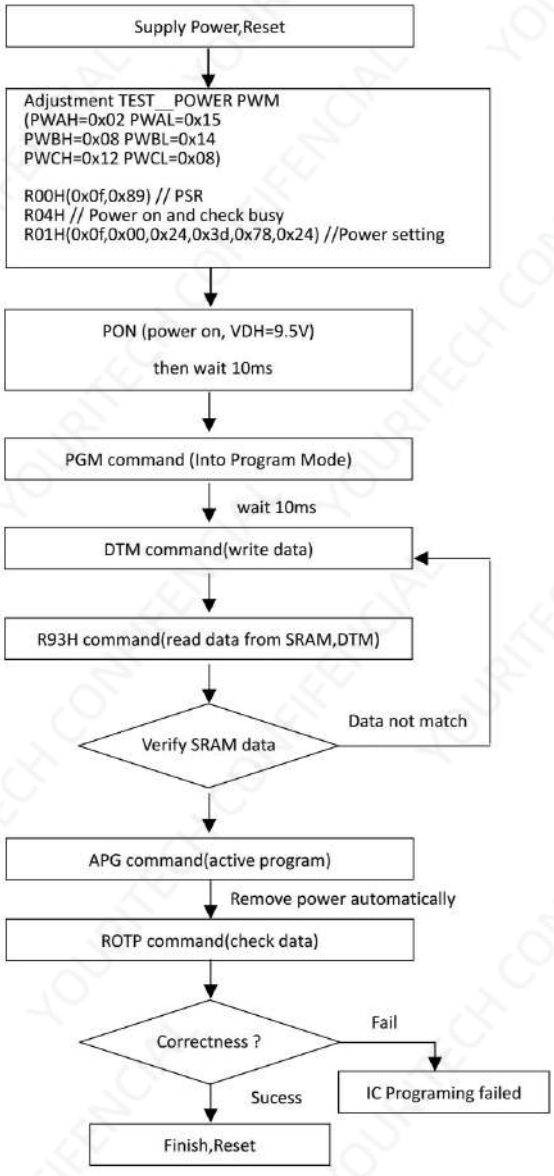
This command only active when BUSY_N="1"

R92H(ROTP): Read OTP Data

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Read OTP Data	W	0	1	0	0	1	0	0	1	0	(92H)
	R	1	Dummy								(00H)
	R	1	The data of address0 in the OTP								(00H)
	R	1									(00H)
	R	1	The data of address(n) in the OTP								(00H)



OTP Programming Flow (External VPP)



OTP Programming Flow (Internal VPP)

R93H(RSRAM):Read SRAM Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Read SRAM Data	W	0	1	0	0	1	0	0	1	1	(93H)
	R	1	Dummy								(00H)
	R	1	The data of address0 in the SRAM								(00H)
	R	1									(00H)
	R	1	The data of address(n) in the SRAM								(00H)

RA2H(PGM_CFG):OTP Program Config Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
OTP program Config	W	0	1	0	1	0	0	0	1	0	(A2H)
1st Parameter	W	1	-	-	-	VPPSEL	-	-	-	-	(00H)
2nd Parameter	W	1	PGM_SADDR[15:8]								(00H)
3rd Parameter	W	1	PGM_SADDR[7:0]								(00H)
4th Parameter	W	1	PGM_DSIZE[15:8]								(15H)
5th Parameter	W	1	PGM_DSIZE[7:0]								(DFH)

This command is to set the configuration of OTP

1st Parameter

Bit4	VPPSEL
0	External VPP **(default)**
1	Internal VPP

2nd and 3rd Parameters: Program start address PGM_SADDR[15:0]

4th and 5th Parameters: Program data size PGM_DSIZE[15:0]

Default PGM_DSIZE[15:0] is 0x15DF.

RA3H(PGM_STAT):OTP Program Status Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
OTP program Status	W	0	1	0	1	0	0	0	1	1	(A3H)
1st Parameter	W	1	-	-	-	-	-	-	PGM_VER_ERR	PGM_EXE_ERR	(00H)

This command is to read OTP Program status

1st Parameter:

Bit1	Data verification of APG
0	OK
1	NOK

Bit0	OTP program execution status
0	Normal
1	Invalid APG setting

RE0H(CCSET):Chip Temperature Input Select Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Temperature Input	W	0	1	1	1	0	0	0	0	0	(E0H)
1st Parameter	W	1	-	-	-	-	-	-	TSFIX	CCEN	(00H)

This command is control input path of temperature value

1st Parameter:

Bit0	Output clock enable/disable
0	Output 0v at CL pin **(default)**
1	Ouptut clock at CL pin for alave chip.**(Cascade mode)**

CCEN=1 : The master temperature is synchronized with the salve. This setting needs to wait until BUSY_N="1".

Bit1	Temperature Input Selection
0	Use temperature sensor **(default)**
1	Use TSSET[7:0] value

RE4H(LVSEL): LVD Voltage Select Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Select LVD Voltage	W	0	1	1	1	0	0	1	0	0	(E4H)
1st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		(03H)

LVD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVDvalue
00	<2.2V
01	<2.3V
10	<2.4V
11	<2.5V (default)

RE6H(TSSET): Force Temperature Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Force Temperature	W	0	1	1	1	0	0	1	1	0	(E6H)
1st Parameter	W	1	TS[7]	TS[6]	TS[5]	TS[4]	TS[3]	TS[2]	TS[1]	TS[0]	(00H)

TS[7:0]: Temperature boundary: -25C~60C

When TSFIX=1, Internal TS is disable, Temperature value will be set by TS[7:0].

TS[7:0]	Temperature (°C)	TS[7:0]	Temperature (°C)
1110_0111	-25	0000_0000	0
1110_1000	-24	0000_0001	1
1110_1001	-23	0000_0010	2
1110_1010	-22	0000_0011	3
1110_1011	-21	0000_0100	4
1110_1100	-20	0000_0101	5
1110_1101	-19	0000_0110	6
…	…	…	…
1111_1110	-2	0011_1011	59
1111_1111	-1	0011_1100	60

RFFH(TEST): Enter TEST MODE

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	1	1	1	1	1	(FFH)
1st Parameter	W	1	1	0	1	0	0	1	0	1	(A5H)

TEST(0xFF)+Code(0xA5)=Enter TEST MODE

RFFH(TEST): Exit TEST MODE

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	1	1	1	1	1	(FFH)
1st Parameter	W	1	1	1	1	0	0	0	1	1	(E3H)

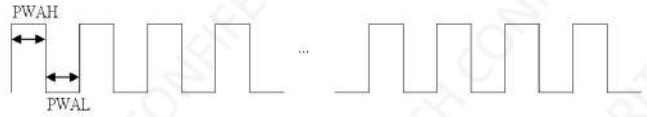
TEST(0xFF)+Code(0xE3)=Exit TEST MODE

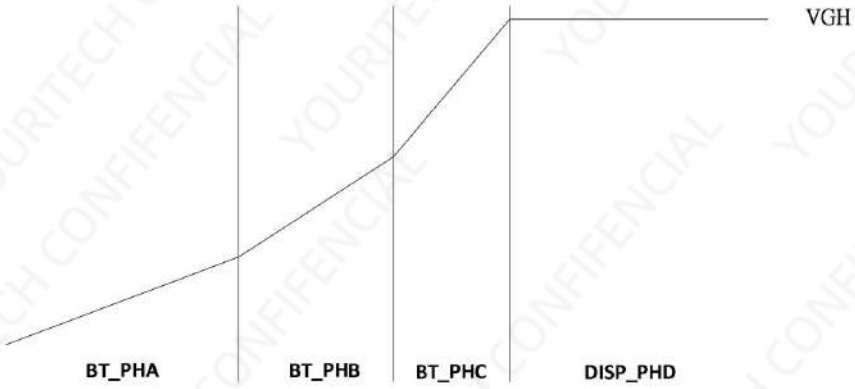
REFH(TEST): POWER PWM Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	0	1	1	1	1	(EFH)
1st Parameter	W	1	BT_PWAH								(01H)
2nd Parameter	W	1	BT_PWAL								(03H)
3rd Parameter	W	1	BT_PWBH								(03H)
4th Parameter	W	1	BT_PWBL								(0AH)
5th Parameter	W	1	BT_PWCH								(04H)
6th Parameter	W	1	BT_PWCL								(20H)
7th Parameter	W	1	DISP_PWDH								(06H)
8th Parameter	W	1	DISP_PWDL								(20H)

1nd Parameter:

Bit7-0	PWxH/L time
00H	0 ns
01H	125 ns
02H	250 ns
03H	375 ns
04H	500 ns
:	:
FCH	31500ns
FDH	31625ns
FEH	31750ns
FFH	31875ns





1st、2nd parameter : correspond to the PWM duty cycle within a specified time for the R06H command BT_PHA.

3rd、4th parameter : correspond to the PWM duty cycle within a specified time for the R06H command BT_PHB.

5th、6th parameter : correspond to the PWM duty cycle within a specified time for the R06H command BT_PHC.

7th、8th parameter : the PWM duty cycle within display refresh(DISP_PHD).

RC9H(TEST): GDROTP

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	0	1	0	0	1	(C9H)
1st Parameter	W	1	GDR_OTP_R								(F8H)

Adjust the GDR driving for the three-stage voltage boosting during POWER ON and display refresh.

Bit7-6	GDR driving within DISP_PHD
Bit5-4	GDR driving within BT_PHC
Bit3-2	GDR driving within BT_PHB
Bit1-0	GDR driving within BT_PHA

RDCH(TEST): CPCK SET enable

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	0	0	(DCH)
1st Parameter	W	1	0	0	0	0	CPCK_SEL		CPCKDFEN	CPCKEN	(0FH)

Bit0	CPCK enable 0:OFF 1:ON
Bit1	CPCKDFEN :CPCK PWH SET & CPCK PWL SET enable 1:follow default 0:follow RDDH & RDEH
Bit3-2	CPCK_SEL : 00:8Mhz, 01:1Mhz, 10:2Mhz, 11:4Mhz(default)

RDDH(TEST): CPCK PWH SET

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	0	1	(DDH)
1st Parameter	W	1	CPCK PWH SET								(08H)

Adjust the sampling frequency of VDH/VDL/VDHR clamping.

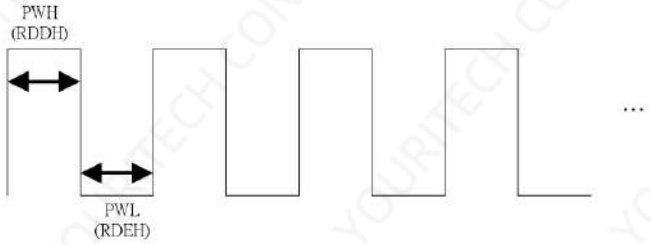
Bit7-0	CPCK PWH SET	Bit7-0	CPCK PWH SET
00H	0 ns	:	:
01H	125 ns	FCH	31500ns
02H	250 ns	FDH	31625ns
03H	375 ns	FEH	31750ns
04H	500 ns	FFH	31875ns

RDEH(TEST): CPCK PWL SET

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	1	0	(DEH)
1st Parameter	W	1	CPCK PWL SET								(08H)

Adjust the sampling frequency of VDH/VDL/VDHR clamping.

Bit7-0	
00H	0 ns
01H	125 ns
02H	250 ns
03H	375 ns
04H	500 ns
:	:
FCH	31500ns
FDH	31625ns
FEH	31750ns
FFH	31875ns



RDFH(TEST): VD_Select

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	1	1	(DFH)
1st Parameter	W	1	0	0	VDHR_SEL		VDH_SEL		VDL_SEL		(3FH)

Bit5-4	VDHR driving	00:weak	11:strong
Bit3-2	VDH driving	00:weak	11:strong
Bit1-0	VDL driving	00:weak	11:strong

RA8H(TEST): VDHROS_EN

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	0	1	0	1	0	0	0	(A8H)
1st Parameter	W	1	0	0	1	1	1	1	1	VDHROS EN	(3FH)

Bit0	VDHR O.S. enable
0	OFF
1	ON(default)

RE8H(TEST): VDLOS_Select

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	0	1	0	0	0	(E8H)
1st Parameter	W	1	0	0	0	0	0	0	VDLOS_SEL		(01H)

Bit1-0	Adjusting VDL O.S. driving 00: strong 11:weak

RFDH(TEST): VDLOS_EN

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	1	1	1	0	1	(FDH)
1st Parameter	W	1	0	0	0	0	0	0	0	VDLOS EN	(01H)

Bit0	VDL O.S. enable
0	OFF
1	ON (default)

8. Optical Specifications

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	Indoor	8:1		-		8-2
T update	Image update time	at 25 °C		26	-	sec	
Life		Topr		1000000times or 5years			

Notes: 8-1. Luminance meter: Eye-One Pro Spectrophotometer.
8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

9. Handling, Safety and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

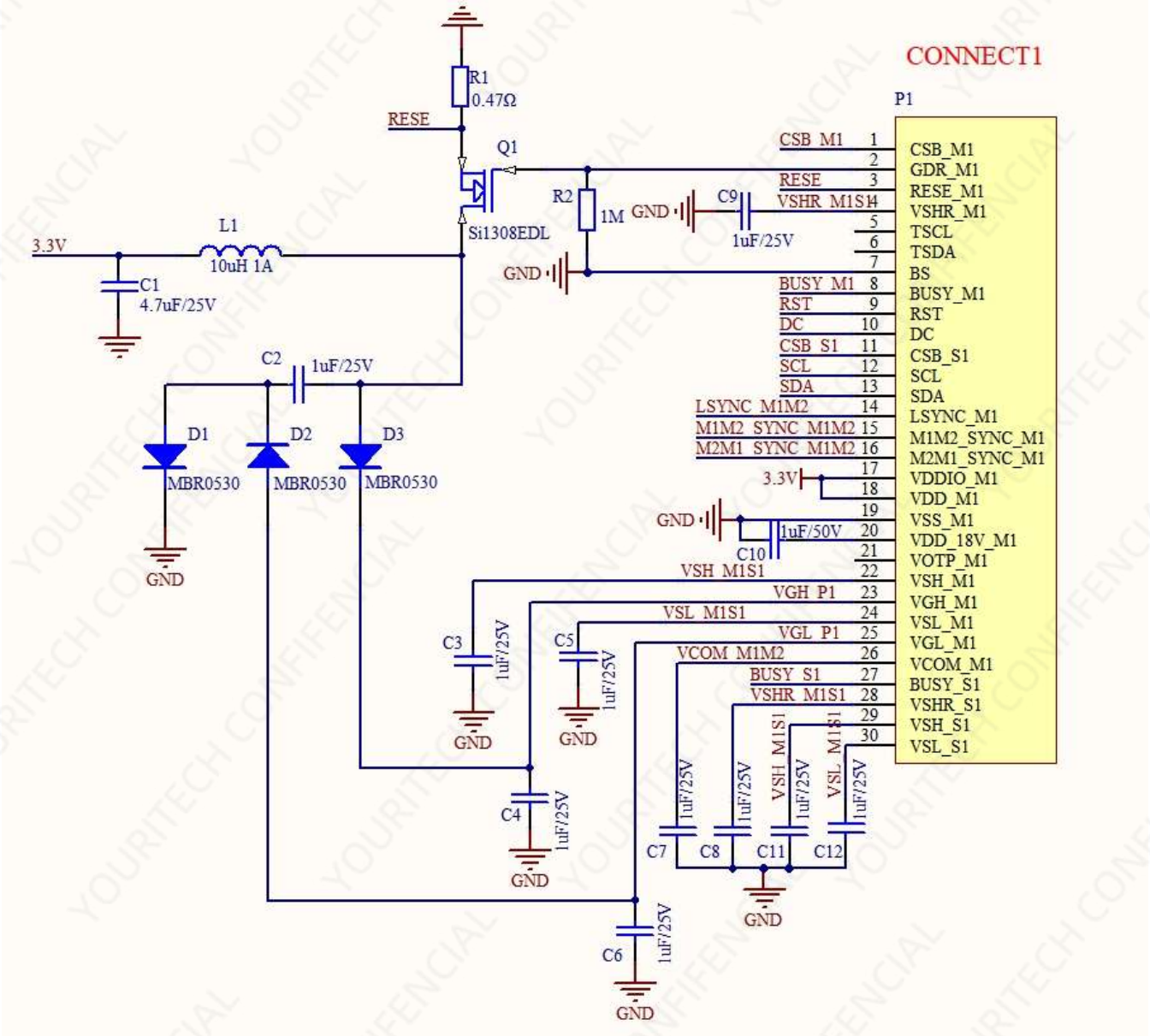
Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

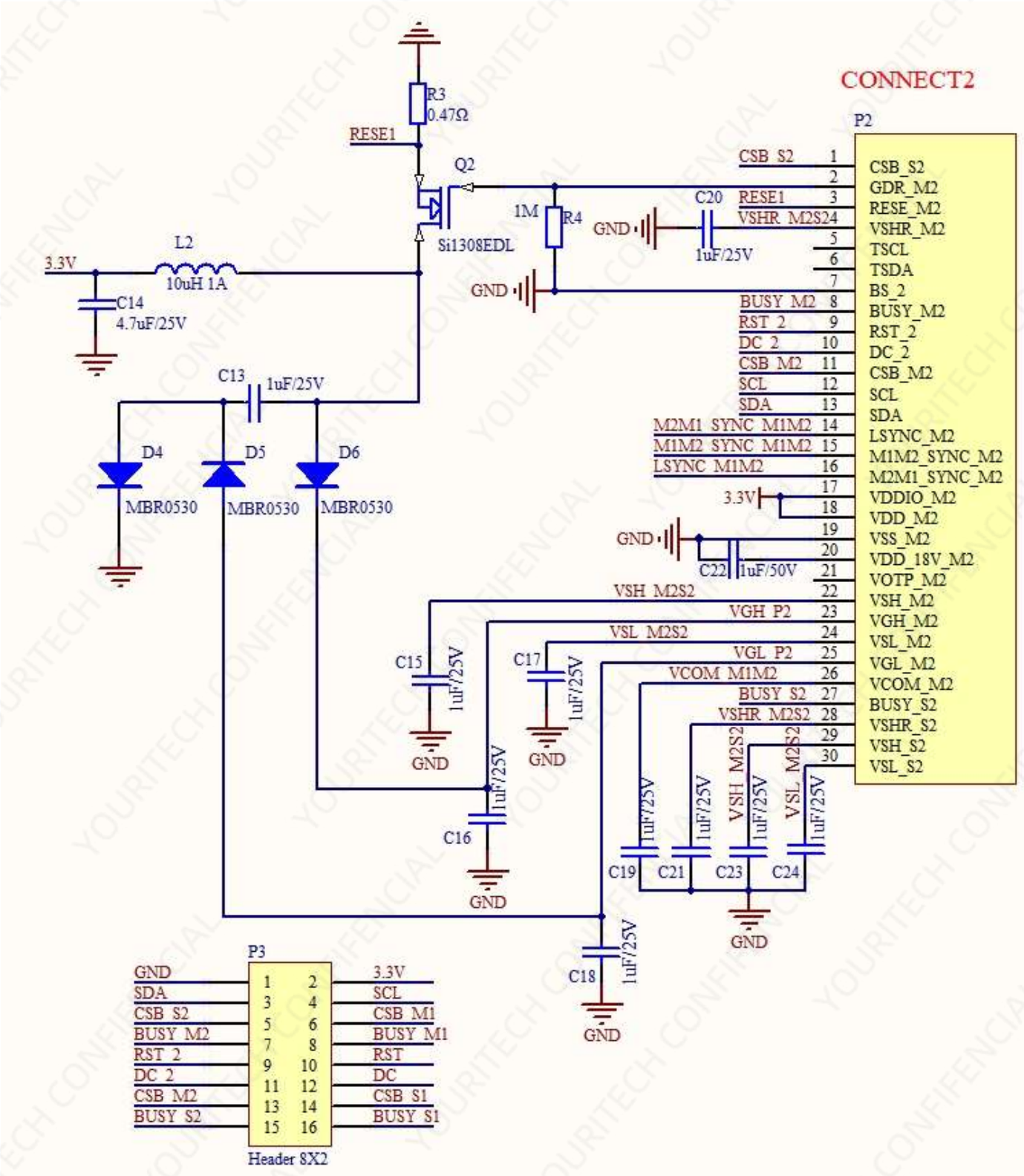
10. Reliability test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=60° C，RH=35%，240h Test in white pattern
3	High-Temperature Operation	T=40° C，RH=35%，240h
4	Low-Temperature Operation	T=0° C，240h
5	High-Temperature, High-Humidity Operation	T=40° C，RH=80%，240h
6	High Temperature, High Humidity Storage	T=50° C，RH=90%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25℃ 30min]→[+60℃ 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m² for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display, no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.

11. Typical Application Circuit




CONNECT2
P2
R3
0.47Ω
RESE1
Q2
Si1308EDL
1M
R4
C20
1uF/25V
L2
10uH 1A
3.3V
C14
4.7uF/25V
C13
1uF/25V
D4
D5
D6
MBR0530
MBR0530
MBR0530
GND
C22
1uF/50V
C15
C16
C17
C18
C19
C21
C23
C24
VSH M2S2
VSL M2S2
P3
Header 8X2

Part Name	Requirements for spare part
C1—C24	0603/0805; X5R/X7R;Voltage Rating:≥25V
R1—R4	0603/0805;1% variation,≥0.05W
D1—D6	MBR0530: 1)Reverse DC Voltage≥30V 2)Io≥500mA 3)Forward voltage ≤430mV
Q1、Q2	Si1308EDL:1)Drain-Source breakdown voltage≥30V 2)Vgs(th)≤1.5V 3)Rds(on)≤400mΩ
L1、L2	NR3015: Io=1000mA(max)
P1、P2	30pins,0.5mm pitch