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MODEL NO : ET028QV03-TT

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-12-17

□Preliminary Specification

■Final Product Specification

Customer :_____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 240xRGBx320
As to basic specification of the driver IC, refer to the IC (Sitronix:ST7789T3) specification and data book.
All material & processing of the LCD module should be Lead Free.

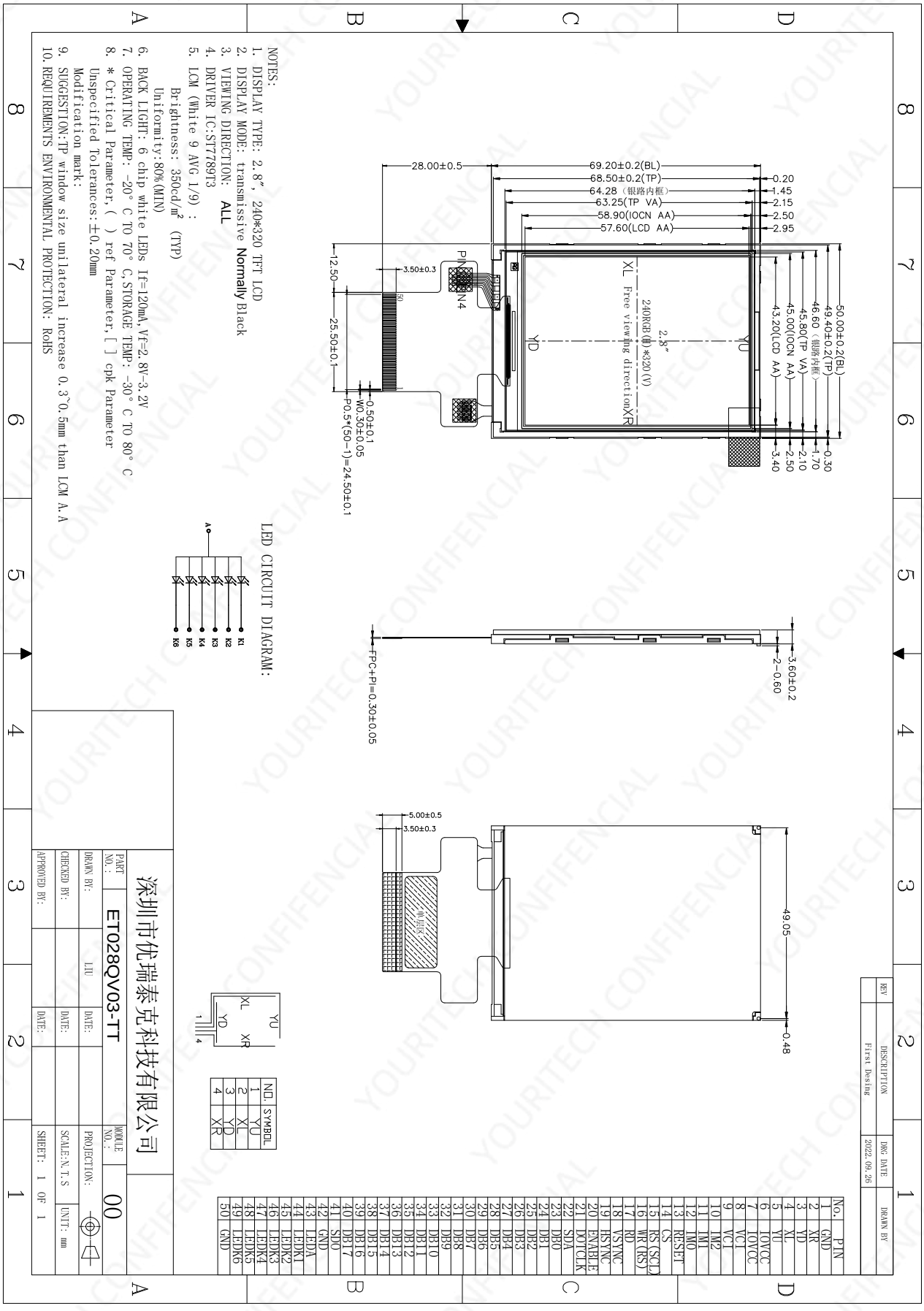
1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL+RTP;
IPS Type LCD
240 dot-segment and 320 dot-common outputs;
65K\262K Color can be selected by software;
White LED back light;
SPI\MCU\RGB interface

1.3 Applications:

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally black	--
Drive element	TFT active matrix	--
Number of pixels	240*3RGB(H)X320(V)	Dots
Pixel arrangement	RGB stripe	--
Pixel Pitch (H*V)	0.180(H) x0.180 (V)	mm
Active area	43.20(H) x 57.60(V)	mm
LCM Size(W*H*T)	50.00(W)x69.20(H)x2.00(T)	mm
LCM+RTP Size(W*H*T)	49.40(W)x68.50(H)x3.60(T)	mm
Viewing direction	ALL O'CLOCK	-
TFT Driver IC	ST7789T3	-
TFT interface	SPI\MCU\RGB interface	-
Approx. Weight	TBD	g
Touch structure		
Touch Driver IC		-
Touch Interface		


NOTES:
1. DISPLAY TYPE: 2.8", 240*320 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL
4. DRIVER IC:ST7789T3
5. LCM (White 9 AVG 1/9) :
Brightness: 350cd/m² (TYP)
Uniformity:80%(MIN)
6. BACK LIGHT: 6 chip white LEDs If=120mA,Vf=2.8V~3.2V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
Unspecified Tolerances:±0.20mm
Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS
LED CIRCUIT DIAGRAM:
A
K1
K2
K3
K4
K5
K6
28.00±0.5
69.20±0.2(BL)
68.50±0.2(TP)
64.28（银路内框）
63.25(TP VA)
58.90(IOCN AA)
57.60(LCD AA)
0.20
1.45
2.15
2.50
2.95
50.00±0.2(BL)
49.40±0.2(TP)
46.60（银路内框）
45.80(TP VA)
45.00(IOCN AA)
43.20(LCD AA)
0.30
1.70
2.10
2.50
3.40
2.8"
240RGB(W)*320(V)
Free viewing directionXR
XL
YU
YD
PIN1
PIN40
FILTER
3.50±0.3
12.50
25.50±0.1
0.50±0.1
W0.30±0.05
P0.5*(50-1)=24.50±0.1
FPC+PI=0.30±0.05
3.60±0.2
2-0.60
5.00±0.5
3.50±0.3
49.05
0.48
YU
XL
XR
YD
1
4
NO. SYMBOL
1 YU
2 XL
3 YD
4 XR
No. PIN
1 GND
2 XR
3 YD
4 XL
5 YU
6 IOVCC
7 IOVCC
8 VCI
9 VCI
10 IM2
11 IM1
12 IM0
13 RESET
14 CS
15 RS (SCL)
16 WR (RS)
17 RD
18 VSYNC
19 HSYNC
20 ENABLE
21 DOTCLK
22 SDA
23 DB0
24 DB1
25 DB2
26 DB3
27 DB4
28 DB5
29 DB6
30 DB7
31 DB8
32 DB9
33 DB10
34 DB11
35 DB12
36 DB13
37 DB14
38 DB15
39 DB16
40 DB17
41 SDO
42 GND
43 LEDA
44 LEDK1
45 LEDK2
46 LEDK3
47 LEDK4
48 LEDK5
49 LEDK6
50 GND
REV
DESCRIPTION
First Desing
DRG DATE
2022.06.26
DRAWN BY
深圳市优瑞泰克科技有限公司
PART NO.: ET028QV03-TT
MODULE NO.: 00
DRAWN BY: LIU
DATE:
PROJECTION:
CHECKED BY:
DATE:
SCALE:N.T.S
UNIT: mm
APPROVED BY:
DATE:
SHEET: 1 OF 1

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
TP Operating Temperature & Humidity (20% ~ 90%RH)	T_{OPR}	-20	+70	°C
TP SStorage Temperature & Humidity (20% ~ 90%RH)	T_{STG}	-30	+80	°C
Humidity	RH	-	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.5	2.8	3.3	V
Supply Voltage for(DC/DC)	AVDD				V
Supply Voltage for(DC/DC)	AVEE				V

4.2Back-Light Unit Characeristics

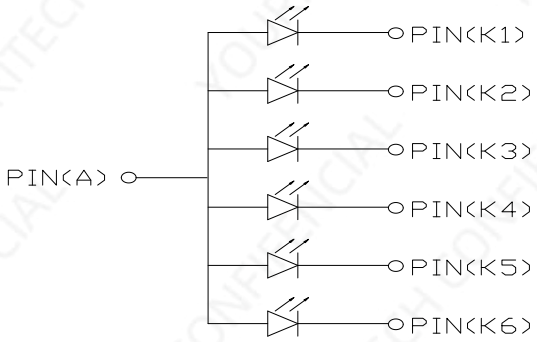
The back-light system is an edge-lighting type with 6 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	2.8	-	3.2	V	-
Forward current	I_F	--	120	-	mA	-
Luminance(With LCD+RTP)	Lv		350	--	cd/m^2	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

LCM Pin Descriptions

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Functional</th></tr>
<tr><td>1</td><td>GND</td><td>Power Ground</td></tr>
<tr><td>2</td><td>XR</td><td>Touch panel coordinate in the Right</td></tr>
<tr><td>3</td><td>YD</td><td>Touch panel coordinate in the Down</td></tr>
<tr><td>4</td><td>XL</td><td>Touch panel coordinate in the Left</td></tr>
<tr><td>5</td><td>YU</td><td>Touch panel coordinate in the Up</td></tr>
<tr><td>6~7</td><td>IOVCC(1.8V)</td><td>I/O Voltage (VDDI to DGND): 1.65V ~ 3.3V</td></tr>
<tr><td>8~9</td><td>VDD(2.8V)</td><td>Power supply 2.5V ~ 3.3V</td></tr>
<tr><td>10</td><td>IM2</td><td rowspan="3"><table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th><th>Data pin</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>80-16bit parallel I/F Ⅱ</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>80-8bit parallel I/F Ⅱ</td><td>DB[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-18bit parallel I/F Ⅱ</td><td>DB[17:0],</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-9bit parallel I/F Ⅱ</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-line 9bit serial I/F Ⅱ</td><td>SDA: in/ SDO: out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-line 8bit serial I/F Ⅱ</td><td>SDA:in/ SDO: out</td></tr>
</table></td></tr>
<tr><td>11</td><td>IM1</td></tr>
<tr><td>12</td><td>IM0</td></tr>
<tr><td>13</td><td>RESET</td><td>Reset signal input terminal. Active at ‘L’.</td></tr>
<tr><td>14</td><td>CSX</td><td>A chip select signal</td></tr>
<tr><td>15</td><td>RS/SCL</td><td>Register selection signal.</td></tr>
<tr><td>16</td><td>WR/RS</td><td>Write strobe signal.</td></tr>
</table>

17	RD	Read data at the rising edge.
18	VSYNC	Vertical sync. Signal in RGB I/F.
19	HSYNC	Horizontal sync. Signal in RGB I/F.
20	ENABLE	Data enable signal in RGB I/F mode 1.
21	PCLK	Pixel clock signal in RGB I/F.
22	SDA	SPI interface input pin.
23~40	DB0~DB17	RGB interface or MCU parallel interface data bus.
41	SDO	SPI interface output pin.
42	GND	Power Ground
43	LEDA	POWER SUPPLY+ FOR BACKLIGHT ANODE
44~49	LEDK1~LEDK6	POWER SUPPLY- FOR BACKLIGHT CATHODE
50	GND	Power Ground

6. Timing Characteristics

VDDI and VDD can be applied in any order.

In CABC function application, VDDI power on need delay 5ms after VDD has been supplied.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

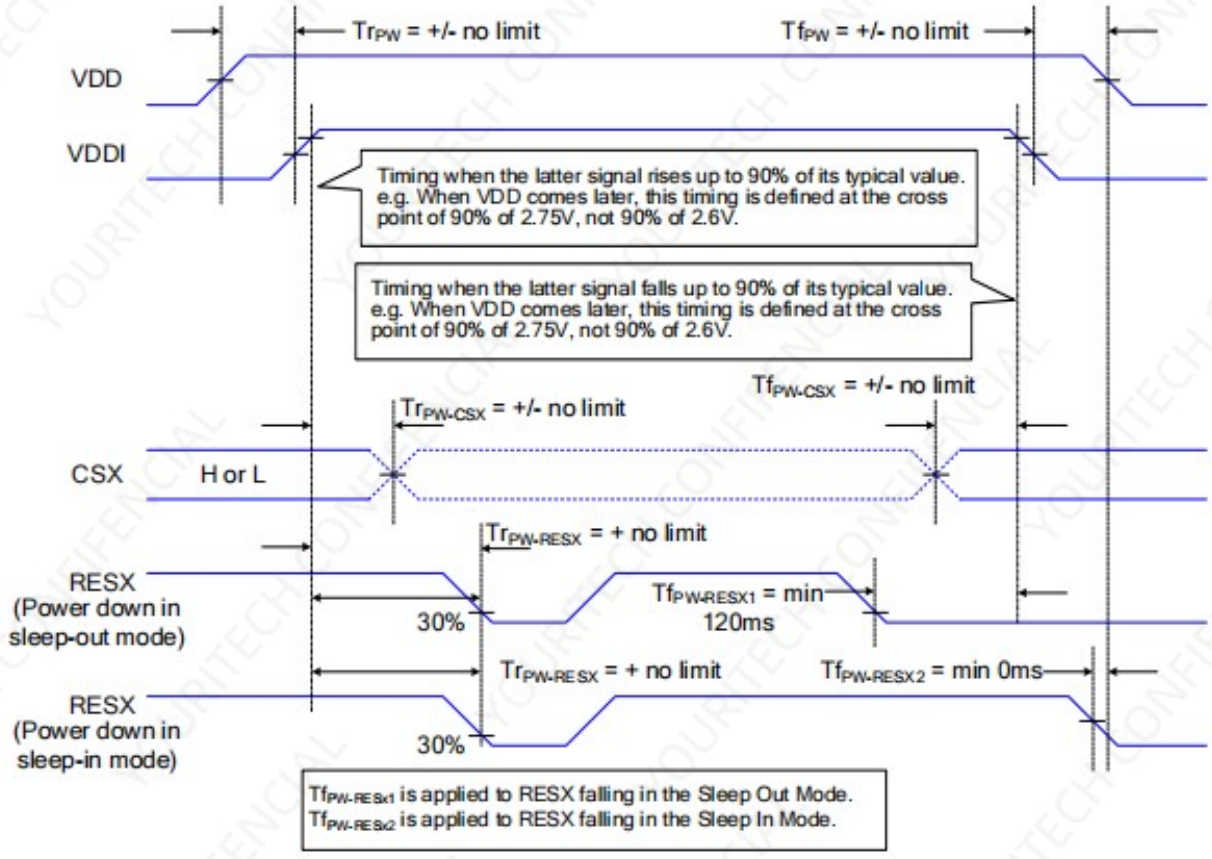
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

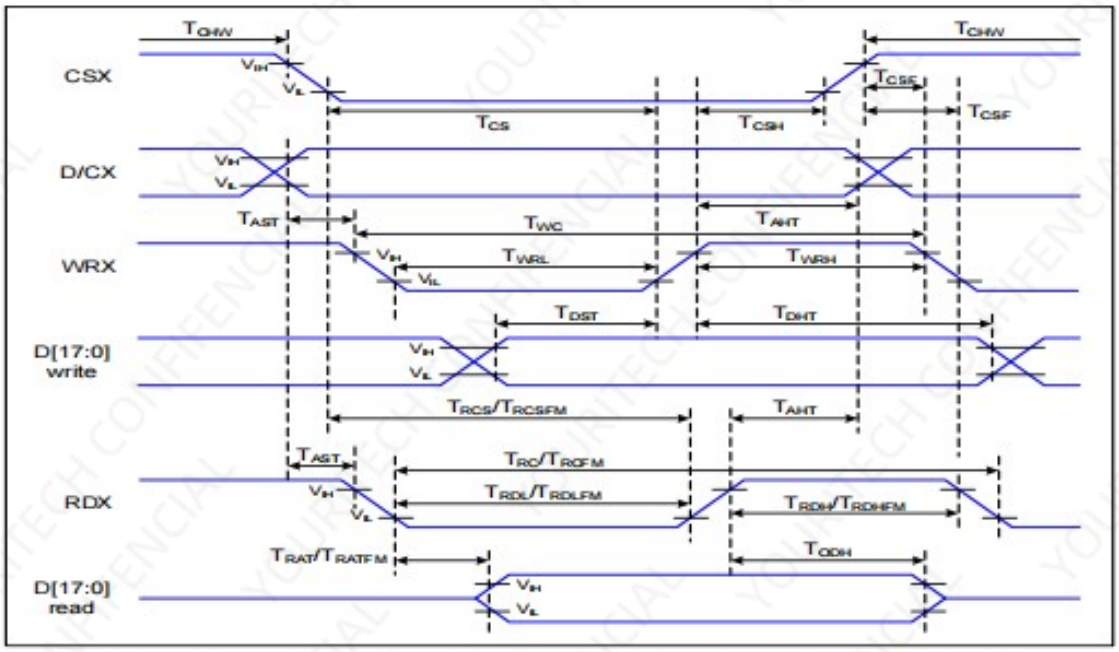


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF

	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Table 4 8080 Parallel Interface Characteristics

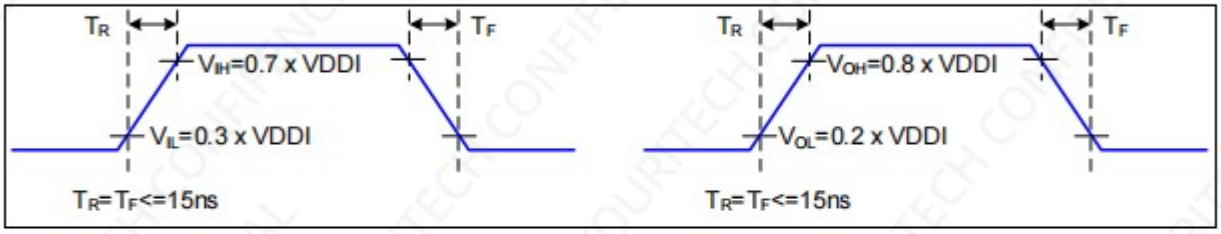


Figure 2 Rising and Falling Timing for I/O Signal

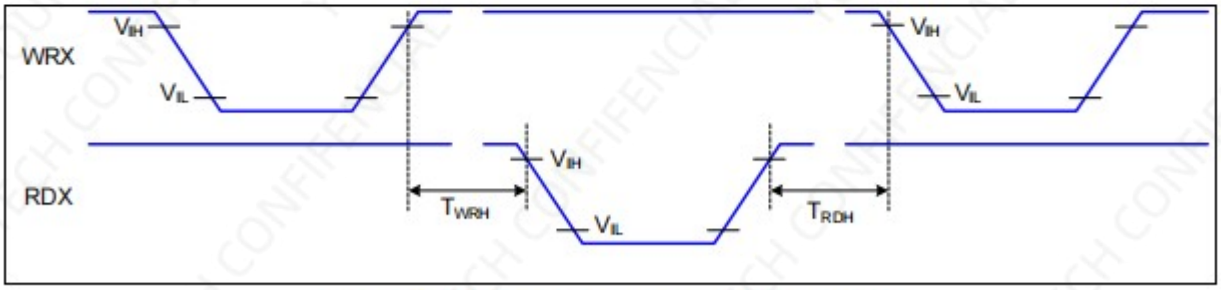


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Serial Interface Characteristics (3-line serial):

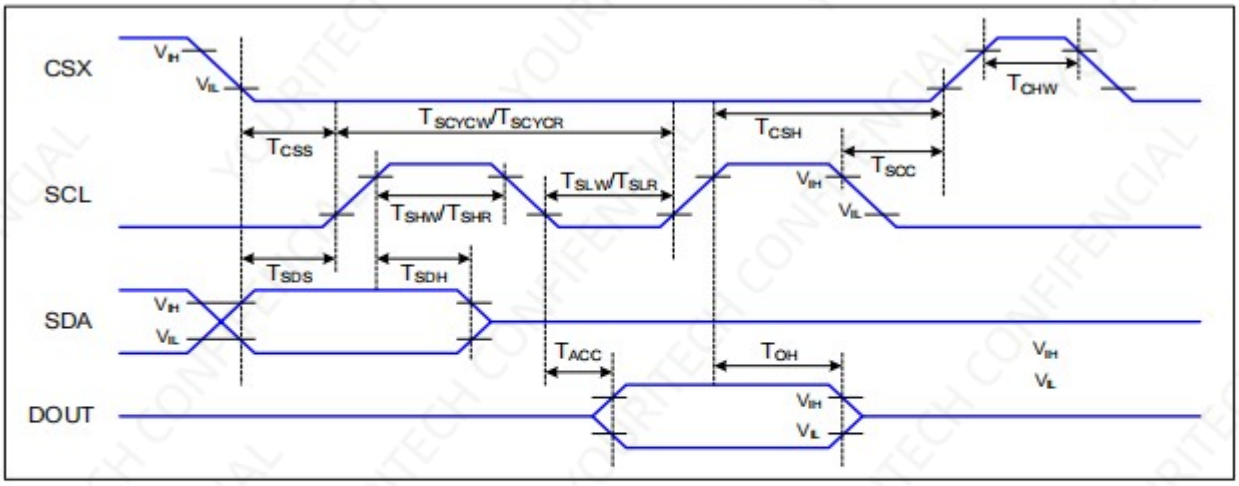


Figure 4 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	
	T_{SHW}	SCL "H" pulse width (Write)	7		ns	
	T_{SLW}	SCL "L" pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note1 : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

Note2: In the read sequence of serial interface, the 500nsec delay time is needed between read command and first read clock..

Serial Interface Characteristics (4-line serial):

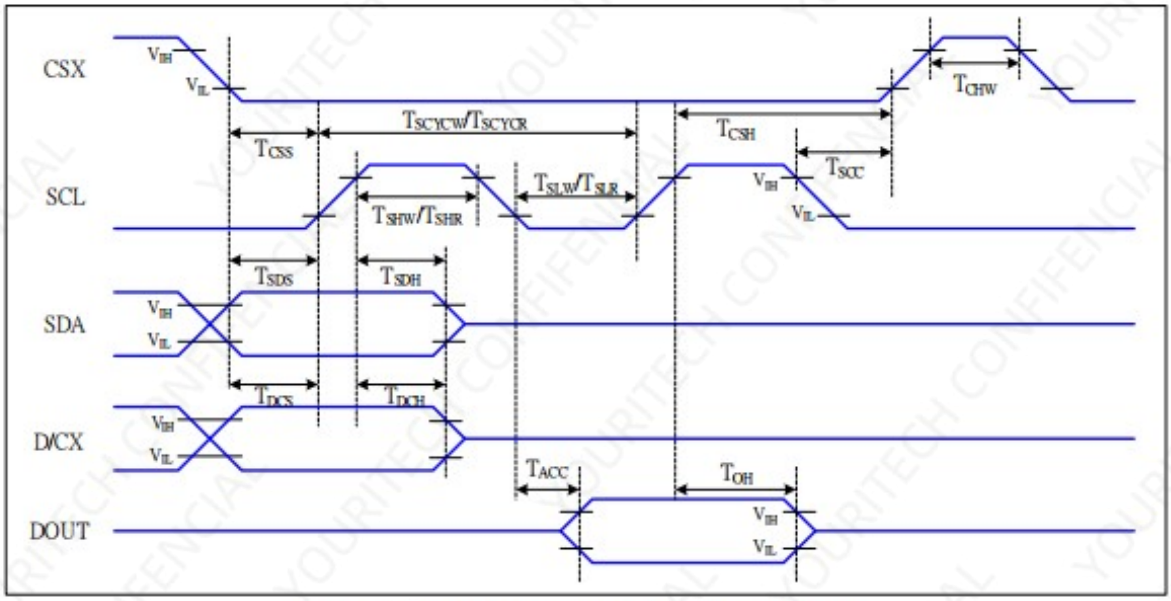


Figure 5 4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	7		ns	
	T_{SLW}	SCL "L" pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 6 4-line serial Interface Characteristics

Note1 : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

Note2: In the read sequence of serial interface, the 500nsec delay time is needed between read command and first read clock.

RGB Interface Characteristics:

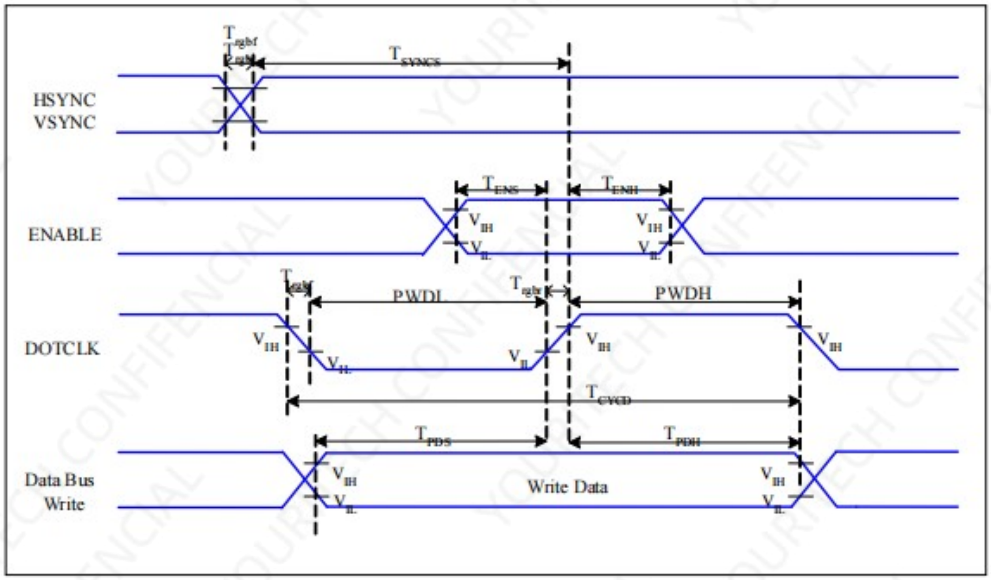


Figure 6 RGB Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

Table 7 18/16 Bits RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	35	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	35	-	ns	
	T_{ENH}	Enable Hold Time	35	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	35	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	35	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	80	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	10	ns	
DB	T_{PDS}	PD Data Setup Time	35	-	ns	
	T_{PDH}	PD Data Hold Time	35	-	ns	

Table 8 6 Bits RGB Interface Timing Characteristics

Reset Timing:

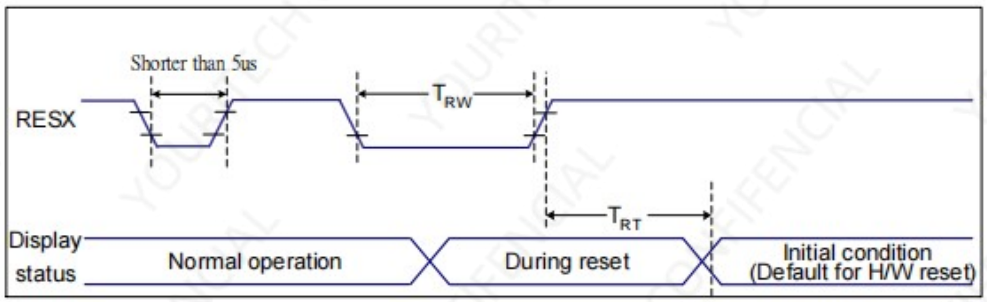


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:

5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

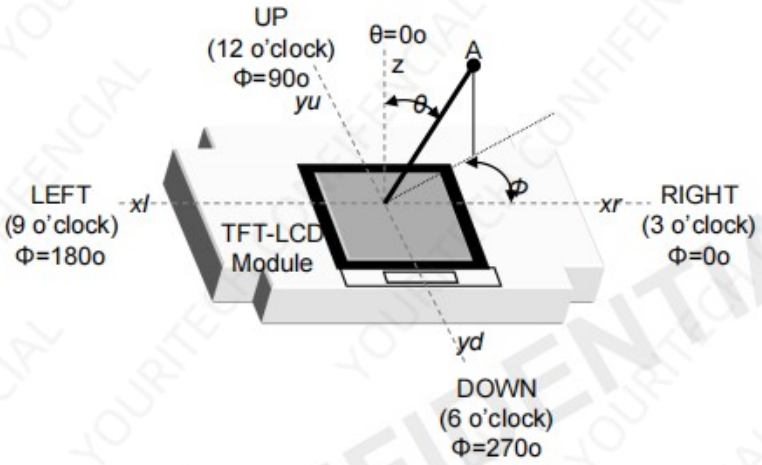
7.Optical Characteristics

<Table 5. Optical Specifications> [Ta=25±2℃]

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	75	80	-	Deg.	Note 4.1
		Θ_9		75	80	-	Deg.	
	Vertical	Θ_{12}		75	80	-	Deg.	
		Θ_6		75	80	-	Deg.	
Contrast Ratio		CR	Θ = 0°	1000	1200	-		APF Note 4.2/4.3
Cell Transmittance		Tr		4.5	4.8	-	%	
Reproduction of color		Rx	Θ = 0°	0.655	0.658	0.661		With BLU @C Light Note 4.4
		Ry		0.335	0.338	0.341		
		Gx		0.259	0.262	0.265		
		Gy		0.597	0.6	0.603		
		Bx		0.131	0.134	0.137		
		By		0.134	0.137	0.14		
		Wx		0.305	0.308	0.311		
		Wy		0.336	0.339	0.342		
Color Gamut			Θ = 0°	65	70	-	%	
Response Time		Ton + Toff	Ta= 25°C Θ = 0°	-	30	35	ms	Note 4.5

Note 1: Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 8).

<Figure 8. Viewing Angle Range Is Defined As Follows>



Note 2: Contrast measurements shall be made at viewing angle of Θ=0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. Luminance Contrast Ratio (CR) is defined mathematically.

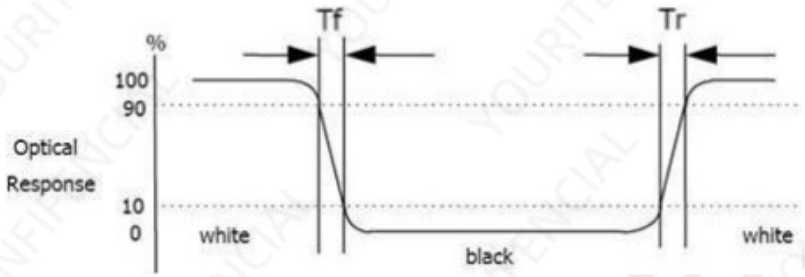
$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 3: Transmittance is the Value with Polarizer.

Note 4: The color chromaticity coordinates specified in Table 16 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

Note 5: The electro-optical response time measurements shall be made as Figure 9 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

<Figure 9. Response Time Testing>



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~60℃（30min），50 cycles	

9. Packing Method----TBD

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