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MODEL NO : ET028QV05-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-12-14

□Preliminary Specification

■Final Product Specification

Customer :_____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 240xRGBx320
As to basic specification of the driver IC, refer to the IC (ST7789T3) specification and data book.
All material & processing of the LCD module should be Lead Free.

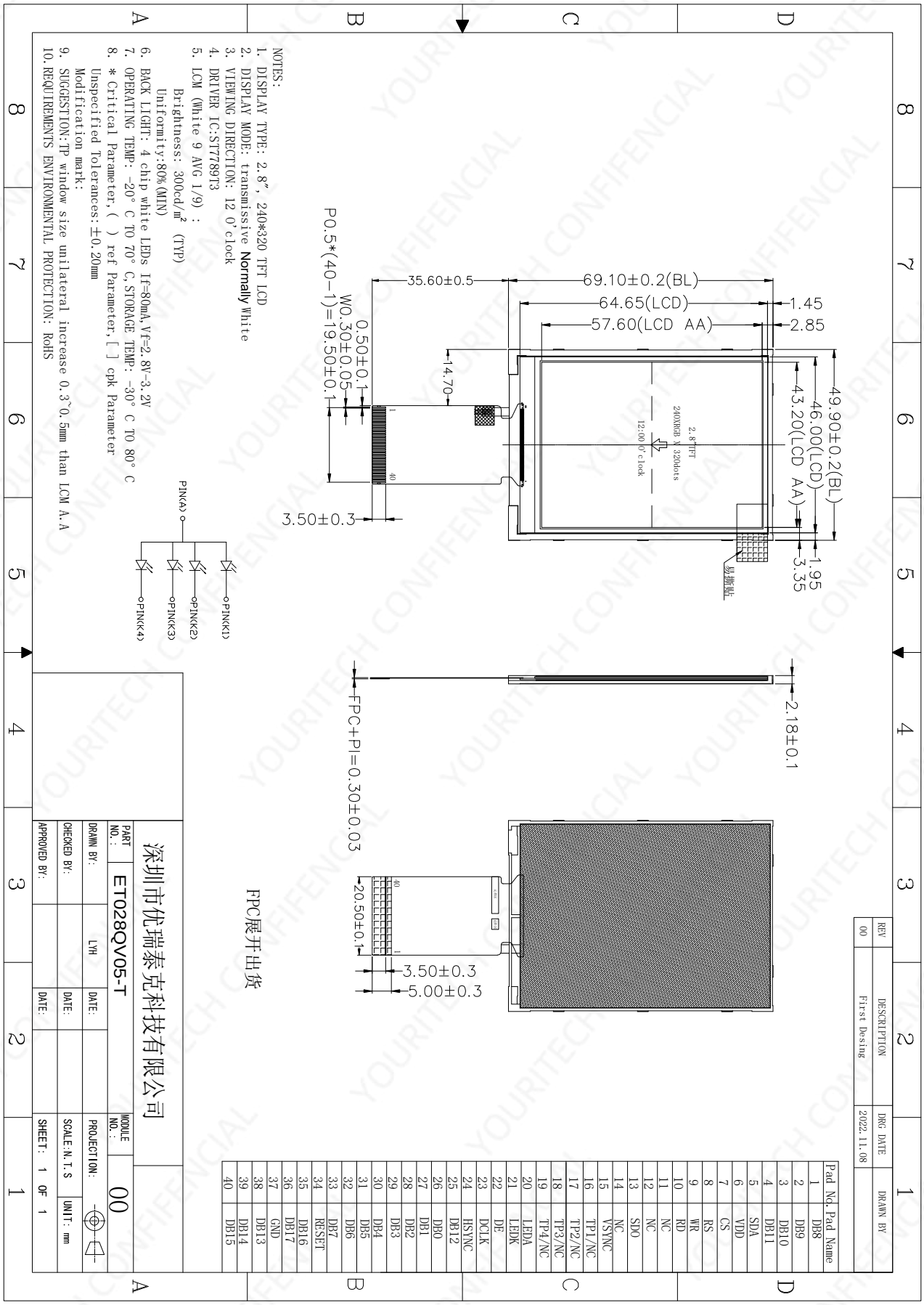
1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;
12 O'CLOCK Type LCD
240 dot-segment and 320 dot-common outputs;
65K/262K Color can be selected by software;
White LED back light;
8line MCU interface

1.3 Applications:

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally White	--
Drive element	TFT active matrix	--
Number of pixels	240*3RGB(H)X320(V)	Dots
Pixel arrangement	RGB Vertical stripe	--
Pixel Pitch (H*V)	0.180(H) x0.180 (V)	mm
Active area	43.20(H) x 57.60(V)	mm
Module Size(W*H*T)	49.90(W)x69.10(H)x2.18(T)	mm
Viewing direction	12 O'CLOCK	-
TFT Driver IC	ST7789T3	-
TFT interface	8Line MCU interface	-
Approx. Weight	TBD	g
Touch structure		
Touch Driver IC		-
Touch Interface		


NOTES:
1. DISPLAY TYPE: 2.8", 240*320 TFT LCD
2. DISPLAY MODE: transmissive Normally White
3. VIEWING DIRECTION: 12 O'clock
4. DRIVER IC:ST7789T3
5. LCM (White 9 AVG 1/9) :
Brightness: 300cd/㎡ (TYP)
Uniformity:80%(MIN)
6. BACK LIGHT: 4 chip white LEDs If=80mA,Vf=2.8V-3.2V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
Unspecified Tolerances:±0.20mm
Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS
PIN(4)
PIN(1)
PIN(2)
PIN(3)
PIN(4)
35.60±0.5
69.10±0.2(BL)
64.65(LCD)
57.60(LCD AA)
1.45
2.85
14.70
0.50±0.1
W0.30±0.05
P0.5*(40-1)=19.50±0.1
49.90±0.2(BL)
46.00(LCD)
43.20(LCD AA)
1.95
3.35
2.8"TFT
240XRGB X 320dots
12:00 O'clock
易撕贴
3.50±0.3
2.18±0.1
FPC+PI=0.30±0.03
20.50±0.1
3.50±0.3
5.00±0.3
FPC展开出货
REV
DESCRIPTION
DRG DATE
DRAWN BY
00
First Desing
2022.11.08
Pad No.
Pad Name
1 DB8
2 DB9
3 DB10
4 DB11
5 SDA
6 VDD
7 CS
8 RS
9 WR
10 RD
11 NC
12 NC
13 SDO
14 NC
15 VSYNC
16 TP1/NC
17 TP2/NC
18 TP3/NC
19 TP4/NC
20 LEDA
21 LEDK
22 DE
23 DCLK
24 HSYNC
25 DB12
26 DB0
27 DB1
28 DB2
29 DB3
30 DB4
31 DB5
32 DB6
33 DB7
34 RESET
35 DB16
36 DB17
37 GND
38 DB13
39 DB14
40 DB15
深圳市优瑞泰克科技有限公司
PART NO.: ET028QV05-T
MODULE NO.: 00
DRAWN BY: LYH
DATE:
PROJECTION:
CHECKED BY:
DATE:
SCALE:N.T.S
UNIT: mm
APPROVED BY:
DATE:
SHEET: 1 OF 1

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
Humidity	RH	-	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	--	--	--	V
Supply Voltage for(DC/DC)	VDD	2.5	2.8	3.3	V
Supply Voltage for(DC/DC)	AVDD				V
Supply Voltage for(DC/DC)	AVEE				V

4.2Back-Light Unit Characeristics

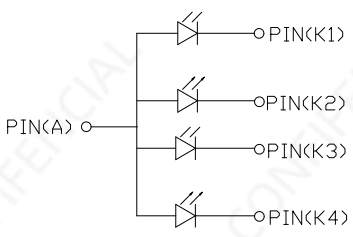
The back-light system is an edge-lighting type with 4 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	2.8	-	3.2	V	-
Forward current	I_F	--	80	-	mA	-
Luminance(With LCD)	Lv		300	--	cd/m^2	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

5.1 LCM Pin Descriptions

Pin No.	Symbol	Functional	Notes
1-4	DB8-DB11	MCU parallel interface data bus.	
5	SDA	SPI interface input pin.	
6	VDD	Power supply 2.5V~3.3V	
7	CS	Chip select signal input pi	
8	RS	Register selection signal.	
9	WR	Write strobe signal.	
10	RD	Read strobe signal.	
11-12	NC	NC	
13	SDO	Serial data output pin.	
14	NC	NC	
15	VS	Vertical (Frame) synchronizing input signal for RGB interface operation.	
16	TP1/NC	NC	
17	TP2/NC	NC	
18	TP3/NC	NC	
19	TP4/NC	NC	
20	LEDA	Power supply for backlight anode input terminal.	
21	LEDK	Power supply for backlight cathode input terminal.	
22	DE	Data enable signal for RGB interface operation.	
23	DOTCLK	Dot clock signal for RGB interface operation.	
24	HS	Horizontal (Line) synchronizing input signal for RGB interface operation.	
25	DB12	MCU parallel interface data bus.	
26-33	DB0-DB7	MCU parallel interface data bus.	
34	RESET	Reset signal input terminal. Active at ‘L’.	
35-36	DB16-DB17	MCU parallel interface data bus.	
37	GND	Ground.	
38-40	DB13-DB15	MCU parallel interface data bus.	

6. Timing Characteristics

VDDI and VDD can be applied in any order.

In CABC function application, VDDI power on need delay 5ms after VDD has been supplied.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

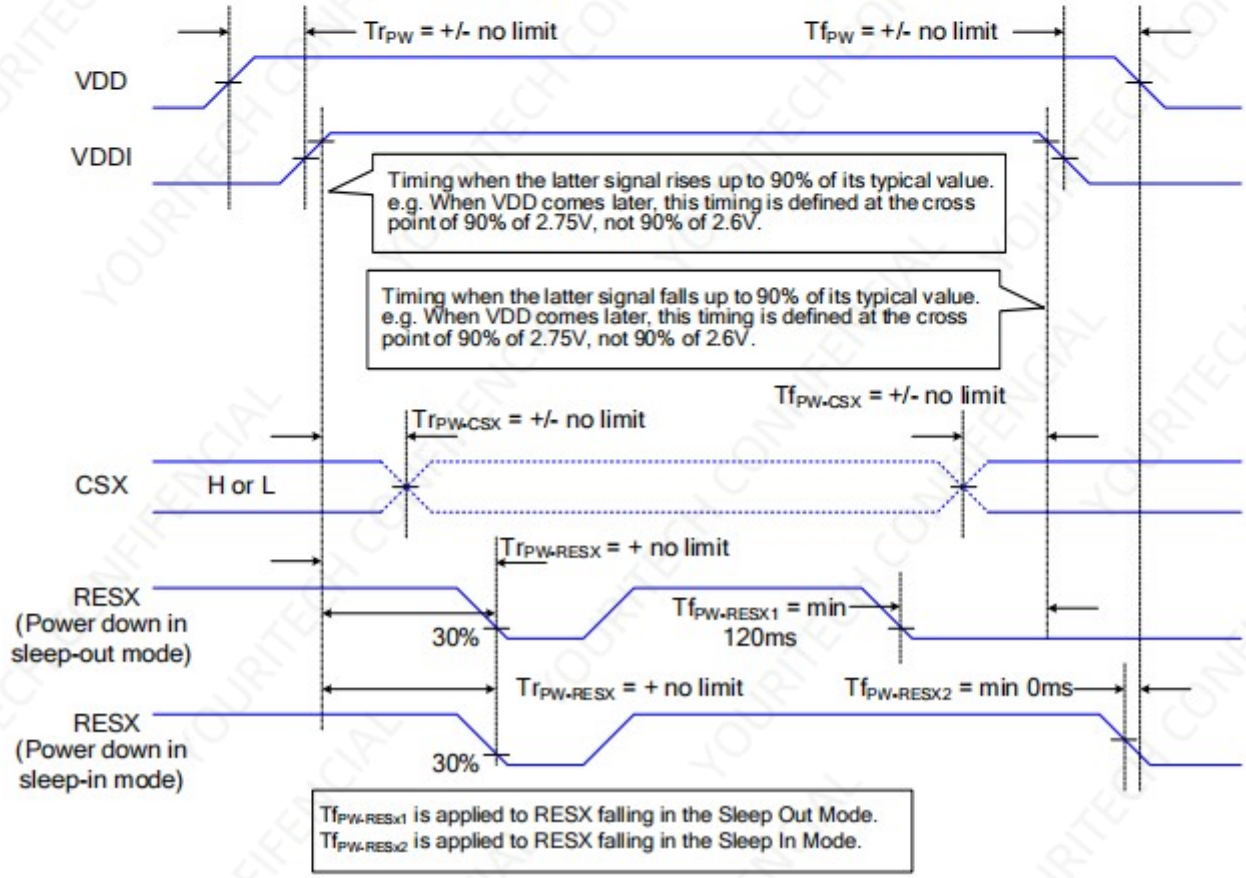
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

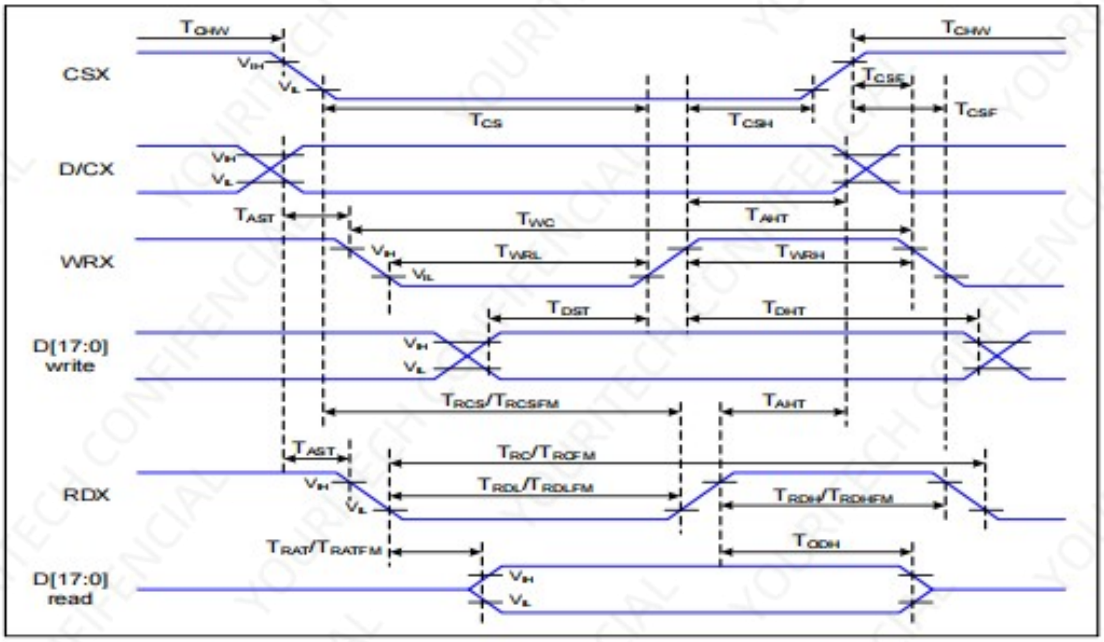


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF

Reset Timing:

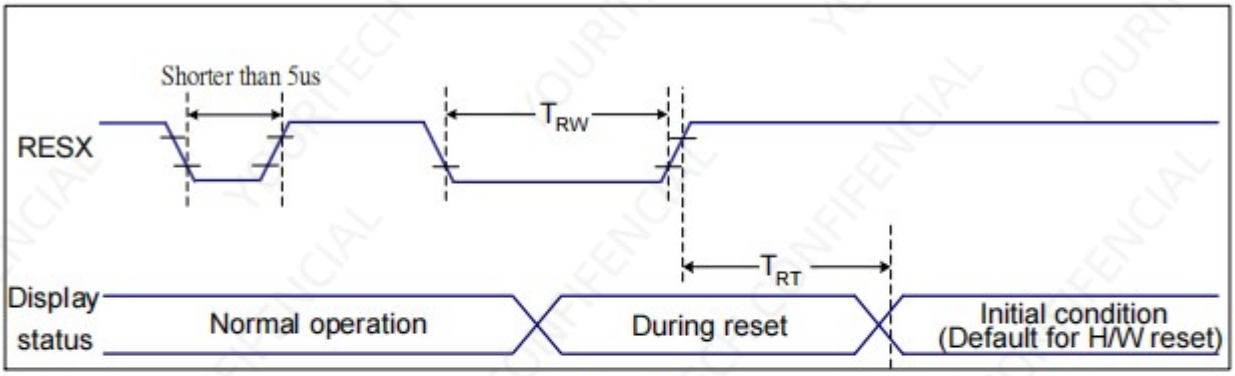


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:

7.Optical Characteristics

Item	Symbol	Condition	Specification			Unit	Remark
			Min.	Typ.	Max.		
Response time (By Quick)	Tr+Tf	θ= 0°	-	16		ms	Note 5
Contrast ratio	CR	θ= 0°	-	500	-		Note 2,6
Viewing angle	Top	CR≧10	-	70	-	deg.	Note 2,6,7
	Bottom	CR≧10	-	50	-		
	Left	CR≧10	-	70	-		
	Right	CR≧10	-	70	-		
Color chromaticity (CF only with ITO, light source is C light, CIE 1931)	Wx	θ= 0°		0.301			Note 3
	Wy			0.337			
	Rx			0.621			
	Ry			0.332			
	Gx			0.294			
	Gy			0.577			
	Bx			0.141			
	By			0.157			
NTSC			-	55	-	%	Note 3
Transmittance	Trans		-	6.4	-	%	Note 9

Note 1: Ambient temperature = 25°C.

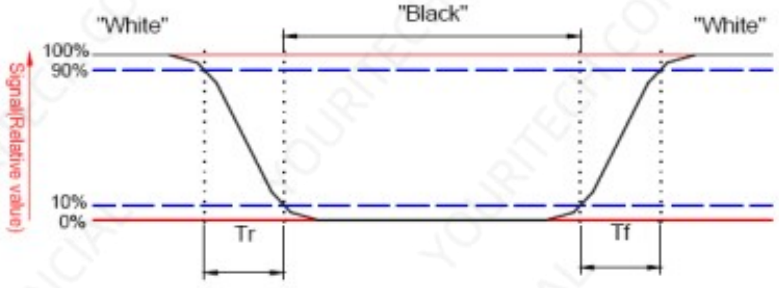
Note 2: To be measured with a viewing cone of 2°by Topcon luminance meter BM-5A.

Note 3: To be measured with Otsuta chromaticity meter LCF-2100M, CF only measure under C light simulation.

Note 4: CTC shipping status is cell without polarizer. Transmittance of Specification is cell with polarizer. The tolerance of Transmittance is ±10%.

Note 5: Definition of response time:

The output signals of TRD-100 are measured when the input signals are changed to "White" (falling time) and from "White" to "Black" (rising time), respectively. The interval is between the 10% and 90% of amplitudes. Refer to figure as below.

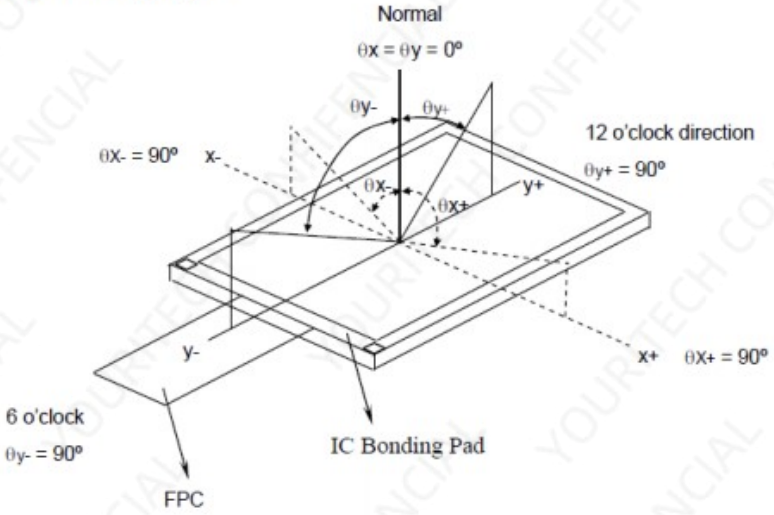


Note 6: Definition of contrast ratio:

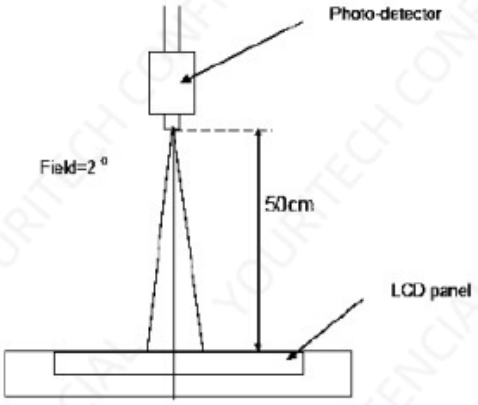
Contrast ratio is calculated by the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "white" state}}{\text{Brightness on the "black" state}}$$

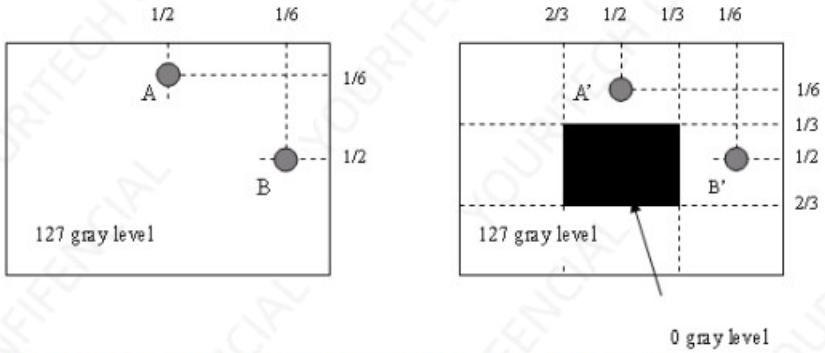
Note 7: Definition of viewing angle



Note 8: Optical characteristic measurement setup.



Note 9:



I LA-LA' I / LA x 100%= 2% max., LA and LA' are brightness at location A and A'.
I LB-LB' I / LB x 100%= 2% max., LB and LB' are brightness at location B and B'.

8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state， -20℃（30min） ~60℃（30min），50 cycles	

9. Packing Method----TBD

- END -