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MODEL NO : ET029HV01-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-06-07

□Preliminary Specification

■Final Product Specification

Customer :_____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 376xRGBx960
As to basic specification of the driver IC, refer to the IC (Sitronix：ST7701SN-G5) specification and data book.
All material & processing of the LCD module should be Lead Free.

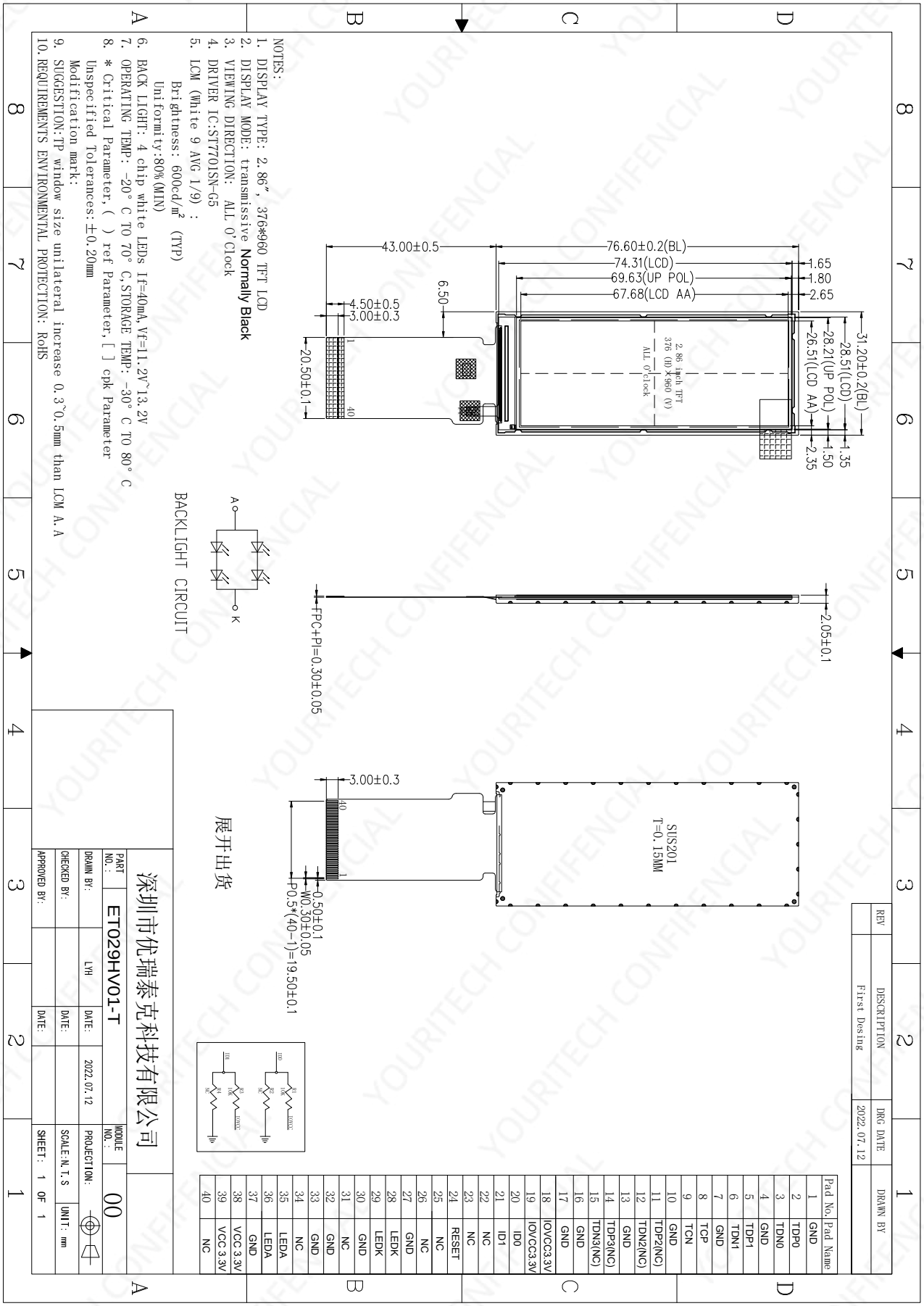
1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;
ALL Viewing Type LCD
376 dot-segment and 960 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
2lane MIPI interface

1.3 Applications:

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	376*3RGB(H)X960(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.0705 (H) x 0.0705 (V)	mm
Active area	26.51(H) x 67.68(V)	mm
Viewing direction	ALL Viewing	-
TFT Driver IC	ST7701SN-G5	
TFT interface	2lane MIPI Interface	-
Approx. Weight	TBD	g
LCM Size(W*H*T)	31.20(W) ×76.60(H) ×2.05(T)	mm
Touch structure	--	
Touch Driver IC	--	-
Touch Interface	--	


NOTES:
1. DISPLAY TYPE: 2.86", 376*960 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL O'Clock
4. DRIVER IC:ST7701SN-G5
5. LCM (White 9 AVG 1/9) :
Brightness: 600cd/m² (TYP)
Uniformity:80%(MIN)
6. BACK LIGHT: 4 chip white LEDs If=40mA, Vf=11.2V~13.2V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
Unspecified Tolerances:±0.20mm
Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS
BACKLIGHT CIRCUIT
展开出货
深圳市优瑞泰克科技有限公司
PART NO.: ET029HV01-T
MODULE NO.: 00
DRAWN BY: LYH
DATE: 2022.07.12
PROJECTION:
CHECKED BY:
DATE:
SCALE:N.T.S
UNIT: mm
APPROVED BY:
DATE:
SHEET: 1 OF 1
REV
DESCRIPTION
First Desing
DRG DATE
2022.07.12
DRAWN BY
Pad No. Pad Name
1 GND
2 TDP0
3 TDN0
4 GND
5 TDP1
6 TDN1
7 GND
8 TCP
9 TCN
10 GND
11 TDP2(NC)
12 TDN2(NC)
13 GND
14 TDP3(NC)
15 TDN3(NC)
16 GND
17 GND
18 IOVCC3.3V
19 IOVCC3.3V
20 ID0
21 ID1
22 NC
23 NC
24 RESET
25 NC
26 NC
27 GND
28 LEDK
29 LEDK
30 GND
31 NC
32 GND
33 GND
34 NC
35 LEDA
36 LEDA
37 GND
38 VCC 3.3V
39 VCC 3.3V
40 NC
43.00±0.5
76.60±0.2(BL)
74.31(LCD)
69.63(UP POL)
67.68(LCD AA)
1.65
1.80
2.65
31.20±0.2(BL)
28.51(LCD)
28.21(UP POL)
26.51(LCD AA)
1.35
1.50
2.35
6.50
4.50±0.5
3.00±0.3
20.50±0.1
2.86 inch TFT
376 (H) X 960 (V)
ALL O'clock
FPC+PI=0.30±0.05
2.05±0.1
SUS201
T=0.15MM
3.00±0.3
0.50±0.1
W0.30±0.05
P0.5*(40-1)=19.50±0.1
A
K

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+60	°C
LCM Storage Temperature	T_{STG}	-30	+70	°C
Humidity	RH	-	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	3.3	3.3	V
Supply Voltage for(DC/DC)	VDD	2.6	3.3	3.3	V
Current Consumption	I_{DD}	--	--	50	mA
	$I_{DD-SLEEP}$	--	--	150	uA

4.2 Back-Light Unit Characeristics

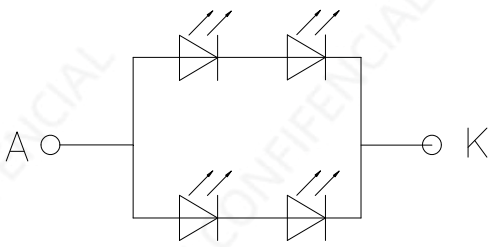
The back-light system is an edge-lighting type with 4 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	11.2		13.2	V	-
Forward current	I_F	--	40	-	mA	-
Luminance(With LCD)	Lv		600		cd/m^2	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	LCM Functional	Notes
1	GND	Power Ground	
2	MIPI_0P	Positive polarity of low voltage differential data 3 signa	
3	MIPI_0N	Negative polarity of low voltage differential data 3 signal	
4	GND	Power Ground	
5	MIPI_1P	Positive polarity of low voltage differential data 3 signa	
6	MIPI_1N	Negative polarity of low voltage differential data 3 signal	
7	GND	Power Ground	
8	CLKP	Positive polarity of low voltage differential clock signal	
9	CLKN	Negative polarity of low voltage differential clock signal	
10	GND	Power Ground	
11	MIPI_2P(NC)	NC	
12	MIPI_2N(NC)	NC	
13	GND	Power Ground	
14	MIPI_3P(NC)	NC	
15	MIPI_3N(NC)	NC	
16~17	GND	Power Ground	
18~19	IOVCC3.3V	Power supply I/O : 1.65V ~ 3.3V	
20~21	ID0~ID1	The MCU interface mode select	
22~23	NC	NC	
24	RESET	Reset signal input terminal. Active at ‘L’.	
25~26	NC	NC	
27	GND	Power Ground	
28~29	LEDK	Power supply for backlight cathode input terminal.	
30	GND	Power Ground	
31	NC	NC	
32~33	GND	Power Ground	
34	NC	NC	
35~36	LEDA	Power supply for backlight anode input terminal.	
37	GND	Power Ground	
38~39	VCC 3.3V	Power Supply For LCD.	
40	NC	NC	

6. Timing Characteristics

POWER ON/OFF SEQUENCE

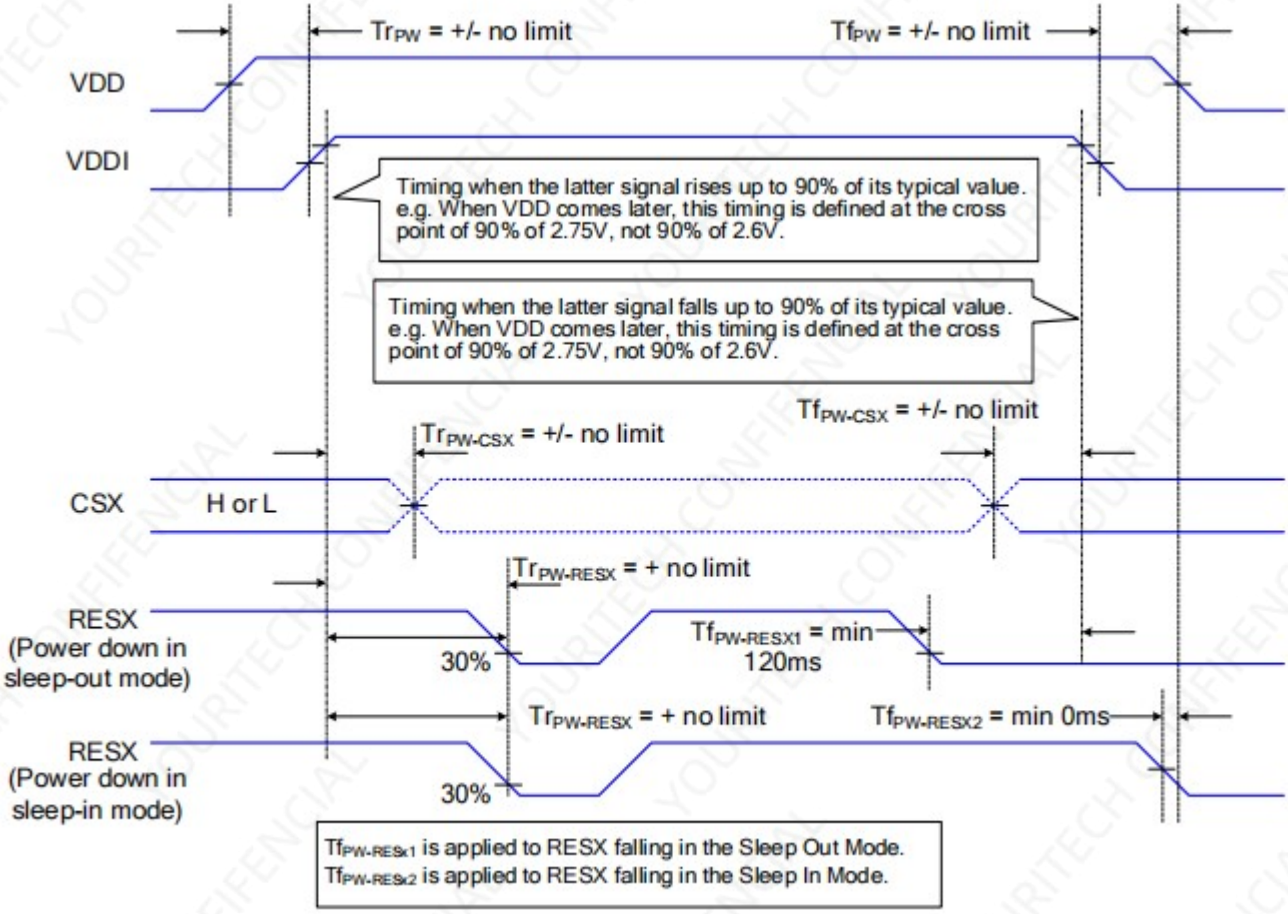
VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released.

CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

Notes:

1. There will be no damage to the ST7701S if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

The power on/off sequence is illustrated below



DSI-MIPI Interface Timing Characteristics of IC

High Speed Mode

DSI clock channel timing

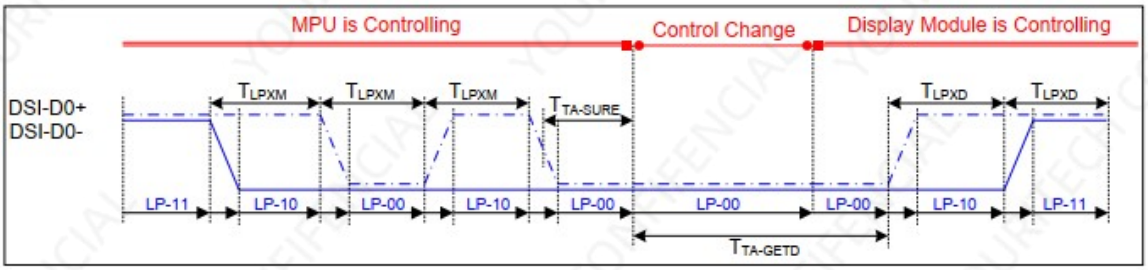
Rising and falling time on clock and data channel

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

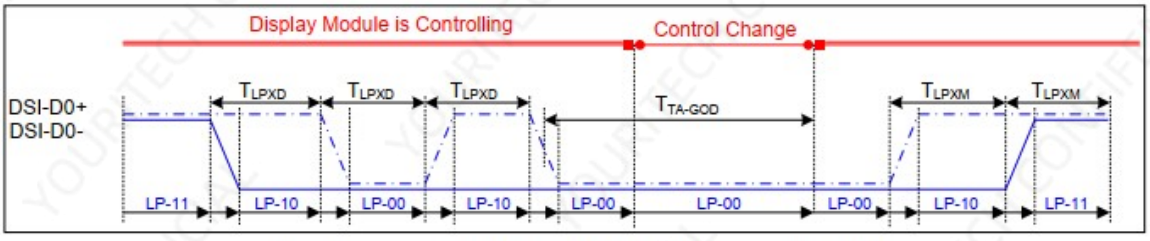
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	12.5	ns	UI = UI_{INSTA}= UI_{INSTB}
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Mipi Interface- High Speed Mode Timing Characteristics

Lowe Power Mode



Bus Turnaround (BTA) from display module to MPU Timing



Bus Turnaround (BTA) from MPU to display module Timing

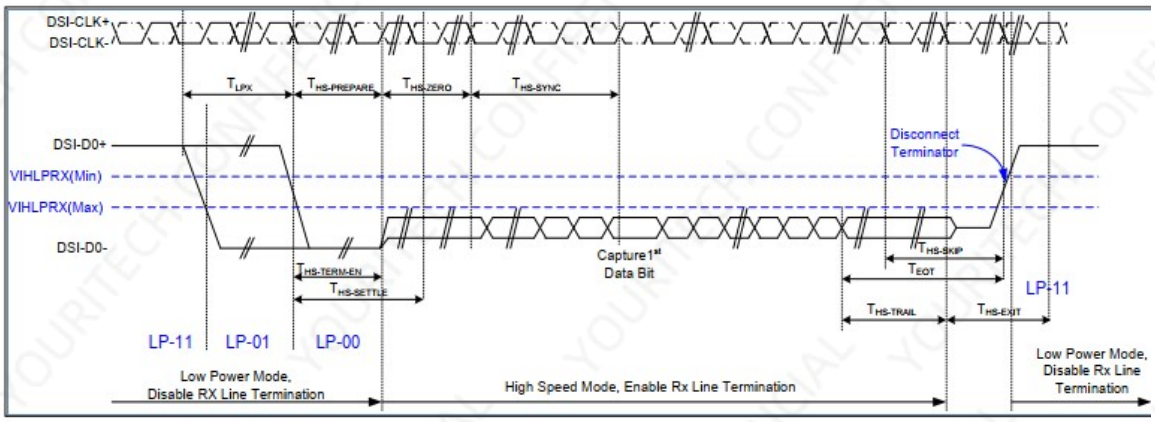
VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

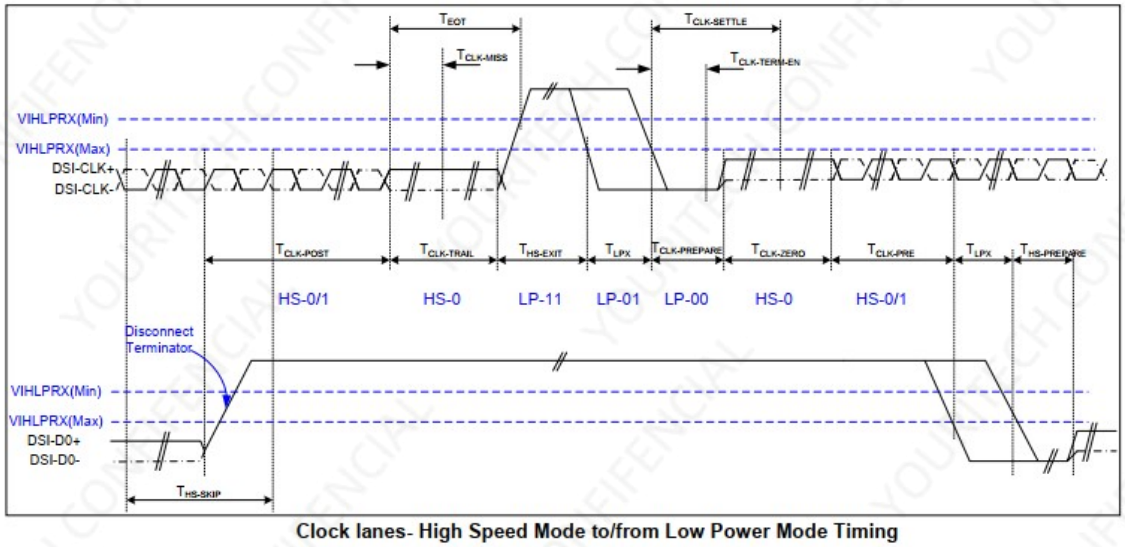
Mipi Interface Low Power Mode Timing Characteristics

DSI Bursts Mode

DSI Bursts Mode



Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

Reset Description:

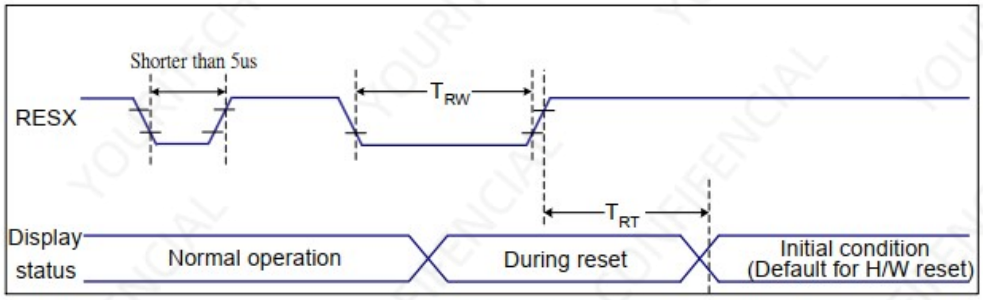


Figure 9 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

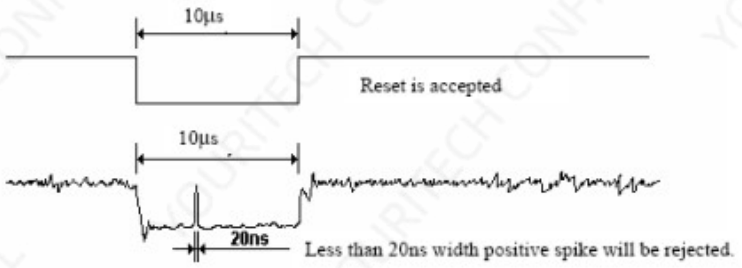
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

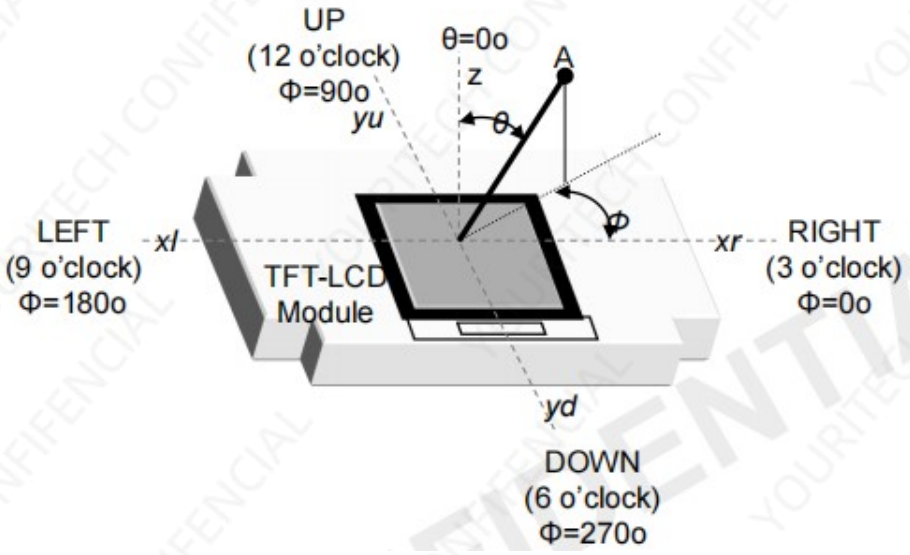
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	75	85	-	Deg.	Note 4.1
		Θ_9		75	85	-	Deg.	
	Vertical	Θ_{12}		75	85	-	Deg.	
		Θ_6		75	85	-	Deg.	
Contrast Ratio		CR	Θ = 0°	1000	1500	-		Without APF Note 4.2/4.3
Cell Transmittance		Tr		3.0	3.5	-	%	
Reproduction of color		Rx	Θ = 0°	0.589	0.619	0.649	-	@C Light Note 4.4
		Ry		0.302	0.332	0.362	-	
		Gx		0.273	0.303	0.333	-	
		Gy		0.533	0.563	0.593	-	
		Bx		0.105	0.135	0.165	-	
		By		0.104	0.134	0.164	-	
		Wx		0.288	0.318	0.348	-	
		Wy		0.310	0.340	0.370	-	
Color Gamut			Θ = 0°	50	55.1	-	%	
Response Time		Tr	Ta= 25°C Θ = 0°	-	-	-	ms	Note 4.5
		Tf		-	-	-	ms	
		Tr+Tf		-	30	35	ms	

Note 4.1: Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 6).

<Figure 6. Viewing Angle Range Is Defined As Follows>



Note 4.2: Contrast measurements shall be made at viewing angle of Θ=0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. Luminance Contrast Ratio (CR) is defined mathematically.

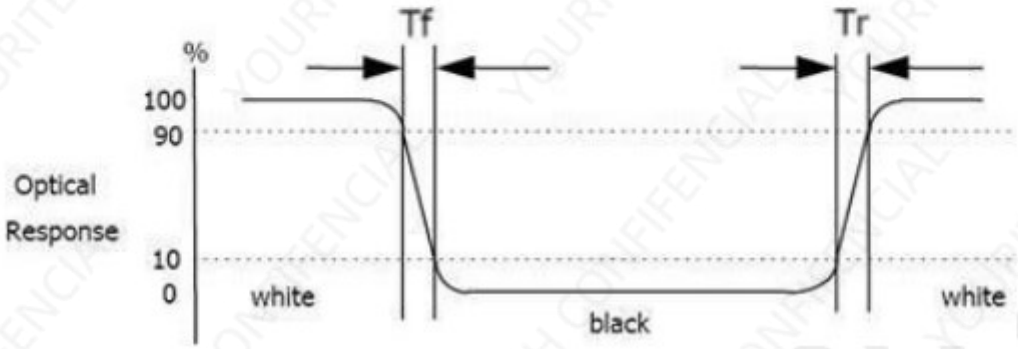
$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 4.3: Transmittance is the Value with Polarizer.

Note 4.4: The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

Note 4.5: The electro-optical response time measurements shall be made as Figure 7. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

<Figure 7. Response Time Testing>



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+70°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+60°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state， -20℃（30min） ~60℃（30min），50 cycles	

9. Packing Method----TBD

- END -