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Custom Display

PCAP

Mechanical design

Production Custom designs Installation



MODEL NO : ET032QV03-TT

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2023-01-02

☐ Preliminary Specification

☒ Final Product Specification

Customer : _____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

This specification applies to the LCD module that is supplied by Tian Xian Wei Technology CO., LTD.

LCD specification: Dots 240xRGBx320.

As to basic specification of the driver IC, refer to the IC (Sitronix:ILI9341V) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL+RTP;

12 O'clock Type LCD

240dot-segment and 320 dot-common outputs;

65/262K Color can be selected by software;

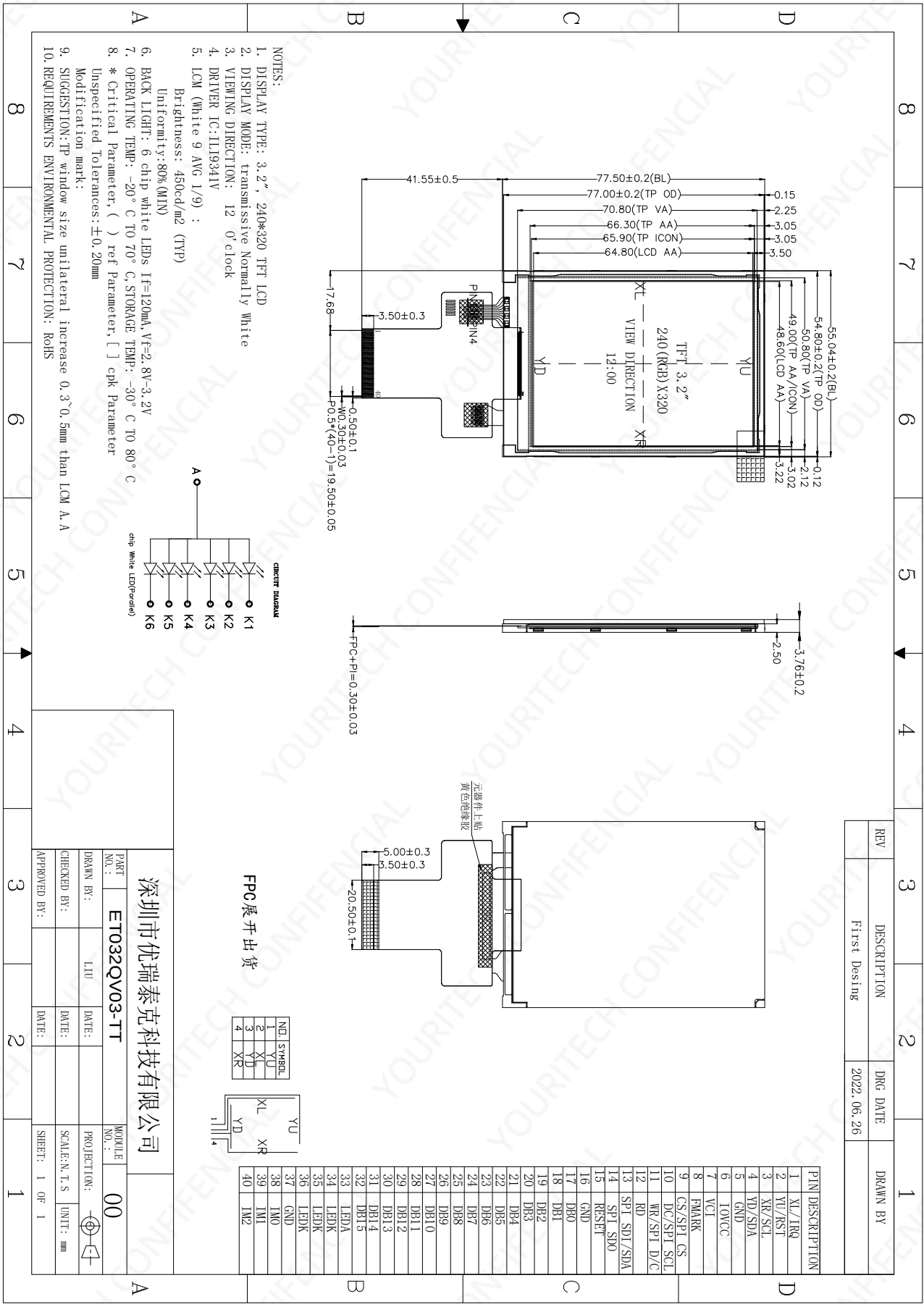
White LED back light;

16bit MCU+4lane SPI interface

1.3 Applications:

2. LCM General specification

ITEM	Standard value	Unit
LCD Type	Normally White	--
Drive element	TFT active matrix	--
Number of pixels	240*3RGB(H)X320(V)	Dots
Pixel arrangement	RGB Vertical stripe	--
Pixel Pitch (W*H)	0.2025(H) x 0.2025(V)	mm
Active area	48.60(W) × 64.80(H)	mm
Viewing direction	12 O'CLOCK	--
TFT Driver IC	ILI9341V	--
TFT interface	16bit MCU+4lane SPI interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	55.04 (W) ×77.50(H) ×2.50(T)	mm
LCM+TP Size(W*H*T)	54.80 (W) ×77.00(H) ×3.76(T)	mm
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--



3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T _{OPR}	-20	+70	°C
LCM Storage Temperature	T _{STG}	-30	+80	°C
TP Operating Temperature & Humidity(20% ~ 90%RH)	T _{OPR}	-20	+70	°C
TP SStorage Temperature & Humidity(20% ~ 90%RH)	T _{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.6	2.8	3.3	V
Current Consumption	I _{DD}	--	--	--	mA
	I _{DD-SLEEP}	--	--	--	uA

4.2 Back-Light Unit Characeristics

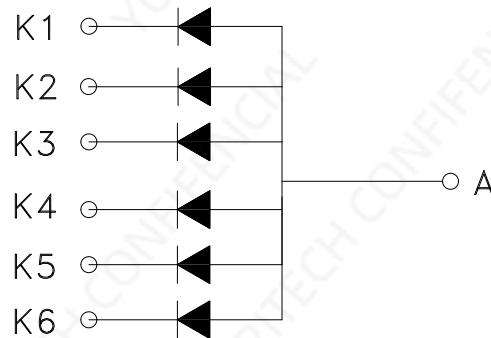
The back-light system is an edge-lighting type with 6 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V _F	2.8	--	3.2	V	--
Forward current	I _F	--	120	--	mA	--
Luminance(With LCD+RTP)	L _v	--	450	--	cd/m ²	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

- (1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED.
The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



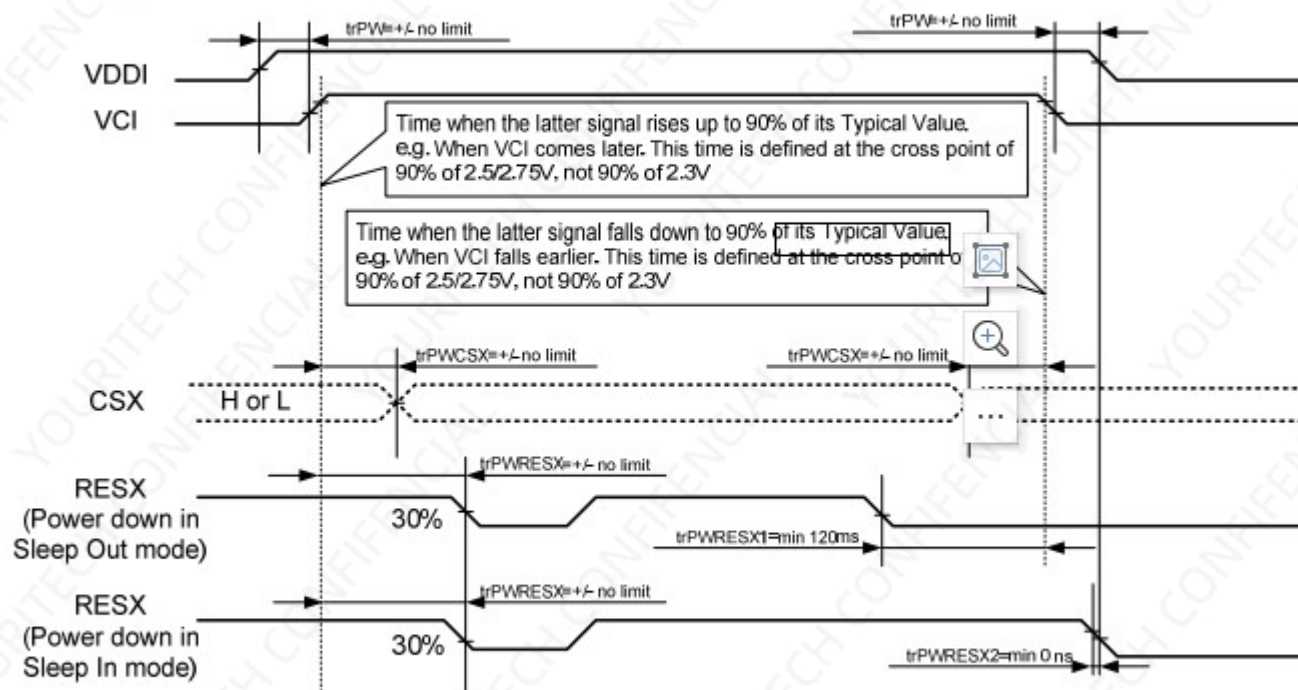
5. Module Function Description

Pin No.	Symbol	Functional	Notes																																										
1	XL/IRQ	Touch panel coordinate in the Left																																											
2	YU/RST	Touch panel coordinate in the Up																																											
3	XR/SCL	Touch panel coordinate in the Right																																											
4	YD/SDA	Touch panel coordinate in the Down																																											
5	GND	Ground.																																											
6	IOVCC	Power Supply For I/O.																																											
7	VCI	Power Supply For LCD.																																											
8	FMARK	Tearing effect signal is used to synchronize MCU to frame memory																																											
9	CS/SPI-CS	Chip select signal input pin																																											
10	DC/SPI-SCL	Register selection signal.																																											
11	WR/SPI-D/C	Write strobe signal.																																											
12	RD	Read strobe signal.																																											
13	SPI-SDI/SDA	Serial data input pin.																																											
14	SPI-SDO	Serial data output pin.																																											
15	RESET	Reset signal input terminal. Active at ‘L’ .																																											
16	GND	Ground.																																											
17-32	DB0-DB15	MCU parallel interface data bus.																																											
33	LEDA	Power supply for backlight anode input terminal.																																											
34-36	LEDK	Power supply for backlight cathode input terminal.																																											
37	GND	Ground.																																											
38-40	IM0-IM2	<table><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>80 MCU 16-bit bus interface II</td><td>D[8:1]</td><td>D[17:10], D[8:1]</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>80 MCU 8-bit bus interface II</td><td>D[17:10]</td><td>D[17:10]</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 MCU 18-bit bus interface II</td><td>D[8:1]</td><td>D[17:0]</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80 MCU 9-bit bus interface II</td><td>D[17:10]</td><td>D[17:9]</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface II</td><td colspan="2">SDI: In SDO: Out</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface II</td><td colspan="2">SDI: In SDO: Out</td></tr></table>	1	0	0	0	80 MCU 16-bit bus interface II	D[8:1]	D[17:10], D[8:1]	1	0	0	1	80 MCU 8-bit bus interface II	D[17:10]	D[17:10]	1	0	1	0	80 MCU 18-bit bus interface II	D[8:1]	D[17:0]	1	0	1	1	80 MCU 9-bit bus interface II	D[17:10]	D[17:9]	1	1	0	1	3-wire 9-bit data serial interface II	SDI: In SDO: Out		1	1	1	0	4-wire 8-bit data serial interface II	SDI: In SDO: Out		
		1	0	0	0	80 MCU 16-bit bus interface II	D[8:1]	D[17:10], D[8:1]																																					
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		1	1	1	0	4-wire 8-bit data serial interface II	SDI: In SDO: Out																																						

6. Timing Characteristics

Case 1 – RESX line is held High or Unstable by Host at Power ON

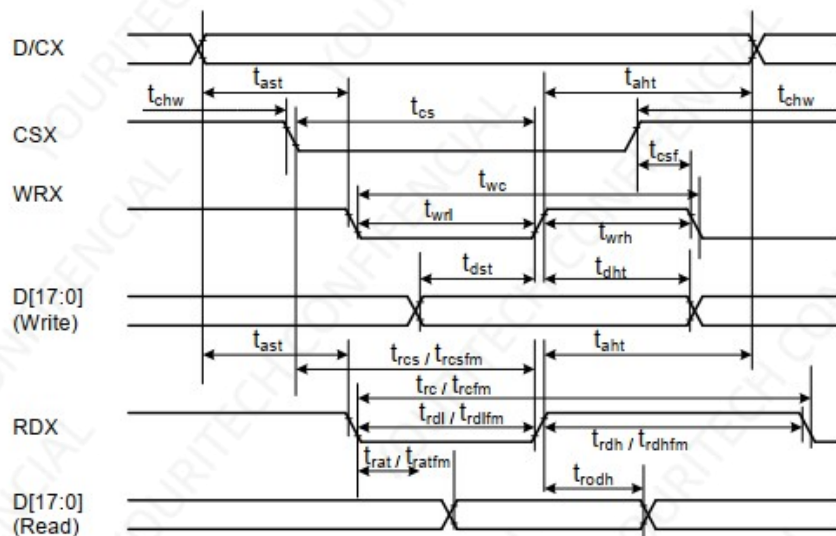
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



$trPWRESX1$ is applied to RESX falling in the Sleep Out Mode
 $trPWRESX2$ is applied to RESX falling in the Sleep In Mode

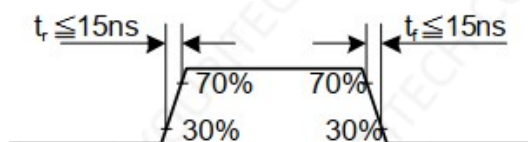
Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

80 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus



Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t _{ast}	Address setup time	0	-	ns	
	t _{ah}	Address hold time (Write/Read)	0	-	ns	
CSX	t _{chw}	CSX "H" pulse width	0	-	ns	
	t _{cs}	Chip Select setup time (Write)	15	-	ns	
	t _{rcs}	Chip Select setup time (Read ID)	45	-	ns	
	t _{rcsfm}	Chip Select setup time (Read FM)	355	-	ns	
	t _{csf}	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	t _{wc}	Write cycle	66	-	ns	
	t _{wrh}	Write Control pulse H duration	15	-	ns	
	t _{wrl}	Write Control pulse L duration	15	-	ns	
RDX (FM)	t _{rcfm}	Read Cycle (FM)	450	-	ns	
	t _{rdhfm}	Read Control H duration (FM)	90	-	ns	
	t _{rdlfm}	Read Control L duration (FM)	355	-	ns	
RDX (ID)	t _{rc}	Read cycle (ID)	160	-	ns	
	t _{rdh}	Read Control pulse H duration	90	-	ns	
	t _{rdl}	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	t _{dst}	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t _{dht}	Write data hold time	10	-	ns	
	t _{rat}	Read access time	-	40	ns	
	t _{ratfm}	Read access time	-	340	ns	
	t _{rodh}	Read output disable time	20	80	ns	

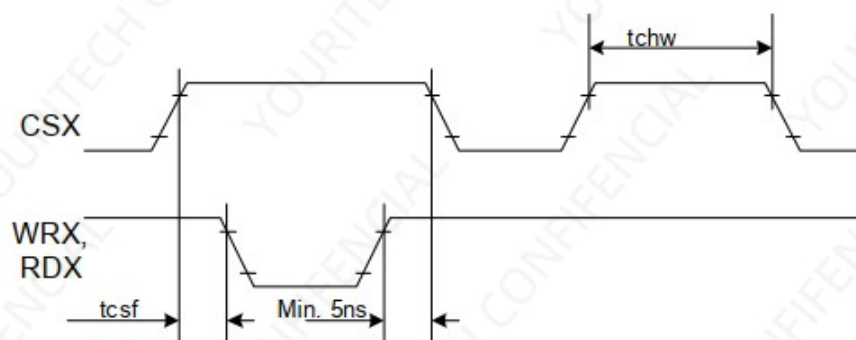
Note: T_a = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V



T _{DHT}	Data hold time	10		ns
T _{RAT}	Read access time (ID)		40	ns
T _{RATFM}	Read access time (FM)		340	ns
T _{ODH}	Output disable time	20	80	ns

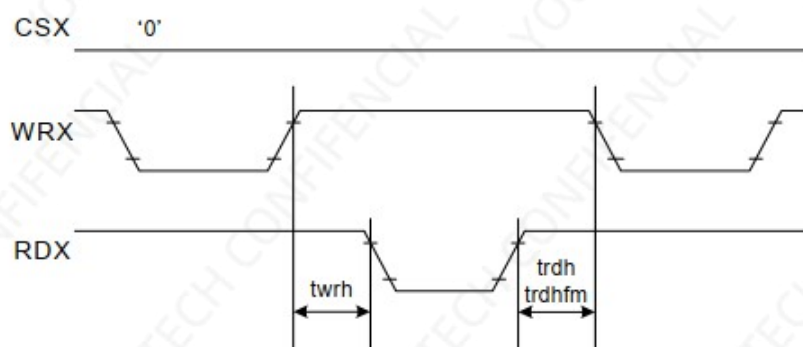
Table 4 8080 Parallel Interface Characteristics

CSX timings :



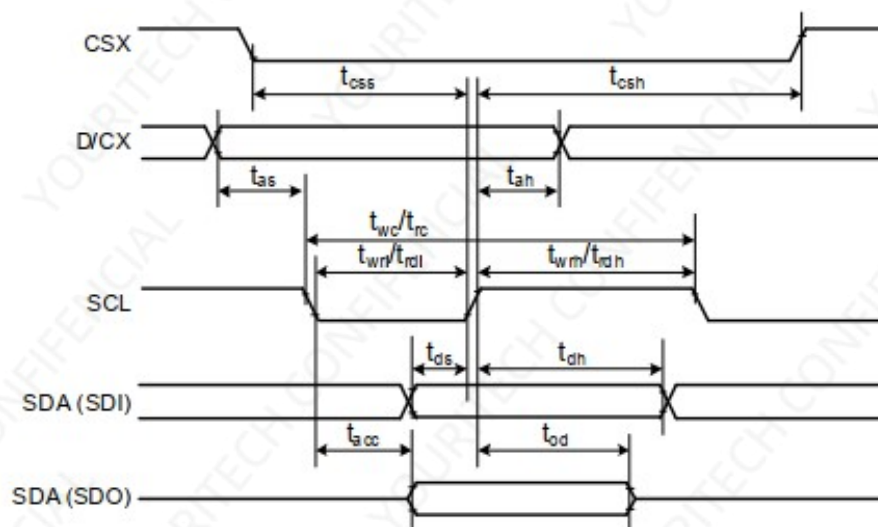
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



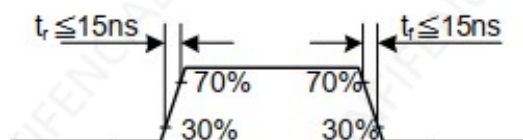
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Display Serial Interface Timing Characteristics (4-line SPI system):

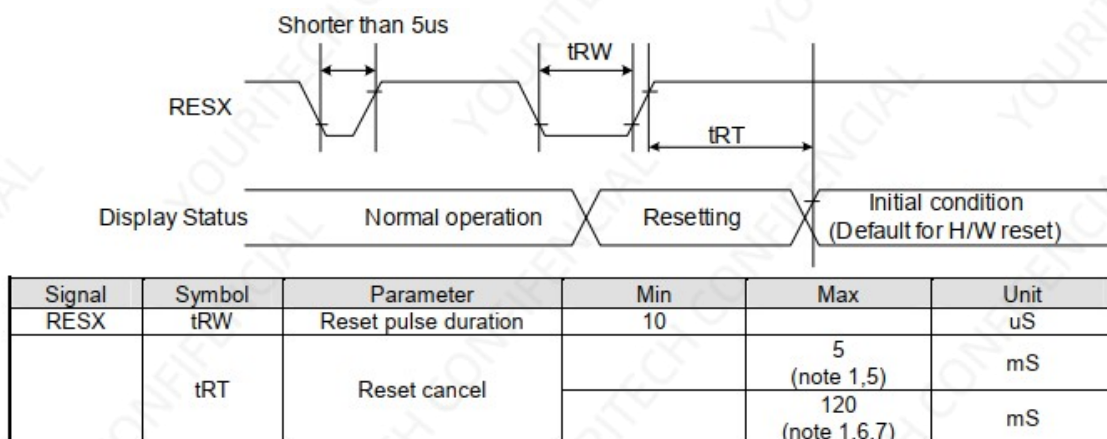


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL "H" pulse width (Write)	40	-	ns	
	twrl	SCL "L" pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: $T_a = 25^\circ\text{C}$, $V_{DDI}=1.65\text{V to }3.3\text{V}$, $V_{CI}=2.5\text{V to }3.3\text{V}$, $AGND=VSS=0\text{V}$



Reset Timing:



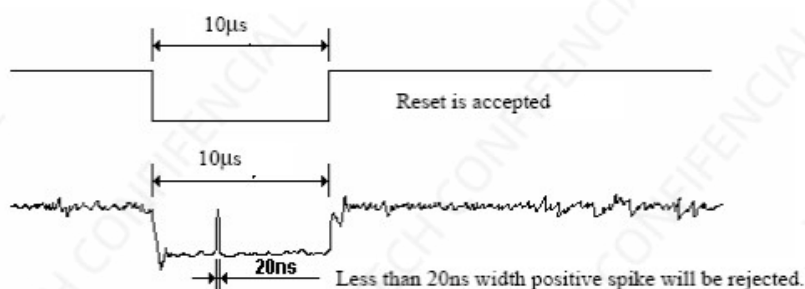
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. Optical Characteristics

1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Transmittance (without Polarizer)		T(%)	—	—	18.0	—	—		
Contrast Ratio		CR	$\Theta = 0$	400	500	—	—	(1)(2)	
Response time	Rising	T _R	Normal viewing angle	—	4	8	msec	(1)(3)	
	Falling	T _F		—	—	12			24
				—					
Color gamut		S(%)			60		%		
Color chromaticity (CIE1931)	White	W _x		0.283	0.303	0.323		(1)(4) CF glass (C-light)	
		W _y		0.305	0.325	0.345			
	Red	R _x		0.606	0.626	0.646			
		R _y		0.314	0.334	0.354			
	Green	G _x		0.257	0.277	0.297			
		G _y		0.529	0.549	0.569			
	Blue	B _x		0.122	0.142	0.162			
		B _y		0.102	0.122	0.142			
Viewing angle	Hor.	Θ _L	CR>10	35	45	—			
		Θ _R		35	45	—			
	Ver.	Θ _U		35	50	—			
		Θ _D		10	20	—			
View Direction		12 O'clock						(5)	

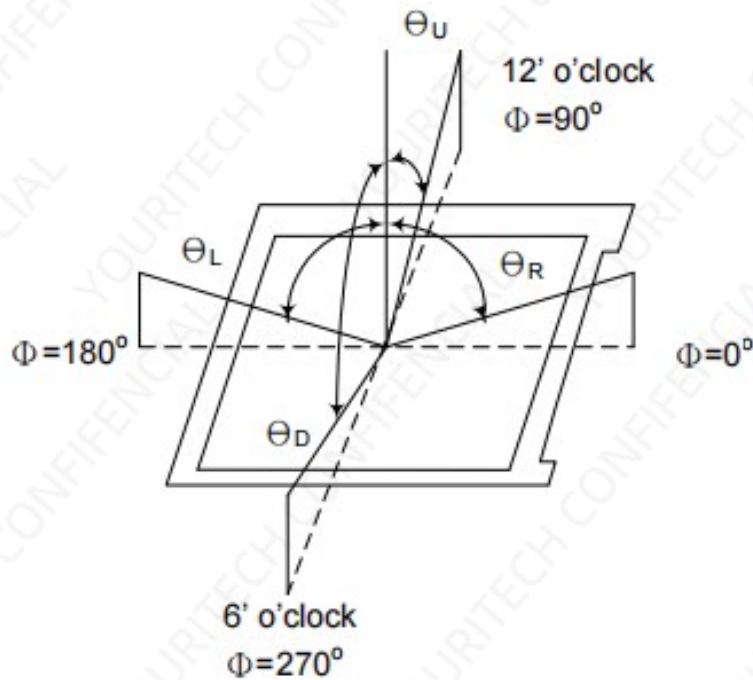
2 Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : $25 \pm 2^\circ\text{C}$
- 15min. warm-up time.

3 Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

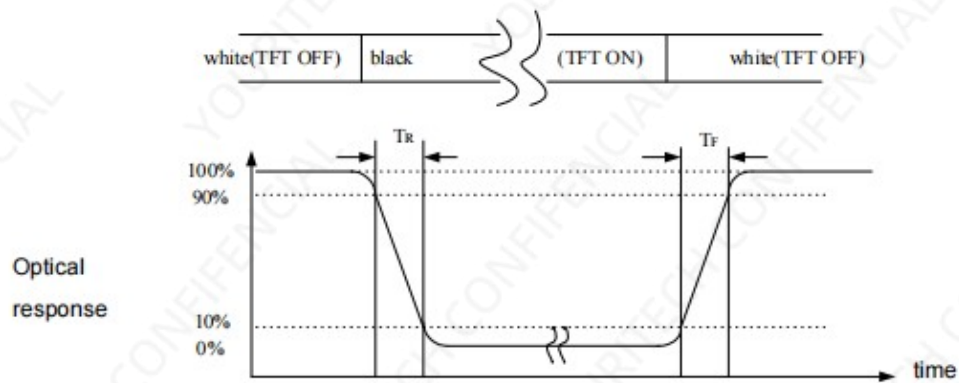
Note (1) Definition of Viewing Angle :



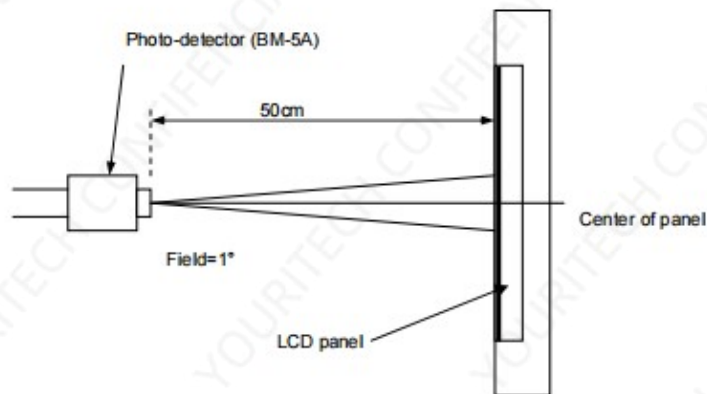
Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

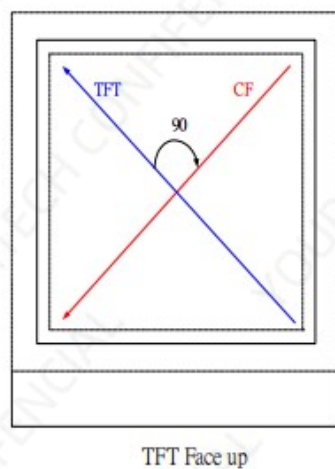
Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different view direction.)



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test is OK. Missing Segment, short, unclear segment non-display, display abnormally and liquid crystal leakage un-allowed. 2. No low temperature bubbles, end seal loose and fall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Temp. Operating	+70°C / 96H	
4	Low Temp. Operating	-20°C / 96H	
5	High Temperature / Humidity storage	50°C x 90%RH / 96H	
6	Thermal and cold shock	Static state, -20°C (30min) ~60°C (30min), 50 cycles	

9. Packing Method----TBD

- END -