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MODEL NO : ET034FD01-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-12-13

□Preliminary Specification

■Final Product Specification

Customer :_____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 800xRGBx800.
As to basic specification of the driver IC, refer to the IC (JD9365DA) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

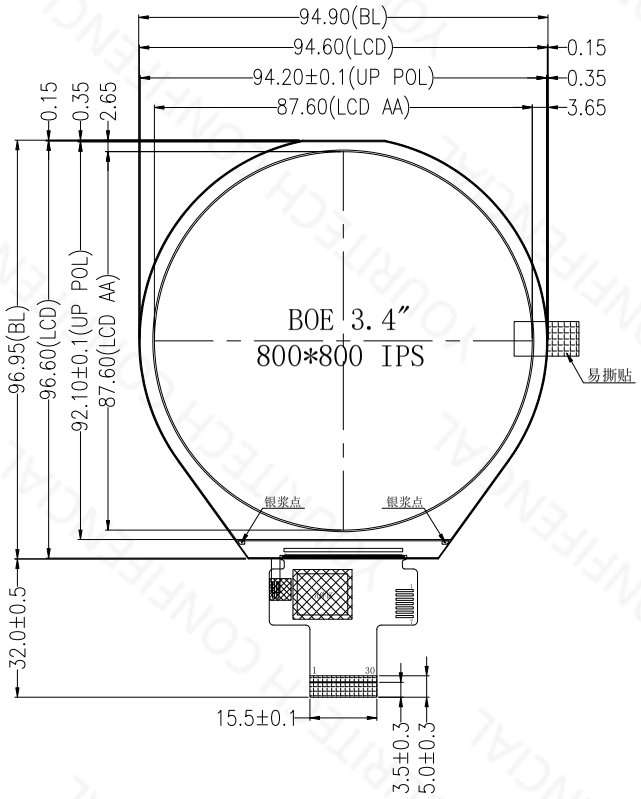
Structure: TFT PANNEL+IC +FPC+BL;
IPS Type LCD
800 dot-segment and 800 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
4Lane MIPI interface

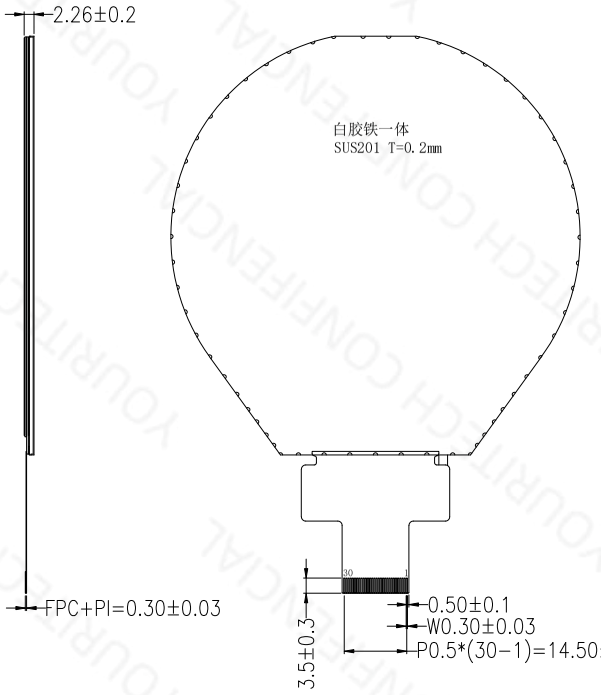
1.3 Applications:

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally black	--
Drive element	TFT active matrix	--
Number of pixels	800*3RGB(H)X800(V)	Dots
Pixel arrangement	RGB Vertical stripe	--
Pixel Pitch (W*H)	0.1095(H) x0.1095 (V)	mm
Active area	87.60(H) x 87.60(V)	mm
Viewing direction	ALL O'CLOCK	mm
TFT Driver IC	JD9365DA	--
TFT interface	4Lane MIPI interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	94.90(W)x 96.95(H) x 2.26(T)	mm
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--

REV	DESCRIPTION	DRG DATE	DRAWN BY
	First Desing	2022.08.26	

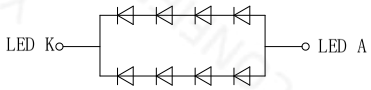




NO.	SYMBOL
1	LEDA
2	LEDK1
3	LEDK2
4	VCI
5	IOVCC
6	RESET
7	TE
8	PWM
9	GND
10	DOP
11	DON
12	GND
13	D1P
14	D1N
15	GND
16	CLKP
17	CLKN
18	GND
19	D2P
20	D2N
21	GND
22	D3P
23	D3N
24	GND
25	TP_INT
26	TP_SDA
27	TP_SCL
28	TP_RESET
29	TP_VCI
30	GND

PIN	TP定义
1	GND
2	INT
3	SDA
4	SCL
5	RST
6	VCI
7	GND

NOTES:
1. DISPLAY TYPE: 3.4″, 800*800 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL
4. DRIVER IC:JD9365DA
5. LCM (White 9 AVG 1/9) :
   Brightness: 500cd/m² (TYP)
   Uniformity:80%(MIN)
6. BACK LIGHT:8 chip white LEDs If=40mA,Vf=22V-26.4V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS



VF=24V (22V-26.4V)
IF=40MA

FPC展开出货

深圳市优瑞泰克科技有限公司

PART NO.:	ET034FD01-T	MODULE NO.:	00
DRAWN BY:	LYH	DATE:	PROJECTION:
CHECKED BY:		DATE:	SCALE:N.T.S UNIT: mm
APPROVED BY:		DATE:	SHEET: 1 OF 1

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	℃
LCM Storage Temperature	T_{STG}	-30	+80	℃
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.5	3.3	3.3	V
Supply Voltage for(DC/DC)	VSP	--	--	--	V
Supply Voltage for(DC/DC)	VSN	--	--	--	V

4.2 Back-Light Unit Characeristics

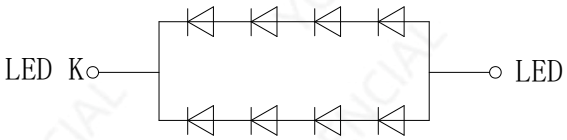
The back-light system is an edge-lighting type with 8 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	22	--	26.4	V	--
Forward current	I_F	--	40	--	mA	--
Luminance(With LCD)	Lv	--	500	--	cd/m^2	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

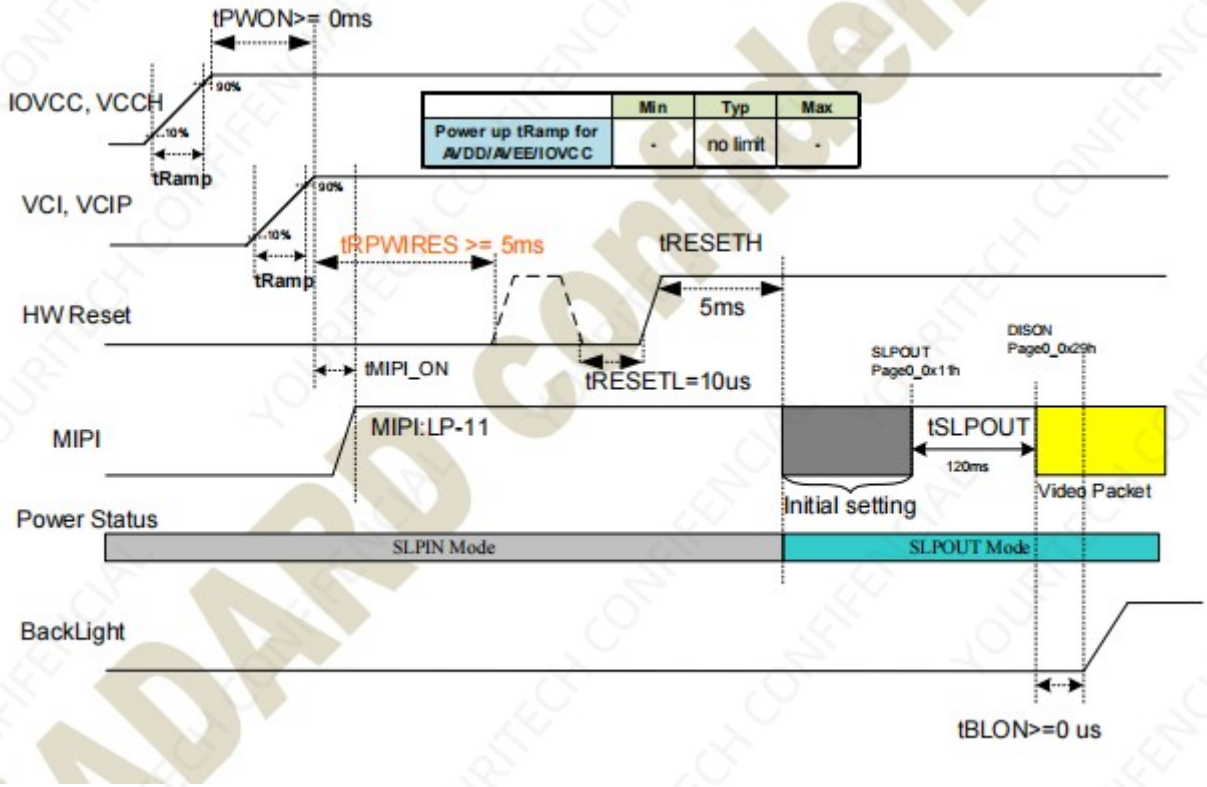
Pin No.	Symbol	LCM Functional	Notes
1	LEDA	Power supply for backlight anode input terminal.	
2	LEDK1	Power supply for backlight cathode input terminal.	
3	LEDK2	Power supply for backlight cathode input terminal.	
4	VCI	Power Supply For LCD.	
5	IOVDD	Power Supply For I/O.	
6	RESET	Reset Signal input pin.	
7	TE	Tearing effect output pin.	
8	PWM	PWM (Pulse Width Modulation) Signal Of LED Driving.	
9	GND	Power Ground	
10	MIPI_D0P	MIPI-DSI Data differential signal input pins	
11	MIPI_D0N	MIPI-DSI Data differential signal input pins	
12	GND	Power Ground	
13	MIPI_D1P	MIPI-DSI Data differential signal input pins	
14	MIPI_D1N	MIPI-DSI Data differential signal input pins	
15	GND	Power Ground	
16	MIPI_CKP	MIPI-DSI CLOCK differential signal input pins	
17	MIPI_CKN	MIPI-DSI CLOCK differential signal input pins	
18	GND	Power Ground	
19	MIPI_D2P	MIPI-DSI Data differential signal input pins	
20	MIPI_D2N	MIPI-DSI Data differential signal input pins	
21	GND	Power Ground	
22	MIPI_D3P	MIPI-DSI Data differential signal input pins	
23	MIPI_D3N	MIPI-DSI Data differential signal input pins	
24	GND	Power Ground	
25	CTP_INT	Touch panel interrupt output	
26	CTP_SDA	Touch panel I2C data	
27	CTP_SCL	Touch panel I2C clock	
28	CTP_RESET	Touch panel reset	
29	CTP_VCI	Touch panel Power supply 2.8~3.3V	
30	GND	Power Ground	

6. Timing Characteristics

Power on sequence for differential power mode

Symbol	Min	Typ	Max	Unit	Remark
tRamp	-	no limit	-	us	
tPWON	0	-	-	ms	
tON1	0	-	-	ms	
tMIPI-ON	0	-	tRPWIRES	ms	
tRPWIRES	5	-	-	ms	
tRESETL	10	-	-	us	
tRESETH	5	-	-	ms	
tSLPOUT	120	-	-	ms	
tBLON	0	-	-	ms	

BOOSTM[1:0]=10 (Internal DC/DC power mode : Charge Pump, FP7721)
VCCD=IOVCC=VCCH=1.65V ~ 3.6V, VCI=VCIP=2.5V ~ 4.8V.
Power on:



High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 13.5.

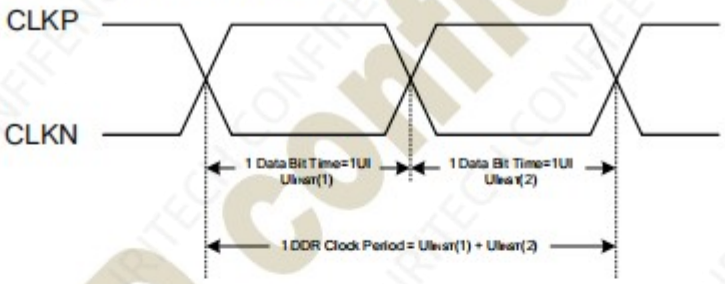


Figure 11.5: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

Burst Mode Data Transmission

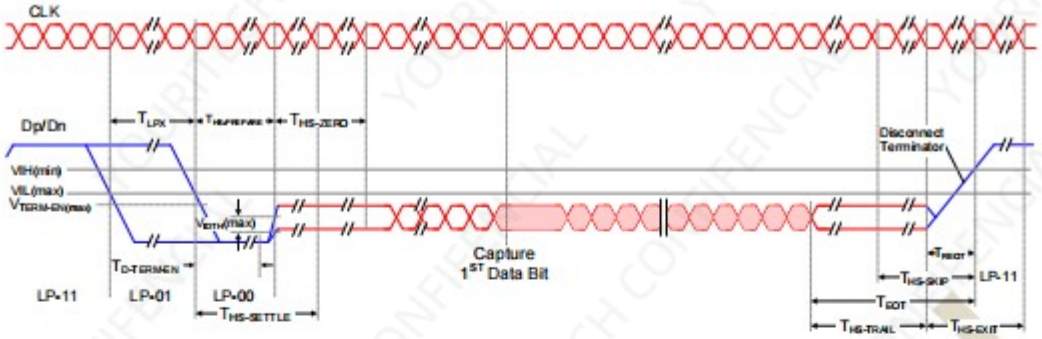


Figure 11.7: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 + n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

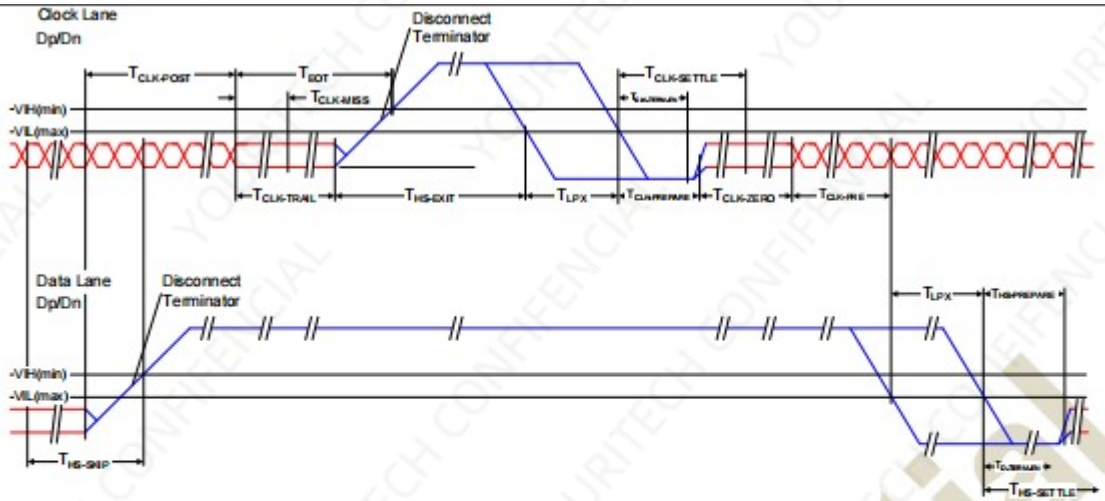


Figure 11.8: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

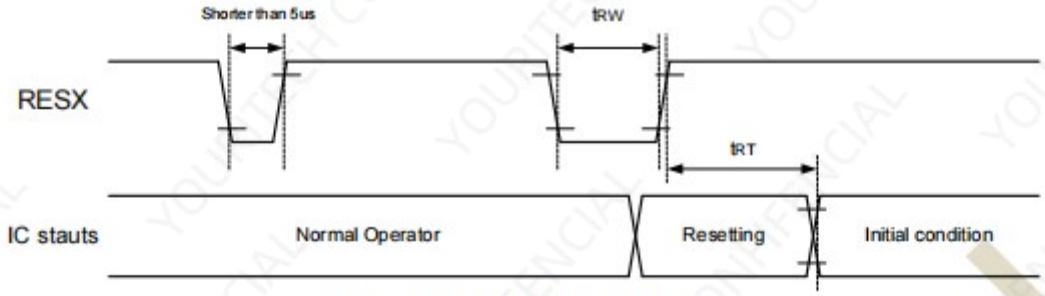


Figure 11.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width(2)	RESX	10	-	µs
t_{RT}	Reset complete time(3)	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

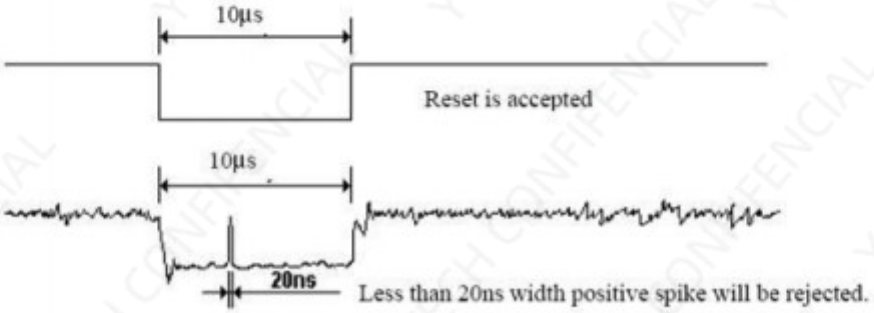
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

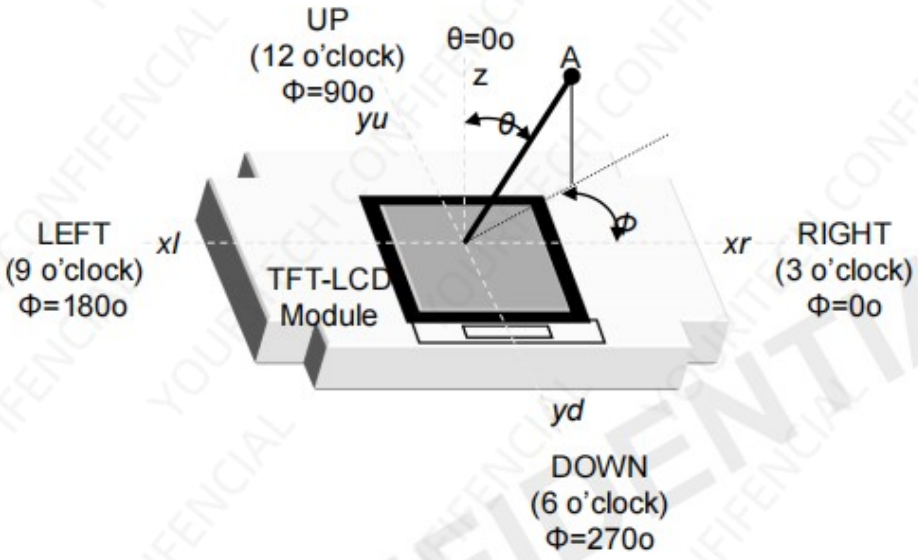
7.Optical Characteristics

<Table 5. Optical Specifications> [Ta=25±2℃]

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	Note 4.1
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Contrast Ratio		CR	Θ = 0°	1000	1200	-		HC+APF & Silicate BLU With B-ITO Note 4.2/4.3
Cell Transmittance		Tr		4.7	5.5	-	%	
Reproduction of color		Rx	Θ = 0°	0.637	0.667	0.697	-	CF @C Light Note 4.4
		Ry		0.293	0.323	0.353	-	
		Gx		0.241	0.271	0.301	-	
		Gy		0.561	0.591	0.621	-	
		Bx		0.104	0.134	0.164	-	
		By		0.091	0.121	0.151	-	
		Wx		0.262	0.292	0.322	-	
		Wy		0.303	0.333	0.363	-	
Color Gamut			Θ = 0°	65	70	-	%	
Response Time		Tr+Tf	Ta= 25°C Θ = 0°	-	30	35	ms	Note 4.5

Note 5.1: Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 5).

<Figure 5. Viewing Angle Range Is Defined As Follows>



Note 5.2: Contrast measurements shall be made at viewing angle of Θ=0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 5.3: Transmittance is the Value with Polarizer(HC+APF) & silicate BLU (Film structure is on Table 6) .

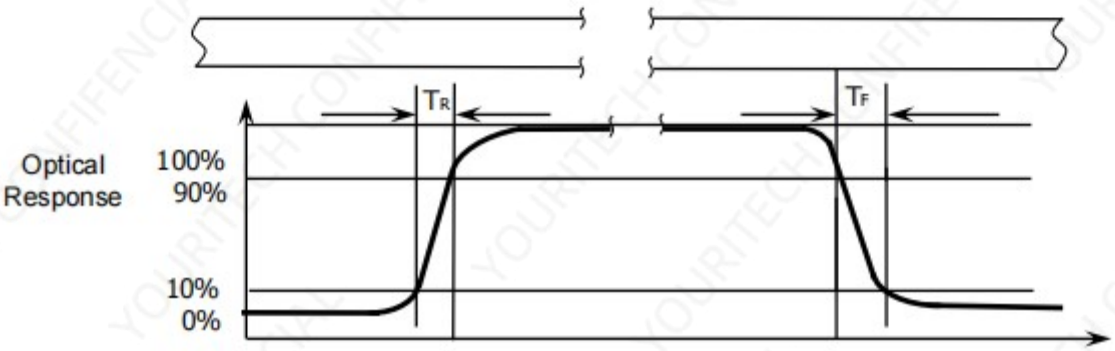
<Table 6. BLU Film structure >

资材	型号	备注
遮光	SK8906B	-
BEF	SG43+QG42	上+下棱镜
DIF	38TMQ	散射片
LGP	TR1801A	导光板
REF	75W28	reiko的银反
胶铁	LB1010W	-
LED	3004 Silicate	AOT LED

Note 5.4: The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

Note 5.5: The electro-optical response time measurements shall be made as Figure 6 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

<Figure 6. Response Time Testing>



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~60℃（30min），50 cycles	

9. Packing Method----TBD

- END -