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SPECIFICATION FOR LCM+CTP Module

MODULE No:	ET035HV30-KT V1
CUSTOMER:	

YOURITECH	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
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* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, capacitance touch panel, back-light unit. The resolution of a 3.5" TFT-LCD contains 320x480 pixels, and can display up to 16.7M colors

* Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	48.96(H)*73.44(V) (3.5inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	16.7M	colors	-
Number of pixels	320(RGB)*480	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.153(H)*0.153(V)	mm	-
Viewing angle	ALL	o'clock	-
Controller IC	ST7796SI	-	-
LCM Interface	8/9/16/18Bit MCU 3/4SPI+16/18Bit RGB 3-line/4-line Serial Interface	-	-
Display mode	Transmissive/ Normally Black	-	-
Operating temperature	-30~+85	°C	-
Storage temperature	-30~+85	°C	-
Module bonding technology	Use Tape bonding between LCM and CTP	-	-

*CTP Features

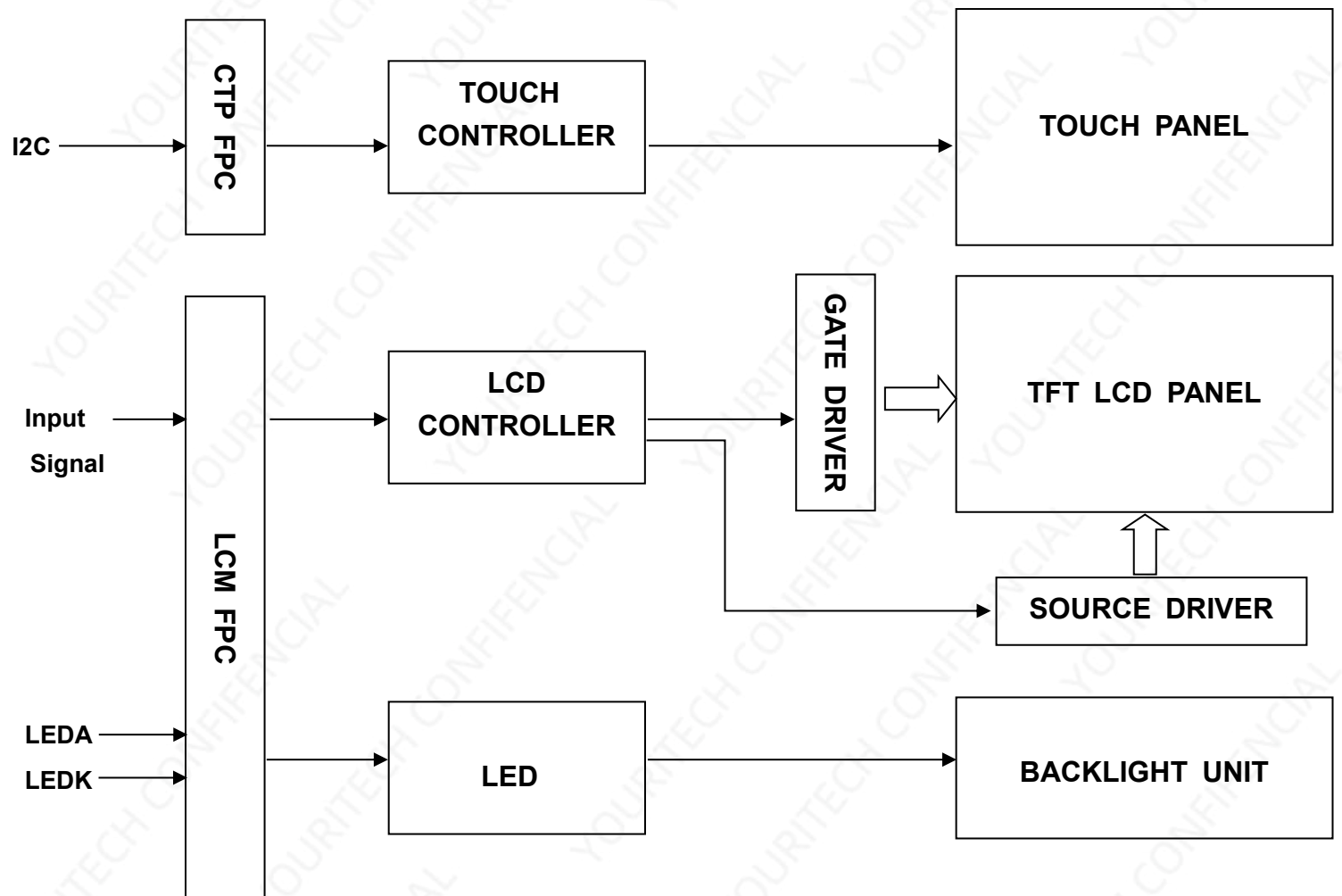
General Information Items	Specification	Unit	Note
	Main Panel		
Resolution	320(H)*480(V)	-	
Structure	G+G	-	
Controller IC	FT5436	-	
Interface	I2C	-	
Slave Address	0x38(7bit)/8bit:0x70(Write) 0x71(Read)	-	
Touch mode	Five points and Gestures	-	
Logic level	3.3	V	



* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		55.50		mm	-
	Vertical(V)		84.96		mm	-
	Depth(D)		4.25		mm	-
Weight			35		g	-

1. Block Diagram



3. Input terminal Pin Assignment

3.1 TFT

NO.	SYMBOL	DISCRIPTION					I/O
1	GND	Ground.					P
2	XR(NC)	Touch panel Right Glass Terminal					A/D
3	YD(NC)	Touch panel Bottom Film Terminal					A/D
4	XL(NC)	Touch panel LIFT Glass Terminal					A/D
5	YU(NC)	Touch panel Top Film Terminal					A/D
6	IOVCC	I/O power supply voltage.					P
7	VCC	Supply Voltage (3.3V).					P
8	IM0	Interface Selection					I
9	IM1	IM2	IM1	IM0	Interface type	DB Pin in use	
10	IM2	0	0	0	DBI Tyb_ 18-bit interface	DB17-DB0	
		0	0	1	DBI Tyb_ 9-bit interface	DB8-DB0	
		0	1	0	DBI Tyb_ 16-bit interface	DB15-DB0	
		0	1	1	DBI Tyb_ 8-bit interface	DB7-DB0	
		1	0	1	3-Wire 9 BIT data serial interface	SDI SCL CS	
		1	1	1	4-Wire 8 BIT data serial interface	SDI SCL CS RS	
11	RESET	Reset input signal Initialize the chip with a low input. Be sure to execute a power-on reset after supplying power.					I
12	VSYNC	Frame synchronizing signal Fix to DGND level when not in use.					I
13	HSYNC	Line synchronizing signal Fix to DGND level when not in use.					I
14	PCLK	Dot clock signal Fix to DGND level when not in use.					I
15	DE	A data ENABLE input signal Fix to DGND level when not in use.					I
16-33	DB17-DB0	18-bit data bus.					I/O
		RGB Interface Type			Data PIN in Use		



		16 BIT RGB	DB0-DB15	
		18 BIT RGB	DB0-DB17	
		Fix to GND level when not in use		
34	SDO	Serial data output Leave the pin open when not in use.		O
35	SDA	DIN/SDA: serial data input/output bi-direction pin Fix to DGND level when not in use.		I
36	RD	serve as a read signal Fix to IOVCC level when not in use.		I
37	WR(SPI-SCL)	WRX pin, serves as a write signal SCL pin as Serial Clock when operates in the serial interface Fix to IOVCC level when not in use.		I
38	RS	Data/Command Selection pin Low: Command High: Parameter Fix to IOVCC level when not in use.		I
39	CS	Chip select input signal Low: the chip is selected and accessible High: the chip is not selected and not accessible Fix to IOVCC level when not in use.		I
40	GND	Ground.		P
41	LEDK8	Cathode pin OF backlight		P
42	LEDK7			
43	LEDK6			
44	LEDK5			
45	LEDK4			
46	LEDK3			
47	LEDK2			
48	LEDK1			
49	LEDA	Anode pin of backlight		P
50	GND	Ground.		P



3.2 CTP

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VDDIO	Supply voltage.	P
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P



4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	$\Theta=0$ Normal viewing angle	800	1000	--		NOTE2
Response time	Rising	T_R+T_F		--	30	35	msec	NOTE4
	Falling							
Uniformity		S(%)		60	65	--	%	NOTE1
Color Filter Chromaticity	White	W_X	-0.04	-0.04	0.314	$+0.04$		
		W_Y			0.355			
	Red	R_X			0.632			
		R_Y			0.349			
	Green	G_X			0.310			
		G_Y			0.581			
	Blue	B_X			0.147			
		B_Y			0.056			
Viewing angle	Hor.	Θ_L	CR>10	80	85	--		NOTE5
		Θ_R		80	85	--		
	Ver.	Θ_U		80	85	--		
		Θ_D		80	85	--		
Option View Direction		ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding : dark room

Ambient temperature : $25\pm 2^\circ\text{C}$

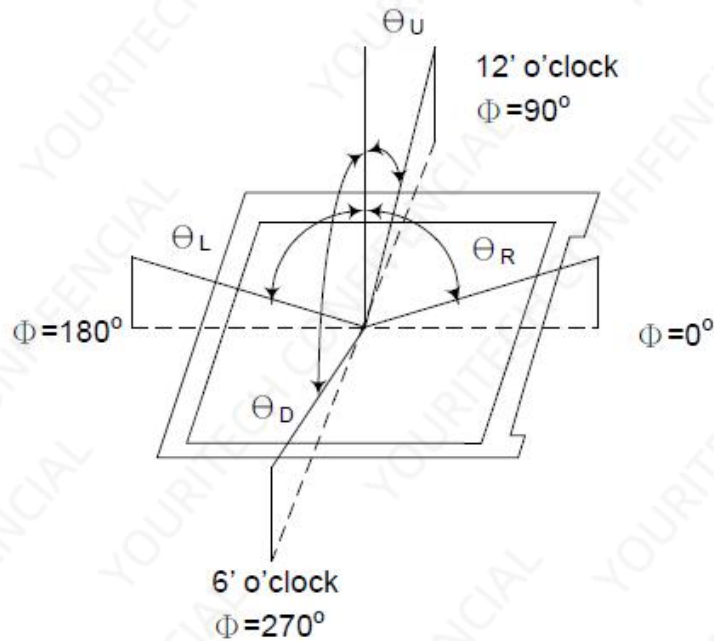
15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.



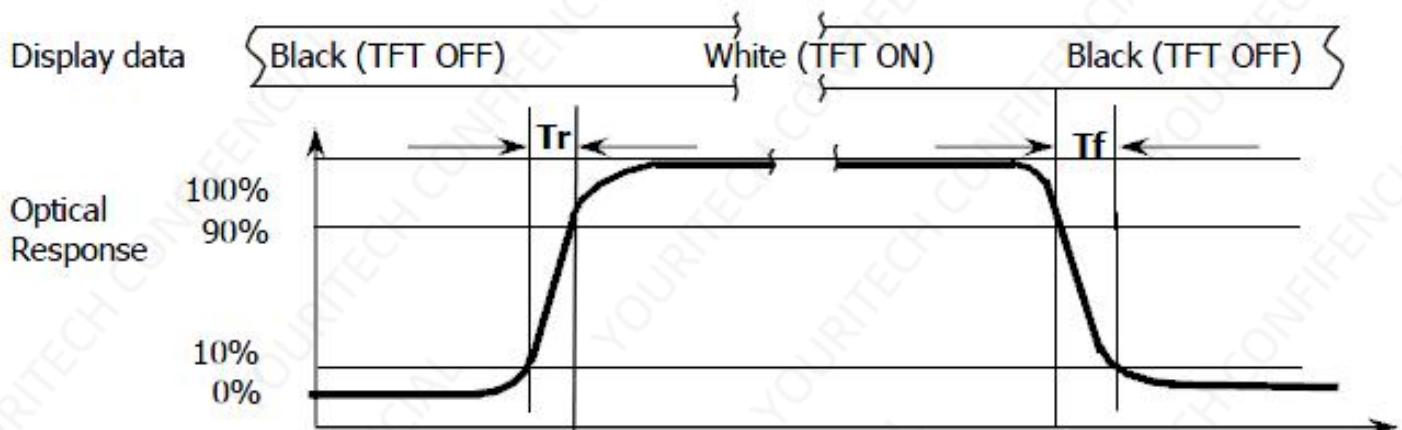
Note (1): Definition of Viewing Angle :



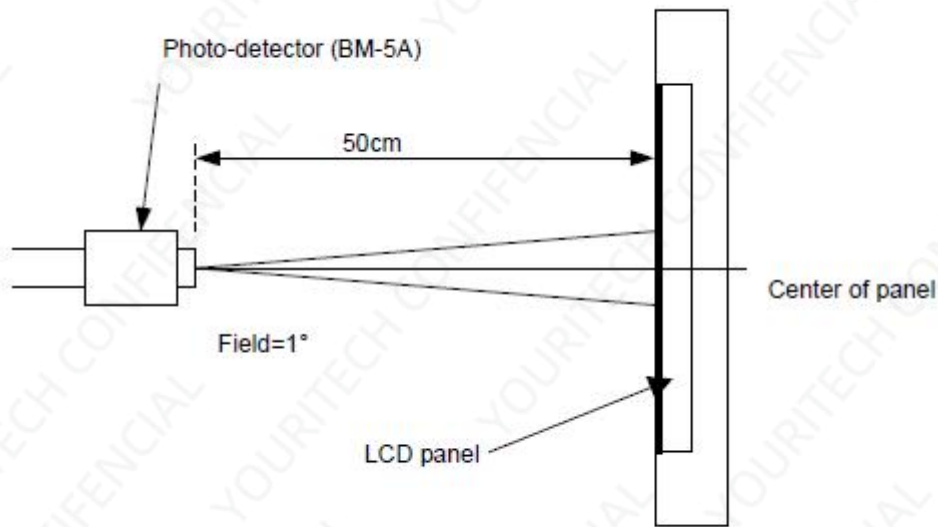
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VCI	-0.3	4.6	V
Digital interface supply Voltage	IOVCC	-0.3	4.6	V
Operating temperature	T _{OP}	-30	+85	°C
Storage temperature	T _{ST}	-30	+85	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	2.75	3.6	V	
Digital interface supply Voltage	IOVCC	1.65	1.8	3.6	V	
Normal mode Current consumption	IDD	--	12	24	mA	
Level input voltage	V _{IH}	0.7IOVCC		IOVCC	V	
	V _{IL}	GND		0.3IOVCC	V	
Level output voltage	V _{OH}	0.8IOVCC		IOVCC	V	
	V _{OL}	GND		0.2IOVCC	V	



5.3 LED Backlight Characteristics

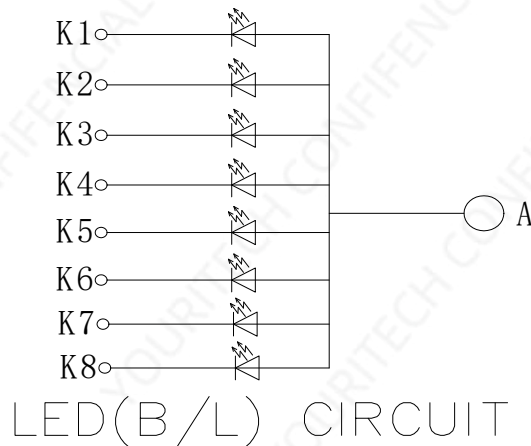
The back-light system is edge-lighting type with 8 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	120	160	--	mA	
Forward Voltage	V_F	--	3.2	--	V	
LCM Luminance	L_V	530	630	--	cd/m ²	$I_F=160\text{mA}$
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

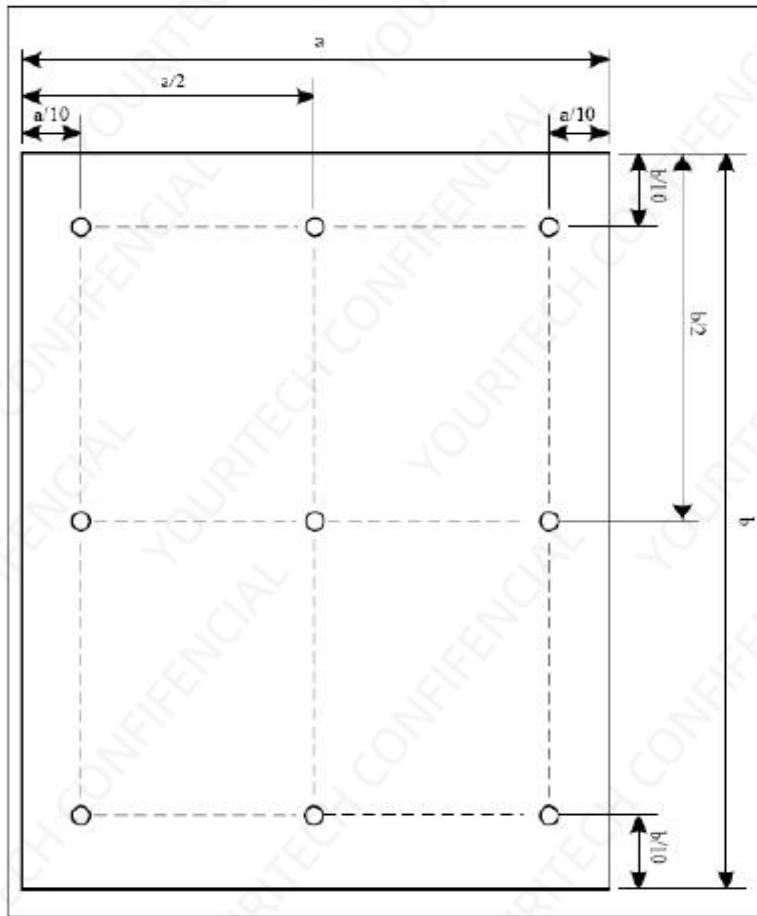
Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

$T_a=25\pm3\text{ }^{\circ}\text{C}$, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at $T_a=25^{\circ}\text{C}$ and $I_L=160\text{mA}$. The LED lifetime could be decreased if operating I_L is larger than 160mA. The constant current driving method is suggested.



NOTE 3: Luminance Uniformity of these 9 points is defined as below:



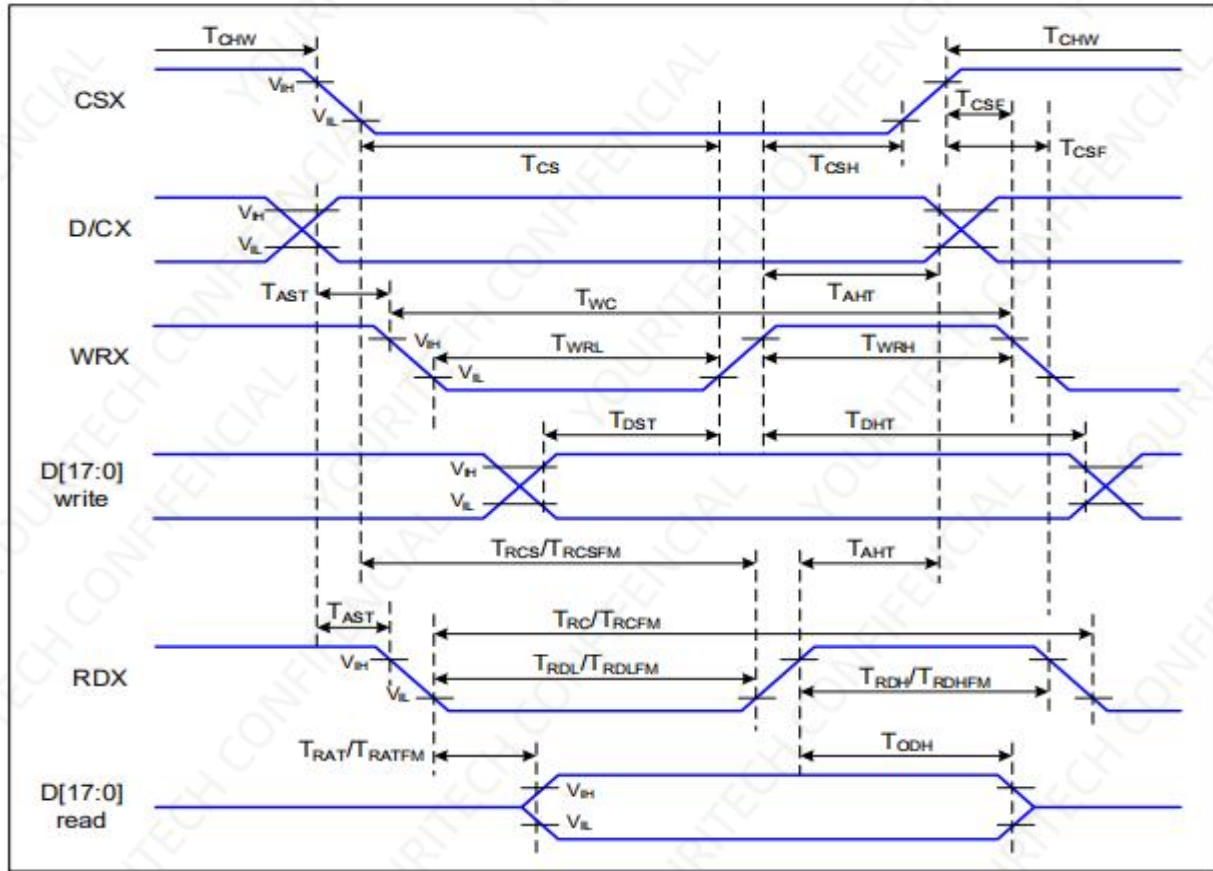
$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$



6. AC Characteristic

6.1 Display Parallel 8/16-bit Interface Timing Characteristics (8080 system)



Parallel Interface Timing Characteristics (8080-Series MCU Interface)

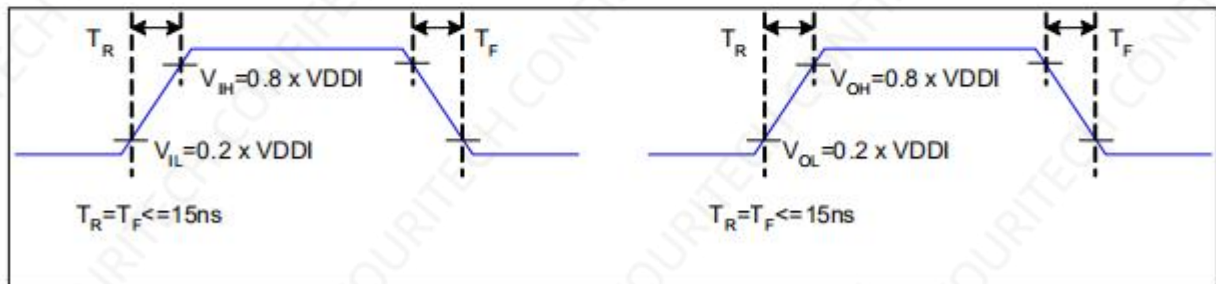
VDDI=1.8V, VDDA=2.8V, AGND=DGND=0V, T_a=25 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T _{AST}	Address setup time	0		ns	-
	T _{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T _{CHW}	Chip select "H" pulse width	0		ns	-
	T _{CS}	Chip select setup time (Write)	15		ns	
	T _{RC}	Chip select setup time (Read ID)	45		ns	
	T _{RCFM}	Chip select setup time (Read FM)	355		ns	
	T _{CSF}	Chip select wait time (Write/Read)	10		ns	
	T _{CSH}	Chip select hold time	10		ns	
WRX	T _{WC}	Write cycle	66		ns	-
	T _{WRH}	Control pulse "H" duration	15		ns	



	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)	-	40	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ODH}	Output disable time	20	80	ns	

8080 Parallel Interface Characteristics

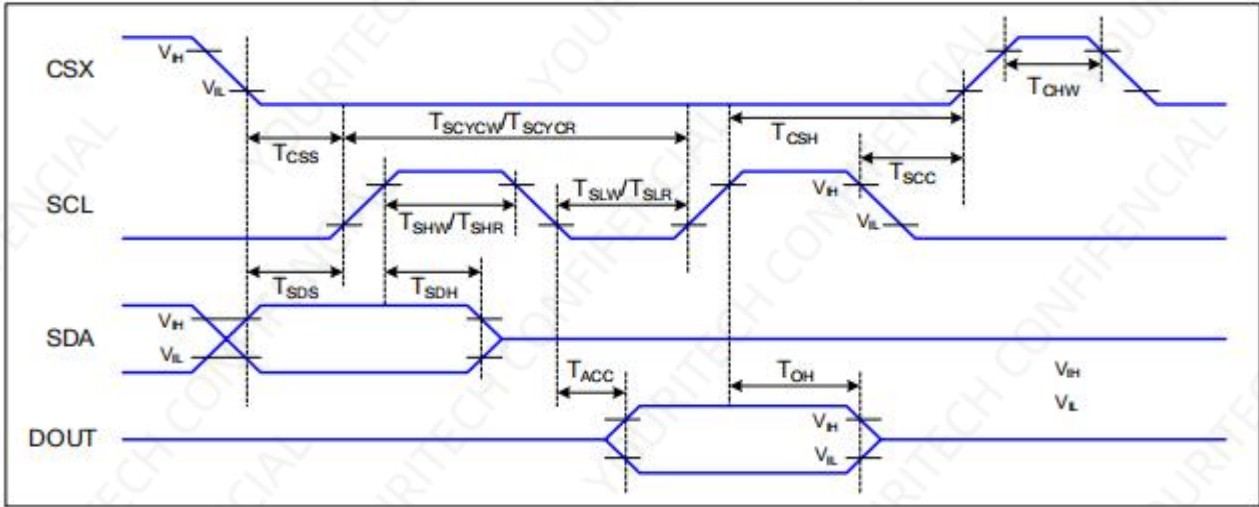


Rising and Falling Timing for I/O Signal

Note: The rising time and falling time (T_R , T_F) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 20% and 80% of V_{DDI} for Input signals.



6.2 Display Serial Interface Timing Characteristics (3-line SPI system)



3-SPI Interface Timing Characteristics

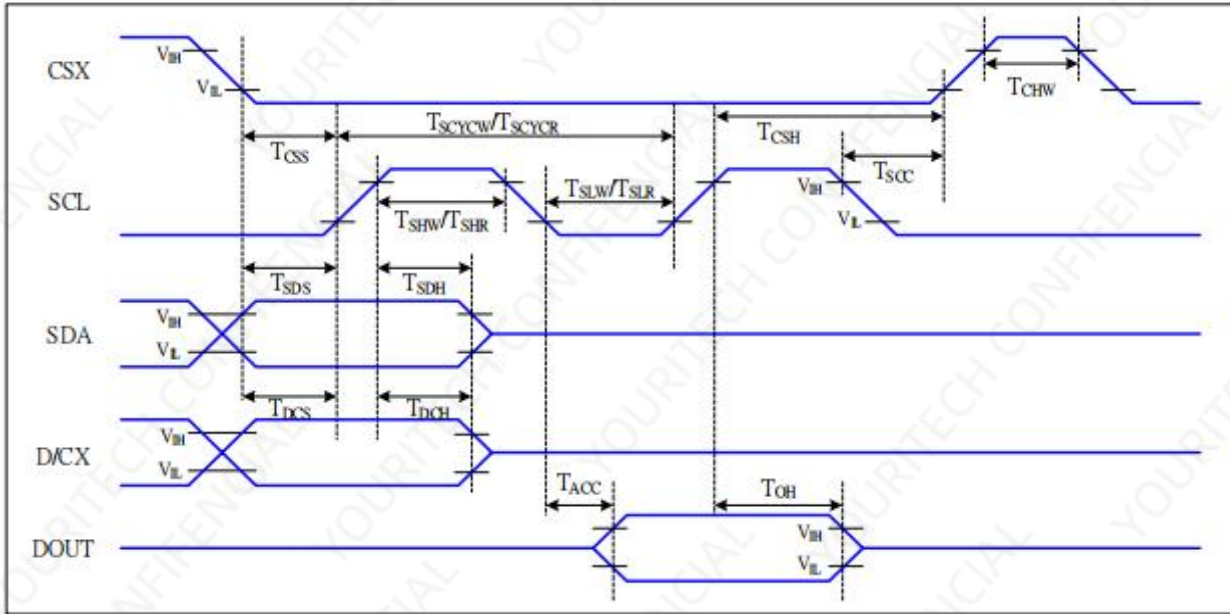
$V_{DD1}=1.8V, V_{DDA}=2.8V, AGND=DGND=0V, T_a=25^{\circ}C$

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	$T_{SCYC W}$	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	$T_{SCYC R}$	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

3-SPI Interface Characteristics



6.3 Display Serial Interface Timing Characteristics (4-line SPI system)



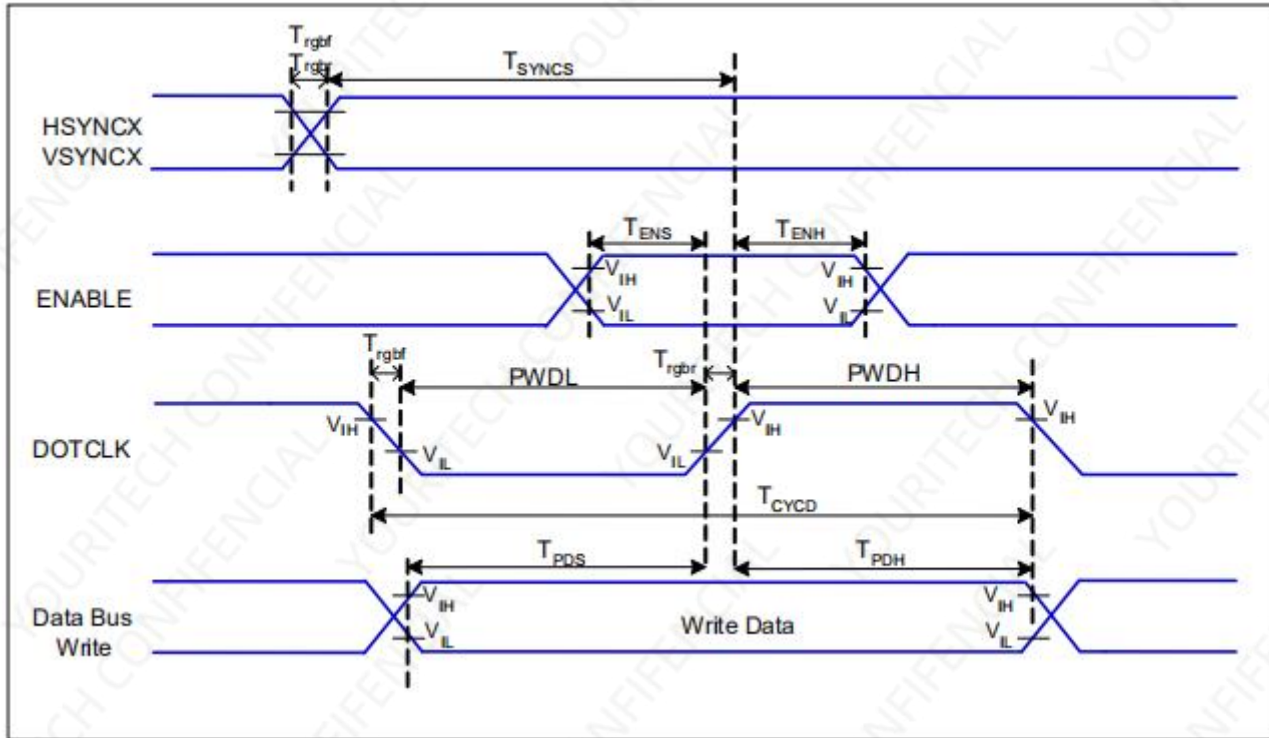
4-SPI Interface Timing Characteristics

VDDI=1.8V, VDDA=2.8V, AGND=DGND=0V, $T_a=25^\circ\text{C}$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF



6.4 Parallel RGB Interface Timing Characteristics



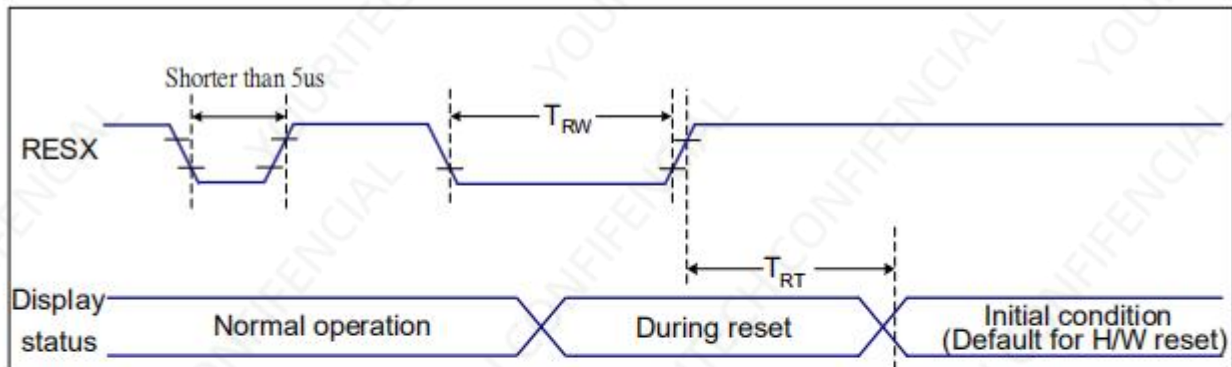
$V_{\text{DDI}}=1.8\text{V}, V_{\text{DDA}}=2.8\text{V}, A_{\text{GND}}=D_{\text{GND}}=0\text{V}, T_a=25^\circ\text{C}$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNC}	VSYNC, HSYNC Setup Time	15	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	15	-	ns	
	T_{ENH}	Enable Hold Time	15	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	30	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	30	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	66	-	ns	
	$T_{\text{rghr}}, T_{\text{rghf}}$	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	15	-	ns	
	T_{PDH}	PD Data Hold Time	15	-	ns	

RGB Interface Timing Characteristics



6.5 Reset Timing Characteristics



Reset Timing

$V_{DDI}=1.8V, V_{DDA}=2.8V, AGND=DGND=0V, T_a=25^{\circ}C$

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 1 Reset Timing

Notes:

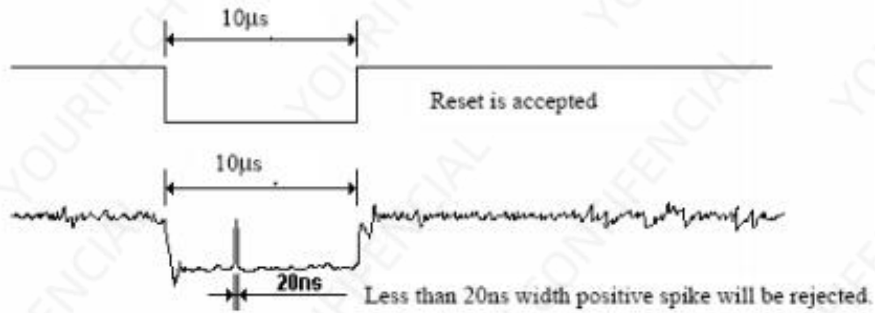
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:





5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.



7. CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	-0.3	3.6	V	1
I/O Digital Voltage	VDDIO	1.8	3.6	V	1
Operating temperature	T _{OP}	-20	+70	°C	-
Storage temperature	T _{ST}	-30	+80	°C	-

NOTES:

- If used beyond the absolute maximum ratings, FT5436 may be permanently damaged. It is strongly recom-manded that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

7.1.2 DC Electrical Characteristics (Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Digital supply voltage	VDD		2.8	3.3	3.6	V	
I/O Digital supply voltage	VDDIO		1.8	3.3	3.6	V	
Normal operation mode Current consumption	I _{opr}	VDD=2.8V	-	4	-	mA	
Monitor mode Current consumption	I _{mon}	Ta=25°C MCLK=17.5Mhz	-	1.5	-	mA	
Sleep mode Current consumption	I _{slp}			50		uA	
Level input voltage	V _{IH}		0.7V _{DDIO}	-	V _{DDIO}	V	
	V _{IL}		-0.3	-	0.3V _{DDIO}	V	
Level output voltage	V _{OH}	I _{OH} =-0.1mA	0.7V _{DDIO}	-	-	V	
	V _{OL}	I _{OH} =0.1mA	-	-	0.3V _{DDIO}	V	



7.2 AC Characteristics

Table 4-1 AC Characteristics of Oscillators

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
OSC clock 1	fosc1	VDDA= 2.8V; Ta=25℃	34.65	35	35.35	MHz	

Table 4-2 AC Characteristics of sensor

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
Sensor acceptable clock	ftx	VDDA= 2.8V; Ta=25℃	0	100	300	KHz	
Sensor output rise time	Ttxr	VDDA= 2.8V; Ta=25℃	-	100	-	nS	
Sensor output fall time	Ttxf	VDDA= 2.8V; Ta=25℃	-	80	-	nS	
Sensor input voltage	Trxi	VDDA= 2.8V; Ta=25℃	-	5	-	V	

7.2.1 I2C Interface

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure4-1:

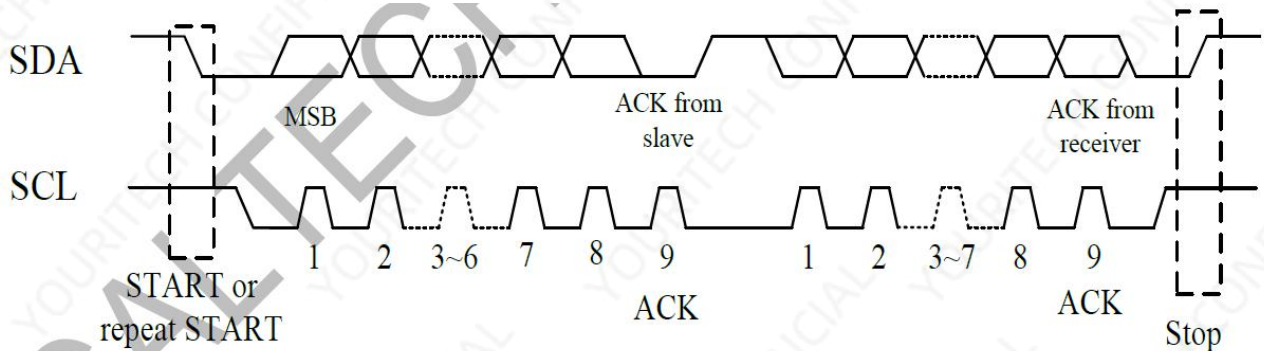


Figure 4-1 I2C Serial Data Transfer Format

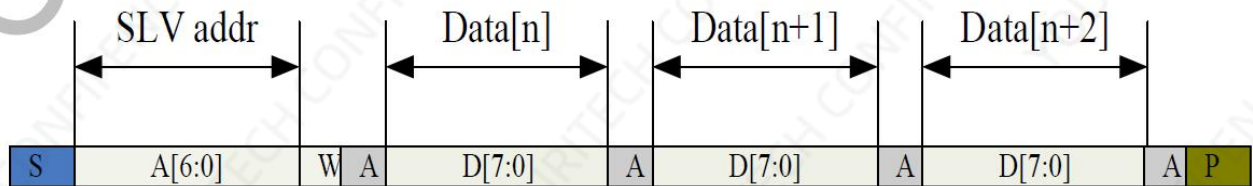


Figure 4-2 I2C master write, slave read



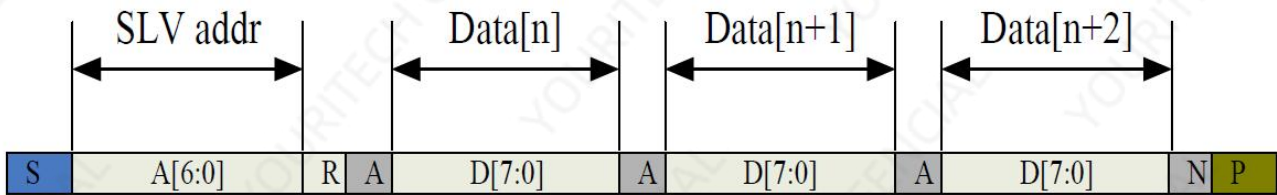


Figure 4-3 I2C master read, slave write

Table4-3 lists the meanings of the mnemonics used in the above figures.

Table 4-3 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0' for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table4-4.

Table 4-4 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us



8. LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

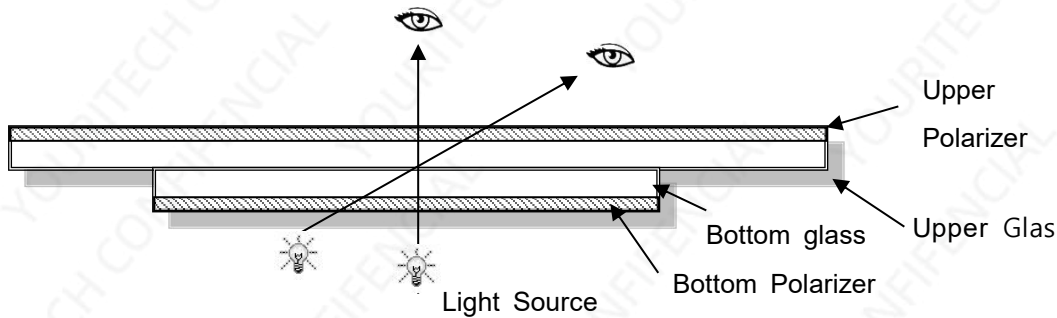
Temperature : $25\pm 5^{\circ}\text{C}$

Humidity : $65\%\pm 10\%\text{RH}$

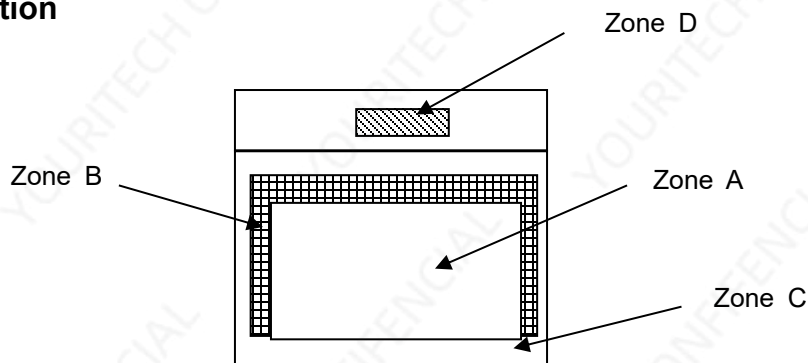
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



8.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C Cover (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note:

As a general rule , visual defects in Zone C can be ignored when it doesn't effect product function or a ppearance after assembly by customer



8.1.3 Sampling Plan

According to GB/T 2828-2012 ; , normal inspection, Class II

AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , LCM: Liquid Crystal Module, CTP: Capacitive Touch Panel

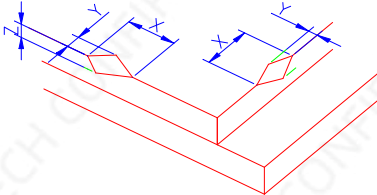
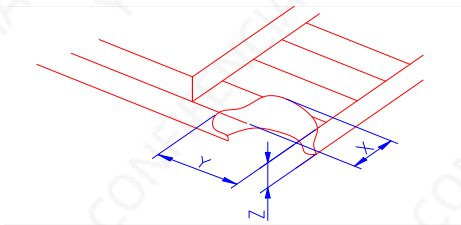
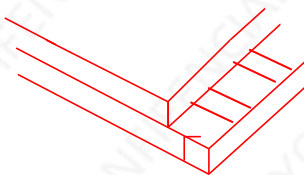
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc	Major
2	Missing	Missing components and etc	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot, Dim spot, (Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer/CTP	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.



8.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of IT O, T: Height of LCD	(1) The edge of LCD broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)LCD corner broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	 Crack Not allowed							



Spot defect

$$\Phi = (X + Y) / 2$$

① light dot (black/white spot , pinhole, stain, etc.)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.15$	Ignore	Ignore	
$0.15 < \Phi \leq 0.25$	3(distance $\geq 10\text{mm}$)		
$0.25 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)		
$\Phi > 0.4$	0		

② Dim spot (light leakage、dent、dark spot, etc)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.15$	Ignore	Ignore	
$0.15 < \Phi \leq 0.25$	3(distance $\geq 10\text{mm}$)		
$0.25 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)		
$\Phi > 0.4$	0		

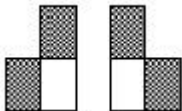
③ Polarizer accidented spot

Zone Size (mm)	Acceptable Qty			
	A	B	C	
$\Phi \leq 0.2$	Ignore		Ignore	
$0.2 < \Phi \leq 0.5$	2(distance $\geq 10\text{mm}$)			
$\Phi > 0.5$	0			

④ Polarizer Bubble

Zone Size (mm)	Acceptable Qty			
	A	B	C	
$\Phi \leq 0.2$	Ignore		Ignore	
$0.2 < \Phi \leq 0.4$	3(distance $\geq 10\text{mm}$)			
$\Phi > 0.4$	0			



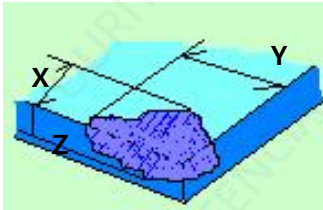
3.0	LCD Pixel defect	Pixel bad points																							
		<table> <tr> <th>Item</th><th>Zone A</th><th>Acceptable Qt</th></tr> <tr> <td rowspan="3">Bright dot</td><td>Random</td><td>$N \leq 2$</td></tr> <tr> <td>2 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td>3 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td rowspan="3">Dark dot</td><td>Random</td><td>$N \leq 2$</td></tr> <tr> <td>2 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td>3 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td>Distance</td><td> 1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot. </td><td>5mm</td></tr> <tr> <td colspan="2">Total bright and dark dot</td><td>$N \leq 4$</td></tr> </table> Note: A) Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern. B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture. C) 2 dot adjacent = 1 pair = 2 dots Picture:     2 dot adjacent 2 dot adjacent 2 dot adjacent (vertical) 2 dot adjacent (slant)	Item	Zone A	Acceptable Qt	Bright dot	Random	$N \leq 2$	2 dots adjacent	$N \leq 0$	3 dots adjacent	$N \leq 0$	Dark dot	Random	$N \leq 2$	2 dots adjacent	$N \leq 0$	3 dots adjacent	$N \leq 0$	Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm	Total bright and dark dot		$N \leq 4$
Item	Zone A	Acceptable Qt																							
Bright dot	Random	$N \leq 2$																							
	2 dots adjacent	$N \leq 0$																							
	3 dots adjacent	$N \leq 0$																							
Dark dot	Random	$N \leq 2$																							
	2 dots adjacent	$N \leq 0$																							
	3 dots adjacent	$N \leq 0$																							
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm																							
Total bright and dark dot		$N \leq 4$																							

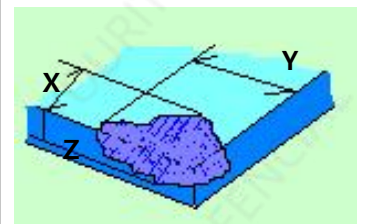


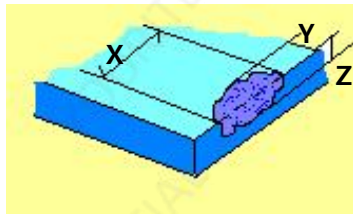
4.0	Line defect (LCD /Polarizer backlight black/white line, scratch, stain)  W: width, L : length N : Count	Width(mm)	Length(m) m)	Acceptable Qty		
				A	B	C
		$\Phi \leq 0.05$	Ignore	Ignore		Ignore
		$0.05 < W \leq 0.06$	$L \leq 4.0$	$N \leq 3$		
		$0.06 < W \leq 0.08$	$L \leq 3.0$	$N \leq 2$		
		$W > 0.08$	Define as spot defect			
5.0	Electronic Components SMT.	Not allow missing parts, solderless connection, cold solder joint, mismatch, The positive and negative polarity opposite				
6.0	Display color& Brightness.	1. Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples. 2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.				
7.0	LCD Mura/Waving/ Hot spot	Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.				

8.0	CTP Related	CTP Cover sensor acc identified black/white spot					
			Size Φ (mm)	Acceptable Qty			
				A	B	C	
			$\Phi \leq 0.1$	Ignore			Ignore
			$0.1 < \Phi \leq 0.2$	3 (distance $\geq 10\text{mm}$)			
			$0.20 < \Phi \leq 0.25$	2 (distance $\geq 10\text{mm}$)			
			$\Phi > 0.25$	0			



		<table><tr><td rowspan="6">CTP Cover scratch</td><td>Width(mm)</td><td>Ignore (mm)</td><td colspan="3">Acceptable Qty</td></tr><tr><td></td><td></td><td>A</td><td>B</td><td>C</td></tr><tr><td>$\Phi \leq 0.05$</td><td>Ignore</td><td colspan="3">Ignore</td></tr><tr><td>$0.05 < W \leq 0.06$</td><td>$L \leq 4.0$</td><td colspan="3">$N \leq 3$</td></tr><tr><td>$0.06 < W \leq 0.08$</td><td>$L \leq 3.0$</td><td colspan="3">$N \leq 2$</td></tr><tr><td>$0.08 < W$</td><td colspan="4">Define as spot defect</td></tr></table>	CTP Cover scratch	Width(mm)	Ignore (mm)	Acceptable Qty					A	B	C	$\Phi \leq 0.05$	Ignore	Ignore			$0.05 < W \leq 0.06$	$L \leq 4.0$	$N \leq 3$			$0.06 < W \leq 0.08$	$L \leq 3.0$	$N \leq 2$			$0.08 < W$	Define as spot defect			
CTP Cover scratch	Width(mm)	Ignore (mm)		Acceptable Qty																													
				A	B	C																											
	$\Phi \leq 0.05$	Ignore		Ignore																													
	$0.05 < W \leq 0.06$	$L \leq 4.0$		$N \leq 3$																													
	$0.06 < W \leq 0.08$	$L \leq 3.0$		$N \leq 2$																													
	$0.08 < W$	Define as spot defect																															
CTP Cover Pinhole/ Lack of ink	<table><tr><td rowspan="5"> Zone Size (mm) </td><td colspan="3">Acceptable Qty</td></tr><tr><td colspan="3">C</td></tr><tr><td colspan="3">Ignore</td></tr><tr><td colspan="3">$3(\text{distance} \geq 10\text{mm})$</td></tr><tr><td colspan="3">$2(\text{distance} \geq 10\text{mm})$</td></tr><tr><td>$\Phi > 0.3$</td><td colspan="3">0</td></tr></table>	Zone Size (mm)	Acceptable Qty			C			Ignore			$3(\text{distance} \geq 10\text{mm})$			$2(\text{distance} \geq 10\text{mm})$			$\Phi > 0.3$	0														
Zone Size (mm)	Acceptable Qty																																
	C																																
	Ignore																																
	$3(\text{distance} \geq 10\text{mm})$																																
	$2(\text{distance} \geq 10\text{mm})$																																
$\Phi > 0.3$	0																																
CTP Bonding bubble/ accidented spot	<table><tr><td rowspan="2">Size Φ(mm)</td><td colspan="2">Acceptable Qty</td></tr><tr><td>A</td><td>B</td></tr><tr><td>$\Phi \leq 0.1$</td><td colspan="2">Ignore</td></tr><tr><td>$0.1 < \Phi \leq 0.2$</td><td colspan="2">$3(\text{distance} \geq 10\text{mm})$</td></tr><tr><td>$0.2 < \Phi \leq 0.25$</td><td colspan="2">$2(\text{distance} \geq 10\text{mm})$</td></tr><tr><td>$\Phi > 0.25$</td><td colspan="2">0</td></tr></table>	Size Φ (mm)	Acceptable Qty		A	B	$\Phi \leq 0.1$	Ignore		$0.1 < \Phi \leq 0.2$	$3(\text{distance} \geq 10\text{mm})$		$0.2 < \Phi \leq 0.25$	$2(\text{distance} \geq 10\text{mm})$		$\Phi > 0.25$	0																
Size Φ (mm)	Acceptable Qty																																
	A	B																															
$\Phi \leq 0.1$	Ignore																																
$0.1 < \Phi \leq 0.2$	$3(\text{distance} \geq 10\text{mm})$																																
$0.2 < \Phi \leq 0.25$	$2(\text{distance} \geq 10\text{mm})$																																
$\Phi > 0.25$	0																																
Assembly deflection	beyond the edge of backlight $\leq 0.2\text{mm}$																																
CTP cover broken X : length Y : width Z : height	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>$X \leq 0.5\text{mm}$</td><td>$Y \leq 0.5\text{mm}$</td><td>$Z < \text{cover thickness}$</td></tr></table> * Circuitry broken is not allowed.	X	Y	Z	$X \leq 0.5\text{mm}$	$Y \leq 0.5\text{mm}$	$Z < \text{cover thickness}$																										
X	Y	Z																															
$X \leq 0.5\text{mm}$	$Y \leq 0.5\text{mm}$	$Z < \text{cover thickness}$																															



			X	Y	Z	
		CTP cover broken	$X \leq 0.3\text{mm}$	$Y \leq 0.3\text{mm}$	$Z < \text{cover thickness}$	
		X : length Y : width Z : height	* Circuitry broken is not allowed.			

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	CTP no function	Not allowed



9. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	85°C,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-30°C, 96HR	
High Temperature Storage	85°C, 96HR	
Low Temperature Storage	-30°C, 96HR	
High Temperature & High Humidity Operating	+60°C, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-30°C,30 min ↔ +80°C,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15°C~35°C, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM BOX)	

Remark:

- 1.The test samples should be applied to only one test item.
- 2.Sample size for each test item is 5~10pcs.
- 3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
- 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.



10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

10.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.



11. Packing

---TBD-----

