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Production Custom designs Installation



MODEL NO : ET035VG04-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-02-18

☐ Preliminary Specification

☒ Final Product Specification

Customer : _____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 640xRGBx480.

As to basic specification of the driver IC, refer to the IC (ST7703I) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;

IPS Type LCD

640dot-segment and 480 dot-common outputs;

16.7M Color can be selected by software;

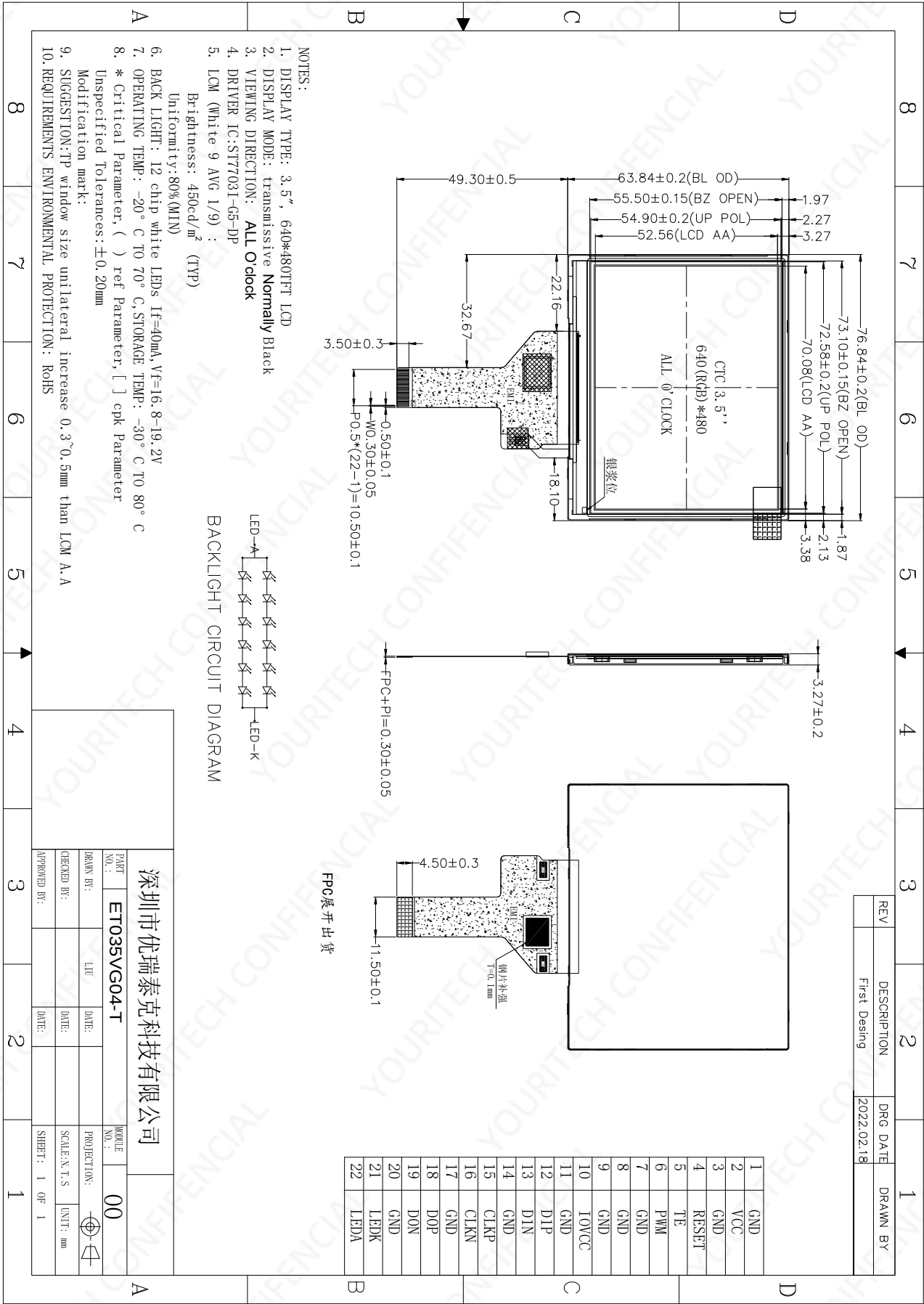
White LED back light;

2lane MIPI interface

1.3 Applications:

2. LCM General specification

ITEM	Standard value	Unit
LCD Type	Normally black	--
Drive element	TFT active matrix	--
Number of pixels	640*3RGB(H)X480(V)	Dots
Pixel arrangement	RGB stripe	--
Pixel Pitch (W*H)	0.1095(W) × 0.1095 (H)	mm
Active area	70.08(W) × 52.56(H)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	ST7703I	--
TFT interface	2lane MIPI interface	--
Module Size(W*H*T)	76.84(W) ×63.84(H) ×3.27(T)	mm
Approx. Weight	TBD	g
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--



3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T _{OPR}	-20	+70	°C
LCM Storage Temperature	T _{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.5	3.3	3.6	V
Supply Voltage for(DC/DC)	AVDD	--	--	--	V
Supply Voltage for(DC/DC)	AVEE	--	--	--	V

4.2 Back-Light Unit Characeristics

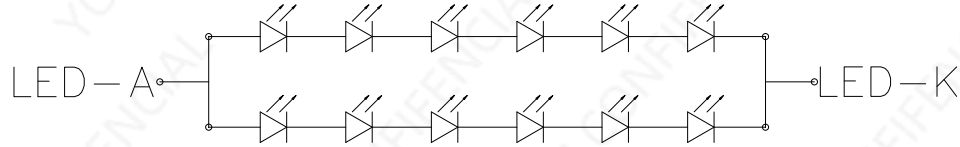
The back-light system is an edge-lighting type with 12 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V _F	16.8	--	19.2	V	--
Forward current	I _F	--	40	--	mA	--
Luminance(With LCD)	L _v	--	450	--	cd/m ²	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

- (1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:

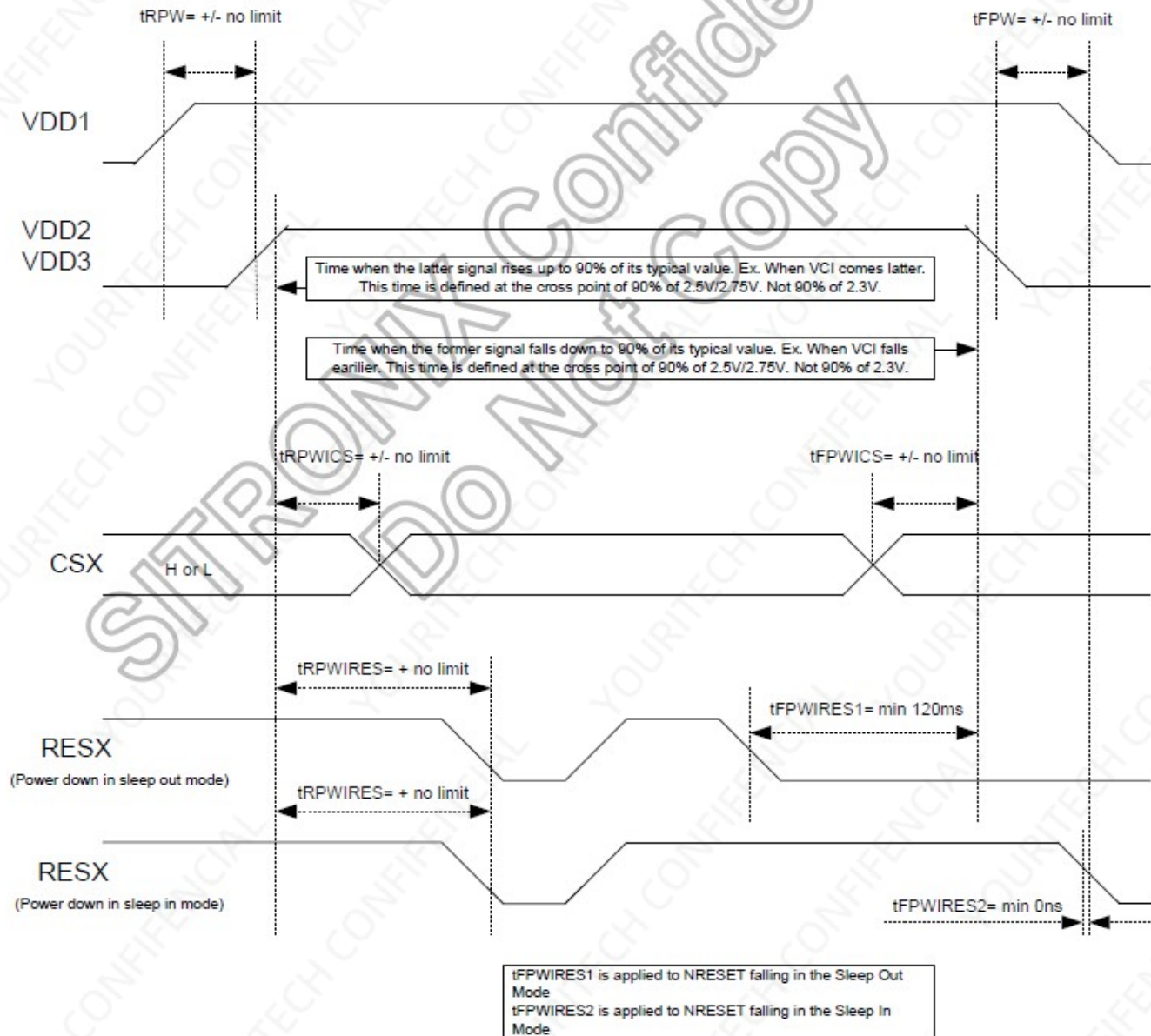


5. Module Function Description

Pin No.	Symbol	Description
1	GND	Power Ground
2	VDD(2.8V)	Analog power supply (VCI): 2.5V to 3.3V
3	GND	Power Ground
4	RESET	Reset signal input terminal. Active at 'L'.
5	TE	Tearing effect output pin is used to synchronize MCU frame writing,
6	PWM	LCD backlight control PWM output pin.
7	GND	Power Ground
8	GND	Power Ground
9	GND	Power Ground
10	IOVCC(1.8V)	Analog power supply (VCI): 1.65V to 3.3V
11	GND	Power Ground
12	D1P	High speed interface data differential signal input/output pins
13	D1N	High speed interface data differential signal input/output pins
14	GND	Power Ground
15	CLKP	High speed interface clock differential signal input pins
16	CLKN	High speed interface clock differential signal input pins
17	GND	Power Ground
18	D0P	High speed interface data differential signal input/output pins
19	D0N	High speed interface data differential signal input/output pins
20	GND	Power Ground
21	LEDK	Power supply for backlight cathode input terminal.
22	LEDA	Power supply for backlight anode input terminal.

6. Timing Characteristics

If RESX line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied- otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



High Speed Mode

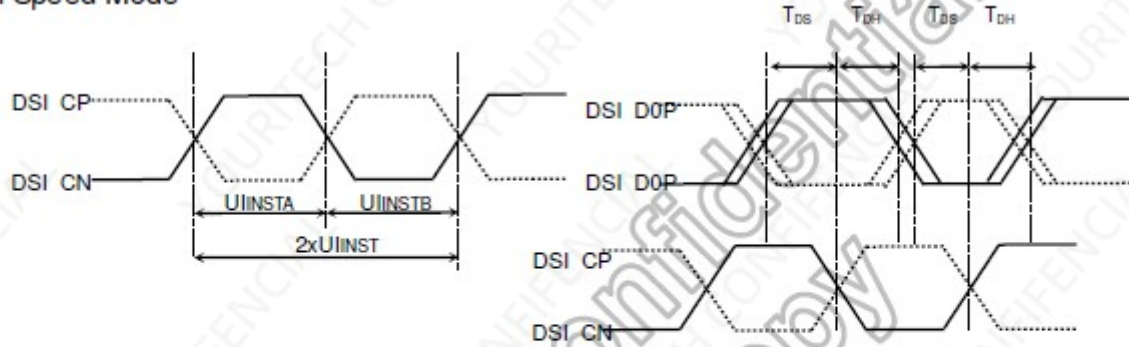


Figure 7.4: DSI clock timing Characteristics

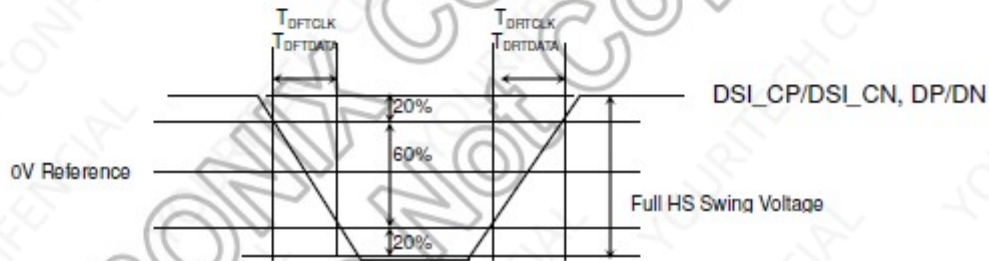


Figure 7.5: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xUI_INST	TBD	-	25	ns
	UI instantaneous	UI_INSTA UI_INSTB	TBD	-	12.5	ns
DP/DN	Data to clock setup time	T _{DS}	0.15xUI	-	-	ps
	Data to clock hold time	T _{DH}	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	T _{DRTCLK}	150	-	0.3UI	ps
	Differential fall time for clock	T _{DFTCLK}	150	-	0.3UI	ps
DP/DN	Differential rise time for data	T _{DRTDATA}	150	-	0.3UI	ps
	Differential fall time for data	T _{DFTDATA}	150	-	0.3UI	ps

Table 7.3: DSI High Speed Mode Characteristics

Low Power Mode

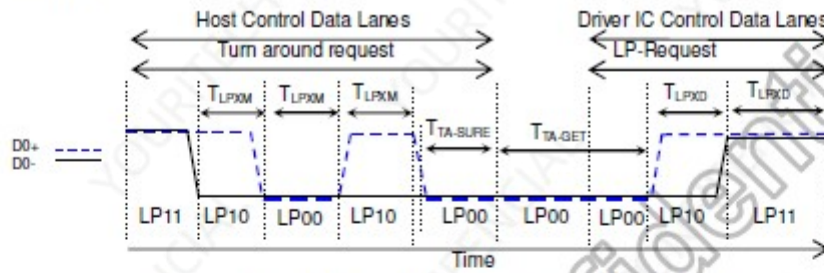


Figure 7.6: BTA from HOST to Display Module Timing

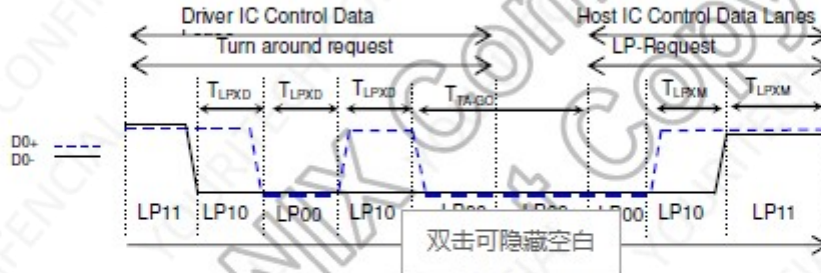
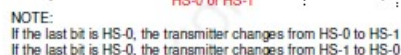
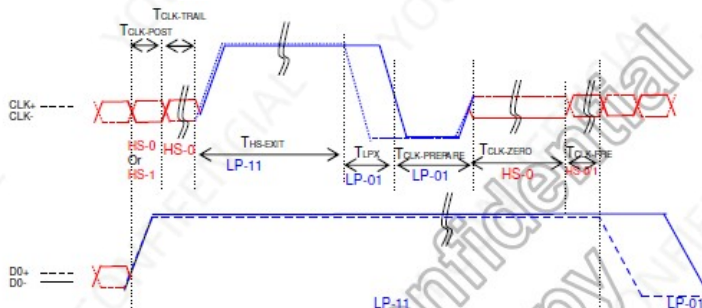


Figure 7.7: BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, $T_A = -30$ to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host → Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module → Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	$2 \times T_{LPXD}$	ns
	Time to drive LP-00 by display module	T_{TA-GET}	$5 \times T_{LPXD}$	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	$4 \times T_{LPXD}$	-	-	ns

Table 7.4: DSI Low Power Mode Characteristics

Table 7.5: DSI Low Power Mode to High Speed Mode TimingTable 7.6: DSI Low Power Mode to High Speed Mode TimingTable 7.7: Clock Lanes High Speed Mode to/from Low Power Mode Timing

Reset input timing

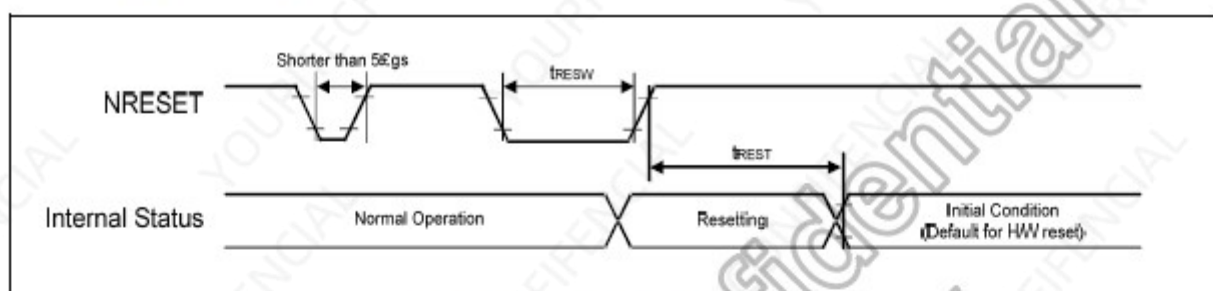


Figure 7.8: Reset input timing

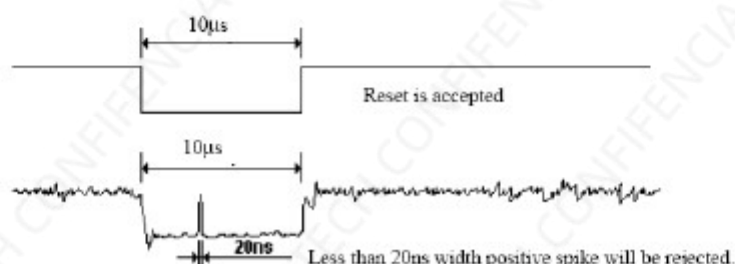
Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width ⁽¹⁾	NRESET	10	-	-	-	μs
tREST	Reset complete time ⁽²⁾	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 7.8: Reset Input Timing

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

- (2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out-mode. The display remains the blank state in Sleep In-mode) and then return to Default condition for H/W reset.
- (3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is HW reset complete time (tREST) within 15ms after a rising edge of NRESET.
- (4) Spike Rejection also applies during a valid reset pulse as shown as below:



- (5) It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

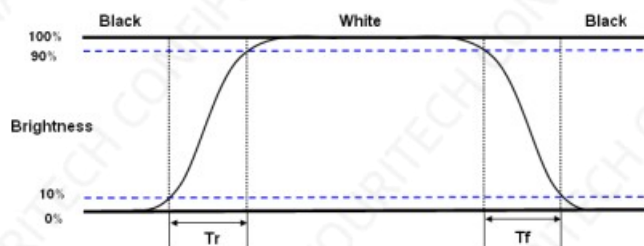
Item	Symbol	Condition	Specification			Unit	Remark
			Min.	Typ.	Max.		
Response time	Tr+Tf	$\theta = 0^\circ$	-	25	50	ms	Note 1,2
Contrast ratio	CR	$\theta = 0^\circ$	600	800	-		Note 1,3
Viewing angle	Top	CR $\geq$ 10	75	85	-	deg.	Note 1,4
	Bottom		75	85	-		
	Left		75	85	-		
	Right		75	85	-		
Color chromaticity (CF only with C light, CIE 1931)	Wx	$\theta = 0^\circ$	-0.015	0.297	+0.015		Note 1,5,6 CF glass
	Wy		-0.015	0.318	+0.015		
Color Gamut (CF only with C light, CIE 1931)	NTSC	CIE1931	45	50	-	%	Note 1,5,6 CF glass
Transmittance (with Polarizer)	Trans	$\theta = 0^\circ$	3.7	4.4	-	%	Note 7 Normal POL

Note 1: Measuring Conditions:

The optical characteristics are determined after the unit has been 'ON' and stable at the maximum brightness, in a dark environment at an ambient temperature at $25^\circ\text{C} \pm 2^\circ\text{C}$.

Note 2: Definition of response time:

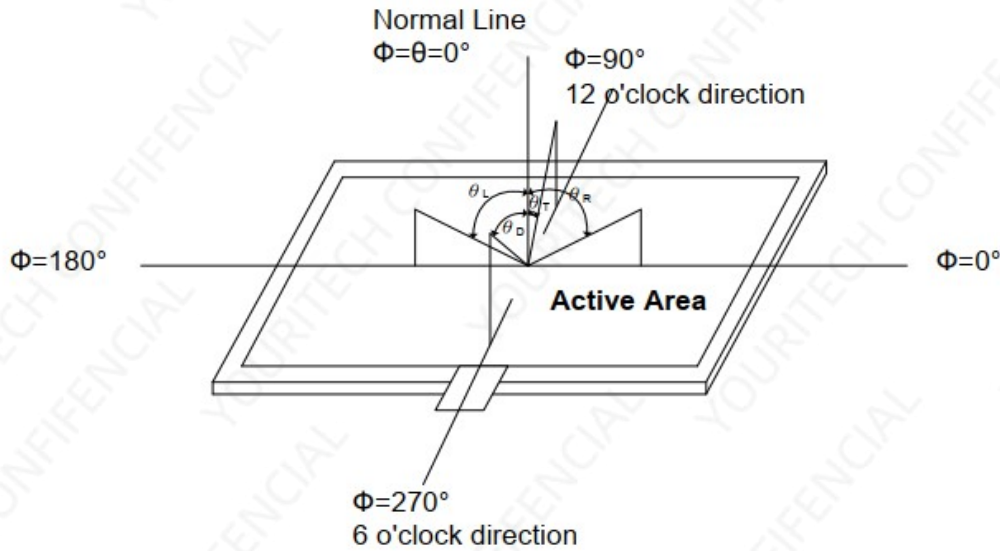
The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time is the time between photo detector output intensity changed from 10% to 90%. And fall time is the time between photo detector output intensity changed from 90% to 10%.



Note 3: Definition of contrast ratio:

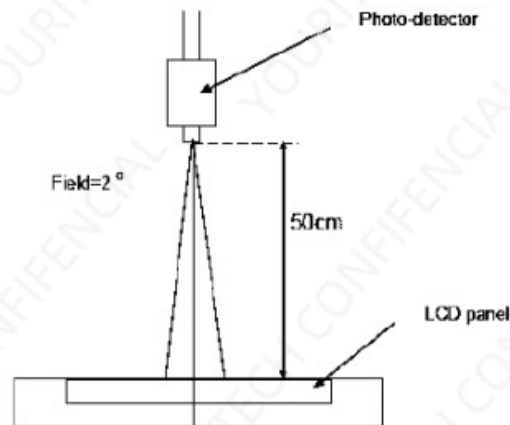
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 4: Definition of viewing angle



Note 5: Optical characteristic measurement setup.

The LCD module should be stabilized at given temperature for 10 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 10 minutes in a windless room.

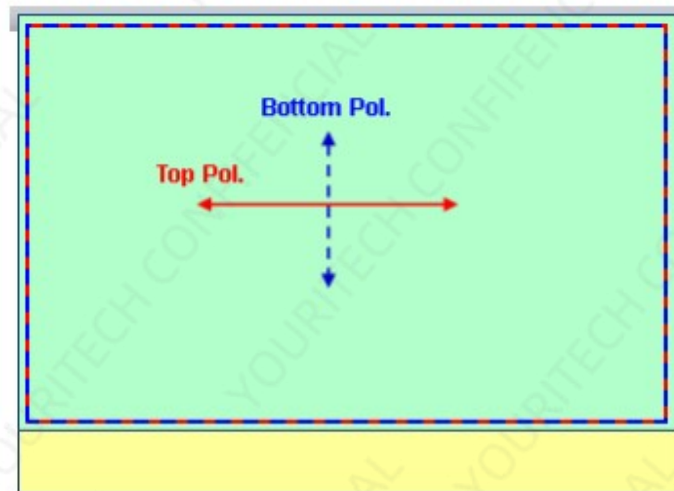


Note 6: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 7: Direction of POL absorption axis

The red and blue arrow directions are meant to be absorption axis.



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test is OK. Missing Segment, short, unclear segment non-display, display abnormally and liquid crystal leakage un-allowed. 2. No low temperature bubbles, end seal loose and fall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature / Humidity storage	60°C x 90%RH / 96H	
6	Thermal and cold shock	Static state, -30°C (30min) ~80°C (30min), 50 cycles	

9. Packing Method----TBD

- END -