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MODEL NO : ET035VG05-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-09-20

□**Preliminary Specification**

■**Final Product Specification**

Customer :_____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 640xRGBx480.
As to basic specification of the driver IC, refer to the IC (ST7703I) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

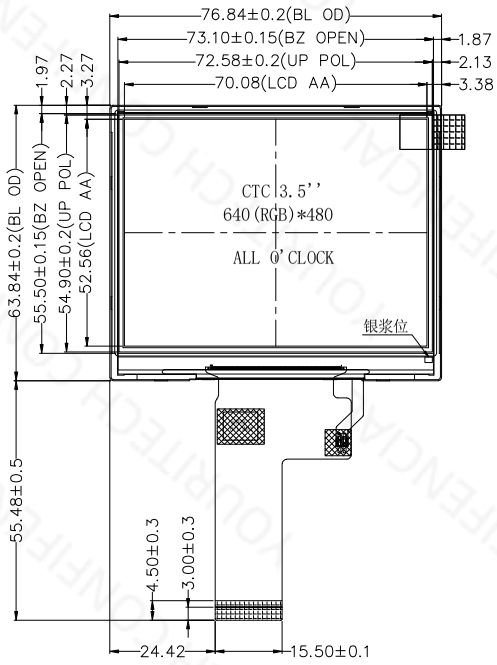
Structure: TFT PANNEL+IC +FPC+BL+CTP;
IPS Type LCD
640dot-segment and 480 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
4lane MIPI interface

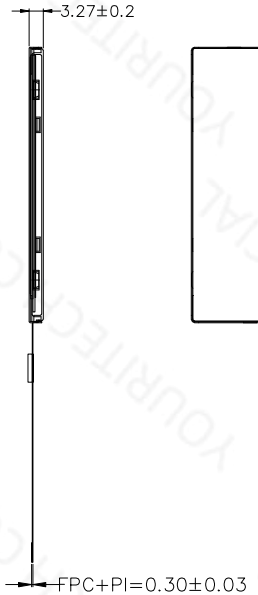
1.3 Applications:

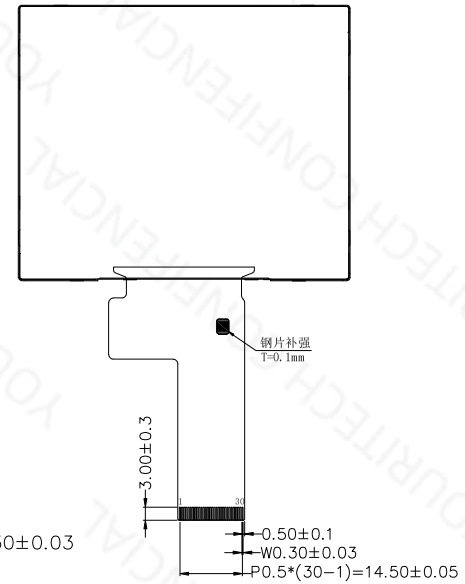
2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally black	--
Drive element	TFT active matrix	--
Number of pixels	640*3RGB(H)X480(V)	Dots
Pixel arrangement	RGB stripe	--
Pixel Pitch (W*H)	0.1095(W) × 0. 1095 (H)	mm
Active area	70.08(W) × 52.56(H)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	ST7703	--
TFT interface	2lane MIPI interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	76.84(W) ×63.84(H) ×3.27(T)	mm
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--

REV	DESCRIPTION	DRG DATE	DRAWN BY
	First Desing	2022.08.10	



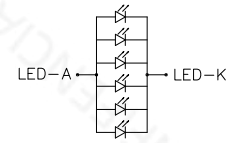




FPC展开出货

1	LEDK
2	LEDK
3	LEDA
4	LEDA
5	NC
6	GND
7	TDN0
8	TDP0
9	GND
10	TDN1
11	TDP1
12	GND
13	CLKN
14	CLKP
15	GND
16	TDN2
17	TDP2
18	GND
19	TDN3
20	TDP3
21	GND
22	GND
23	NC
24	GND
25	TE
26	RESET
27	IOVCC1.8V
28	VDD2.8V
29	GND
30	GND

NOTES:
1. DISPLAY TYPE: 3.5″, 640*480TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL O'clock
4. DRIVER IC:ST7703I
5. LCM (White 9 AVG 1/9) :
   Brightness: 750cd/m² (TYP)
   Uniformity:80%(MIN)
6. BACK LIGHT: 6 chip white LEDs If=120mA,Vf=2.8-3.2V
7. OPERATING TEMP: -20° C TO 60° C,STORAGE TEMP: -30° C TO 70° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS



BACKLIGHT CIRCUIT DIAGRAM

深圳市优瑞泰克科技有限公司

PART NO.:	ET035VG05-T			MODULE NO.:	00
DRAWN BY:	LIU	DATE:		PROJECTION:	
CHECKED BY:		DATE:		SCALE:N.T.S	UNIT: mm
APPROVED BY:		DATE:		SHEET: 1 OF 1	

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+60	°C
LCM Storage Temperature	T_{STG}	-30	+70	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.5	2.8	3.6	V
Supply Voltage for(DC/DC)	AVDD	--	--	--	V
Supply Voltage for(DC/DC)	AVEE	--	--	--	V

4.2 Back-Light Unit Characeristics

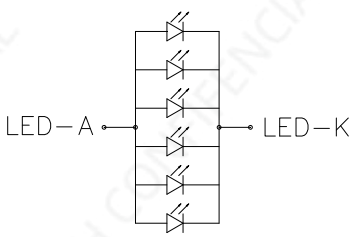
The back-light system is an edge-lighting type with 6 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	2.8	--	3.2	V	--
Forward current	I_F	--	120	--	mA	--
Luminance(With LCD)	Lv	--	750	--	cd/m^2	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	LCM Description
1~2	LEDK	Power supply for backlight cathode input terminal.
3~4	LEDA	Power supply for backlight anode input terminal.
5	NC	NC
6	GND	Power Ground
7	D0N	High speed interface data differential signal input/output pins
8	D0P	High speed interface data differential signal input/output pins
9	GND	Power Ground
10	D1N	High speed interface data differential signal input/output pins
1	D1P	High speed interface data differential signal input/output pins
12	GND	Power Ground
13	CLKN	High speed interface clock differential signal input pins
14	CLKP	High speed interface clock differential signal input pins
15	GND	Power Ground
16	D2N	High speed interface data differential signal input/output pins
17	D2P	High speed interface data differential signal input/output pins
18	GND	Power Ground
19	D3N	High speed interface data differential signal input/output pins
20	D3P	High speed interface data differential signal input/output pins
21~22	GND	Power Ground
23	NC	NC
24	GND	Power Ground
25	TE	Tearing effect output pin is used to synchronize MCU frame writing,
26	RESET	Reset signal input terminal. Active at 'L'.
27	IOVCC(1.8V)	Analog power supply (VCI)：1.65V to 3.3V
28	VDD(2.8V)	Analog power supply (VCI)：2.5V to 3.3V
29~30	GND	Power Ground

6. Timing Characteristics

Case 1: RESX line is held high or unstable by host at power on

If RESX line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied- otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

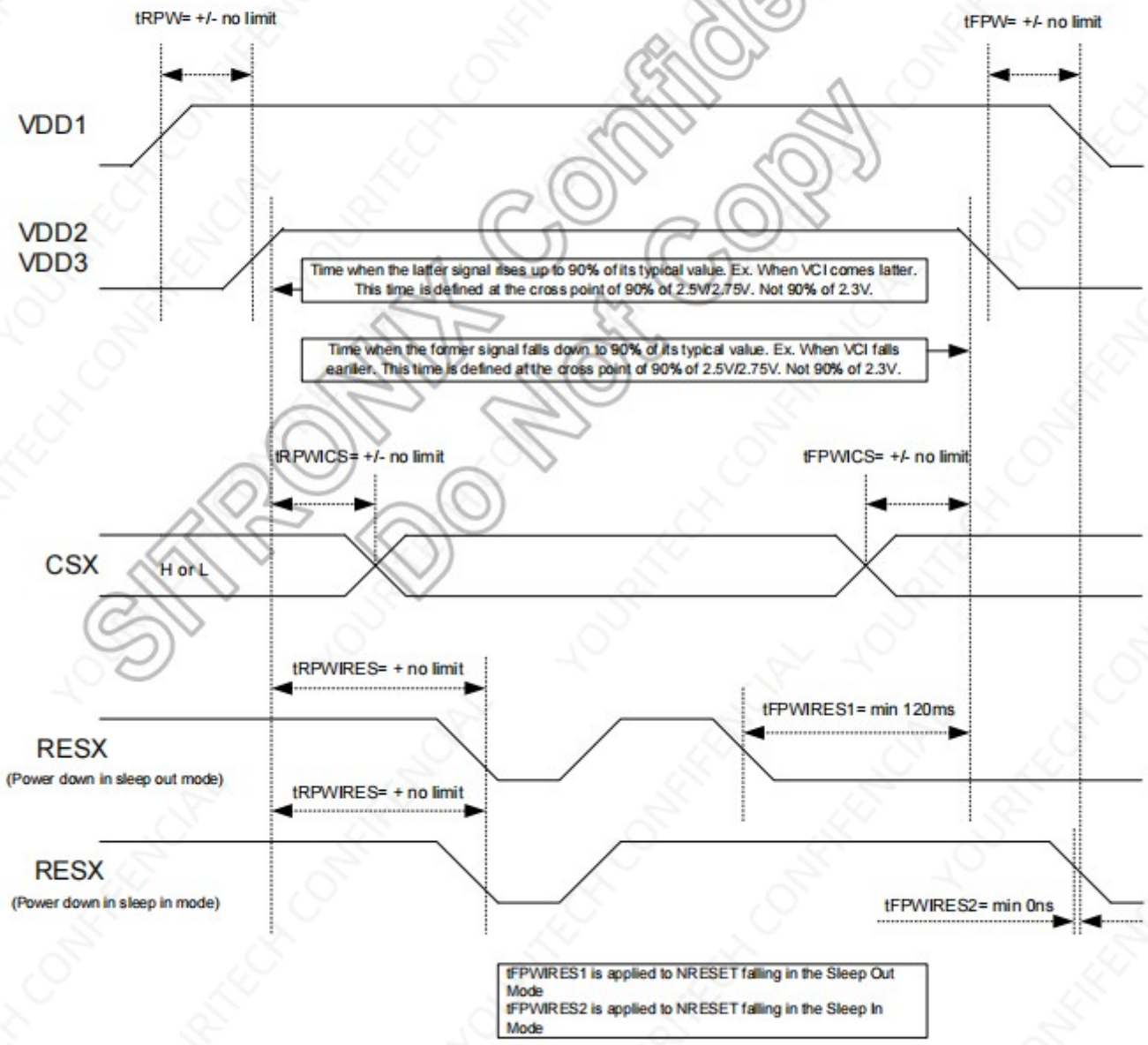


Figure 5.33: Case 1: RESX line is held high or unstable by host at power on

DSI-MIPI Interface Timing Characteristics

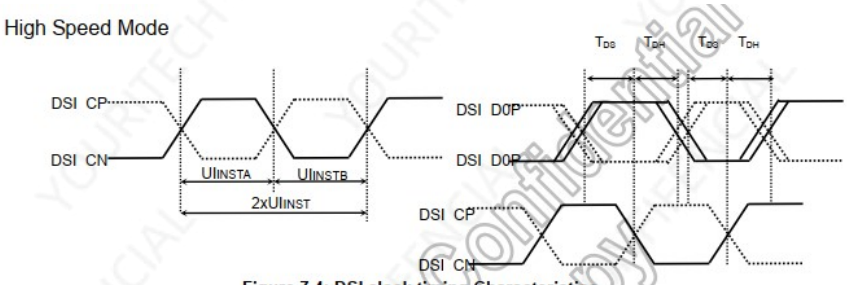


Figure 7.4: DSI clock timing Characteristics

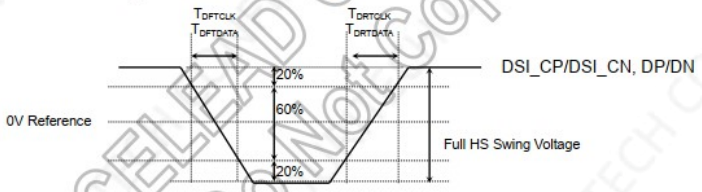


Figure 7.5: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	$2xUI_{INST}$	TBD	-	25	ns
	UI instantaneous	UI_{INSTA} UI_{INSTB}	TBD	-	12.5	ns
DP/DN	Data to clock setup time	T_{DS}	0.15xUI	-	-	ps
	Data to clock hold time	T_{DH}	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	T_{DRTCLK}	150	-	0.3UI	ps
	Differential fall time for clock	T_{DFTCLK}	150	-	0.3UI	ps
DP/DN	Differential rise time for data	$T_{DRTDATA}$	150	-	0.3UI	ps
	Differential fall time for data	$T_{DFTDATA}$	150	-	0.3UI	ps

Table 7.3: DSI High Speed Mode Characteristics

Low Power Mode

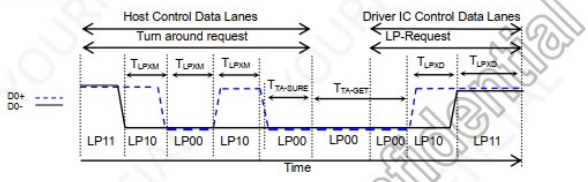


Figure 7.6: BTA from HOST to Display Module Timing

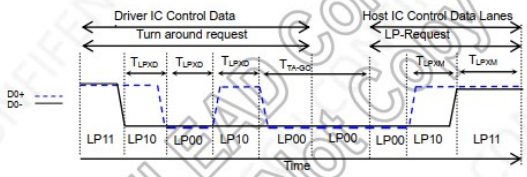


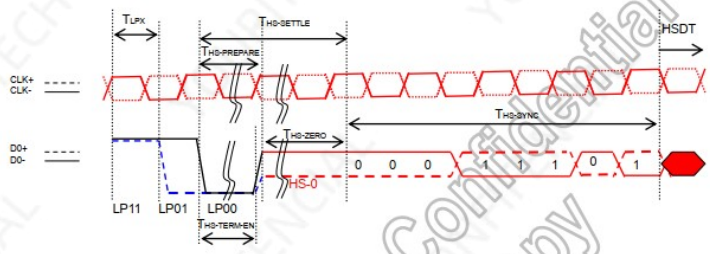
Figure 7.7: BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	$2xT_{LPXD}$	ns
	Time to drive LP-00 by display module	T_{TA-GET}	$5xT_{LPXD}$	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	$4xT_{LPXD}$	-	-	ns

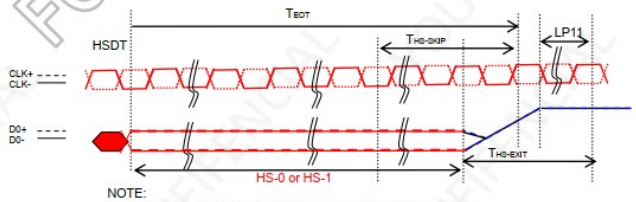
Table 7.4: DSI Low Power Mode Characteristics

DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

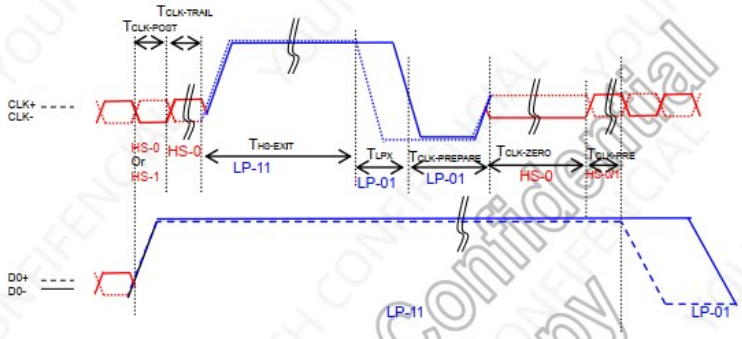
Table 7.5: DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

Table 7.6: DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Table 7.7: Clock Lanes High Speed Mode to/from Low Power Mode Timing

Reset Description:

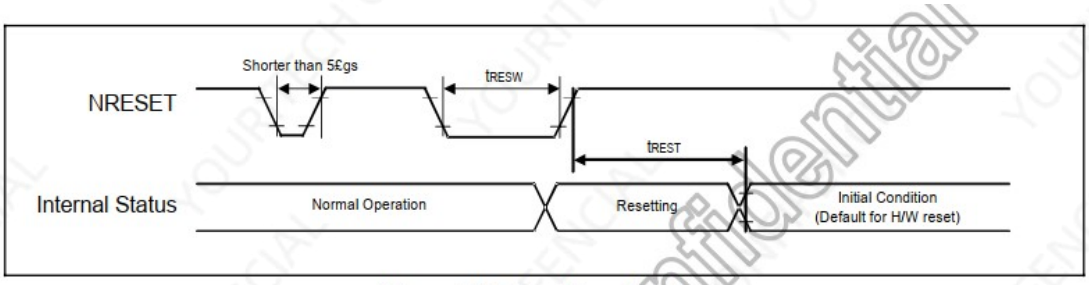


Figure 7.8: Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 7.8: Reset Input Timing

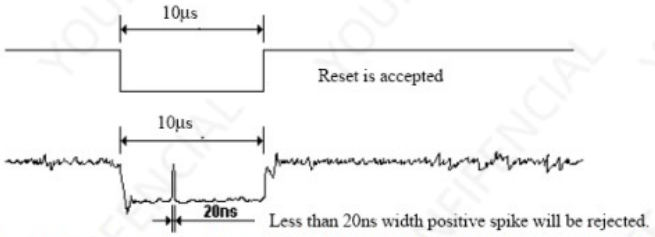
Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 15ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Item	Symbol	Condition	Specification			Unit	Remark
			Min.	Typ.	Max.		
Response time	Tr+Tf	θ= 0°	-	25	50	ms	Note 1,2
Contrast ratio	CR	θ= 0°	600	800	-		Note 1,3
Viewing angle	Top	CR≥10	75	85	-	deg.	Note 1,4
	Bottom		75	85	-		
	Left		75	85	-		
	Right		75	85	-		
Color chromaticity (CF only with C light, CIE 1931)	Wx	θ= 0°	-0.015	0.297	+0.015		Note 1,5,6 CF glass
	Wy		-0.015	0.318	+0.015		
Color Gamut (CF only with C light, CIE 1931)	NTSC	CIE1931	45	50	-	%	Note 1,5,6 CF glass
Trasmittance (with Polarizer)	Trans	θ= 0°	3.7	4.4	-	%	Note 7 Normal POL

Note 1: Measuring Conditions:

The optical characteristics are determined after the unit has been 'ON' and stable at the maximum brightness, in a dark environment at an ambient temperature at 25°C ± 2°C.

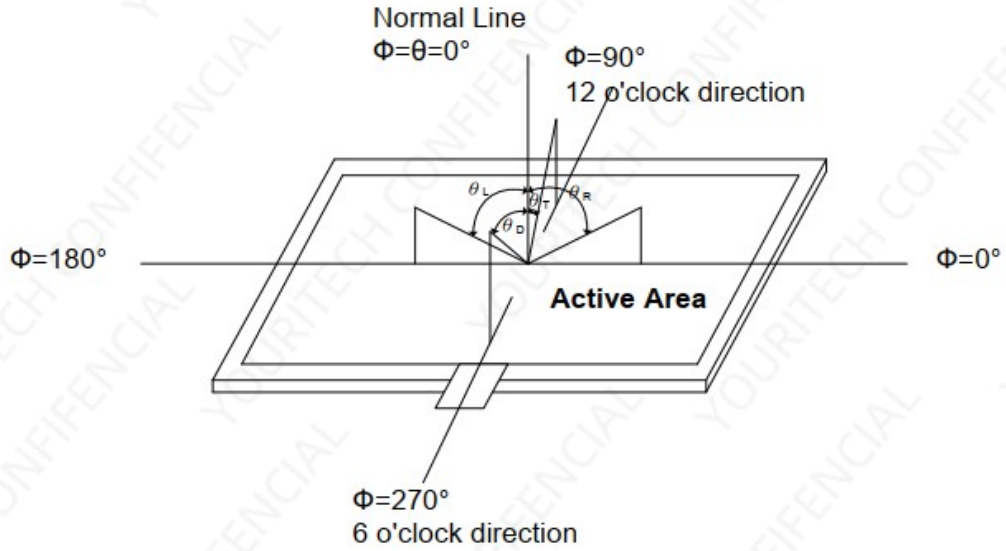
Note 2: Definition of response time:

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time is the time between photo detector output intensity changed from 10% to 90%. And fall time is the time between photo detector output intensity changed from 90% to 10%.

Note 3: Definition of contrast ratio:

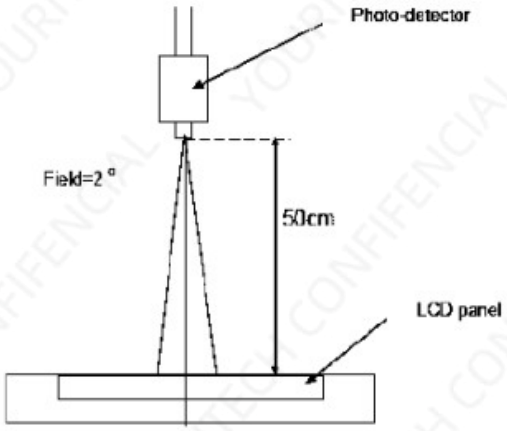
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the " White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 4: Definition of viewing angle



Note 5: Optical characteristic measurement setup.

The LCD module should be stabilized at given temperature for 10 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 10 minutes in a windless room.

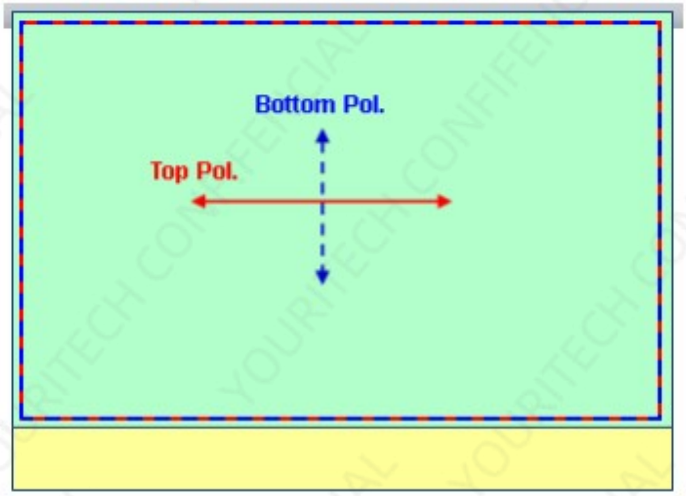


Note 6: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 7: Direction of POL absorption axis

The red and blue arrow directions are meant to be absorption axis.



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+70°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+60°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	60°C x 90%RH / 96H	
6	Thermal and cold shock	Static state，-30℃（30min）~80℃（30min），50 cycles	

9. Packing Method----TBD

- END -