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SPECIFICATION FOR LCM Module

MODULE No:	ET035VG20-K
CUSTOMER:	

YOURITECH	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
2020.10.30	V1.0	ALL	FIRST ISSUE
2021.07.01	V1.1	17,9	Update timing and LCD Optical Characteristics
			S

Contents

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 3.5 " TFT-LCD contains 640x480 pixels, and can display up to 16.7M colors.

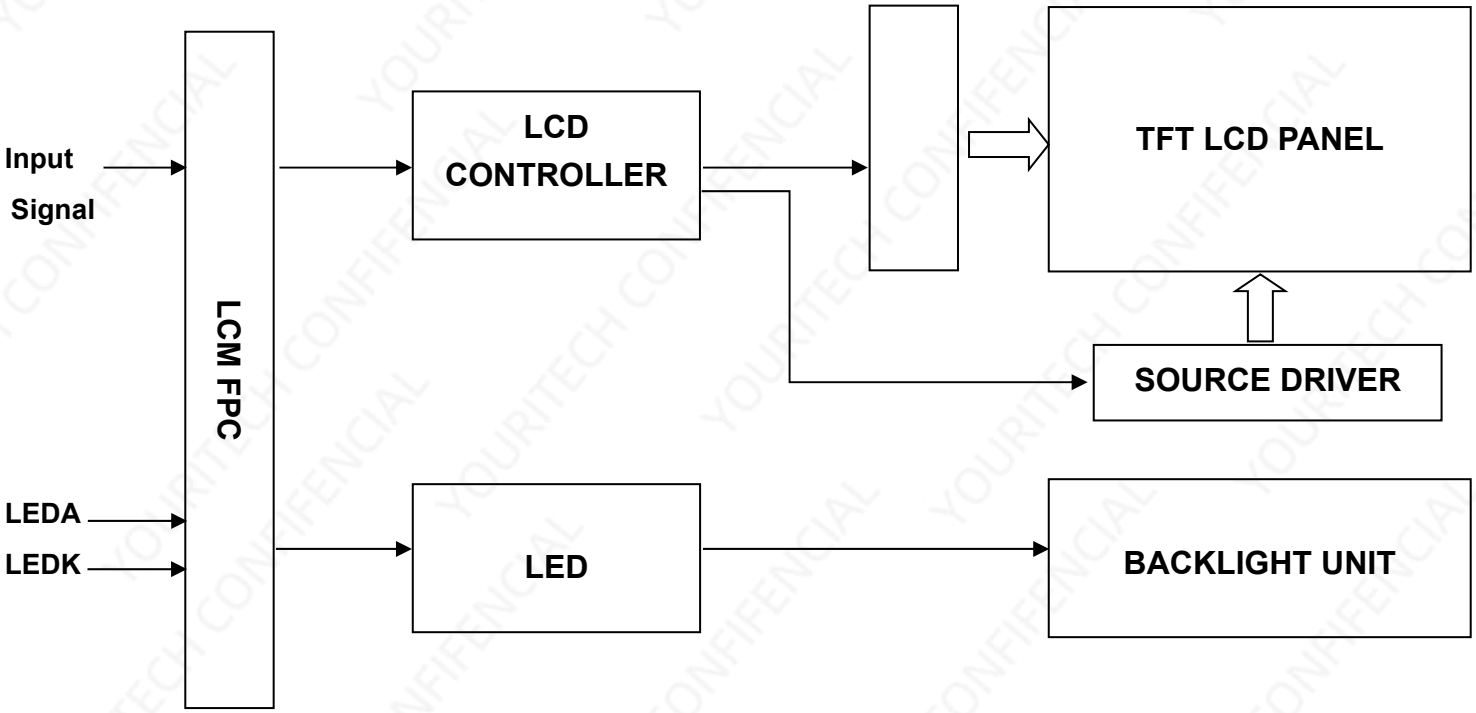
* Features

Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	70.08(H)*52.56(V) (3.5 inch)	mm	
Driver element	TFT active matrix	-	
Display colors	65K/262K/16.7M	colors	
Number of pixels	640(RGB)*480	dots	
Pixel arrangement	RGB vertical stripe	-	
Pixel pitch	0.1095(H)*0.1095(V)	mm	
Viewing angle	Free	o'clock	
Controller IC	NV3052CGRB	-	
LCM Interface	3SPI+16/18/24BIT RGB	-	
Display mode	Transmissive /Normally Black	-	
Operating temperature	-20～+70	℃	
Storage temperature	-30～+80	℃	

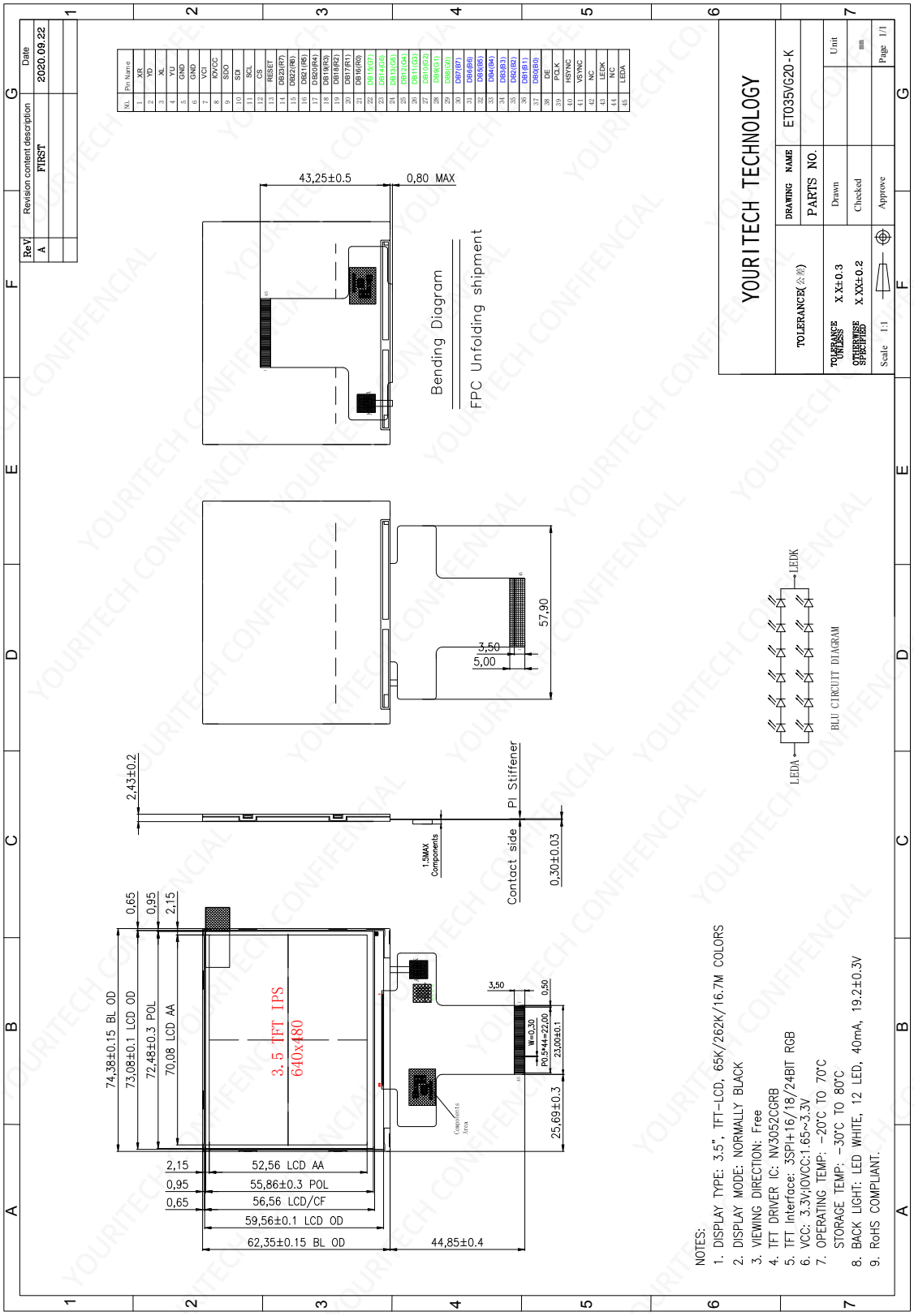
* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	74.38	-	mm	
	Vertical(V)	-	62.35	-	mm	
	Depth(D)	-	2.43	-	mm	
Weight		-	20	-	g	

1. Block Diagram



2. Outline dimension



3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	XR(NC)	Touch panel Right Glass Terminal	A/D
2	YD(NC)	Touch panel Bottom Film Terminal	A/D
3	XL(NC)	Touch panel LIFT Glass Terminal	A/D
4	YU(NC)	Touch panel Top Film Terminal	A/D
5	GND	Ground.	P
6	GND	Ground.	P
7	VCI	Supply voltage (3.3V).	P
8	IOVCC	I/O power supply voltage.	P
9	SDO	SPI interface output pin.-The data is output on the falling edge of the SCL signal.-If not used, let this pin open.	O
10	SDI	Data lane in 1 data lane serial interface. The data is latched on the rising edge of the SCL signal.	I
11	SCL	This pin is used serial interface clock in 3-wire 9-bit serial data interface.	I
12	CS	Chip select input pin (“Low” enable).	I
13	RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.	I
14-37	DB23-DB0	24-bit parallel bi-directional data bus for MCU system and RGB interface mode .Fix to GND level when not in use	I/O
38	DE	Data enable signal for RGB interface peration.	I
39	DOTCLK	Dot clock signal for RGB interface operation.	I
40	HSYNC	Line synchronizing signal for RGB interface operation.	I
41	VSYNC	Frame synchronizing signal for RGB interface operation.	I
42	NC		
43	LEDK	Cathode pin of backlight.	P
44	NC		
45	LEDA	Anode pin of backlight.	P

4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal viewing angle	600	800	--		(1)(2)
Response time	Rising	$T_{R+}T_F$		--	25	50	msec	
	Falling							(1)(3)
Color Gamut		S(%)		45	50	--	%	
Color Filter Chromacicity	White	W_X		0.2706	0.3106	0.3506		(1)(4)
		W_Y		0.2851	0.3251	0.3651		
	Red	R_X		0.5211	0.5611	0.6011		
		R_Y		0.2960	0.3360	0.3760		
	Green	G_X		0.2823	0.3223	0.3623		
		G_Y		0.5012	0.5412	0.5812		
	Blue	B_X		0.1186	0.1586	0.1986		
		B_Y		0.0333	0.0733	0.1133		
Viewing angle	Hor.	ΘL	CR>10	--	85	--		(1)(4)
		ΘR		--	85	--		
	Ver.	ΘU		--	85	--		
		ΘD		--	85	--		
Option View Direction		Free						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding : dark room

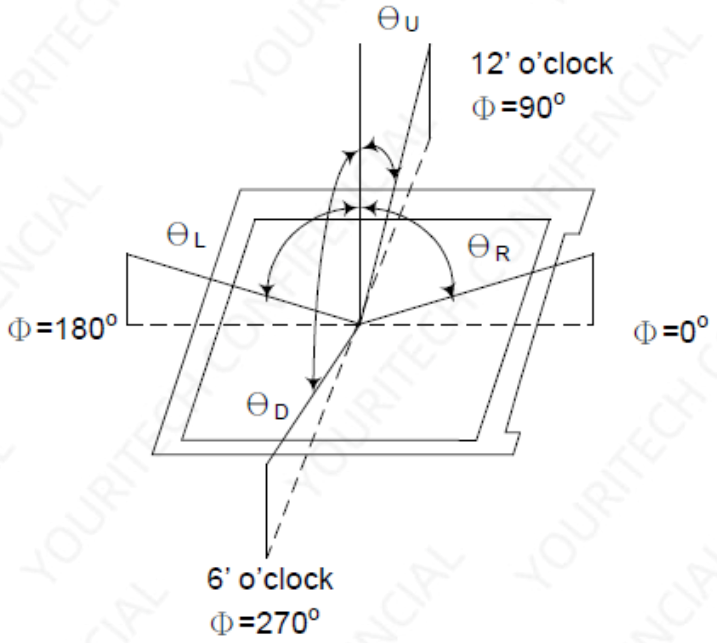
Ambient temperature : 25±2oC

15min. warm-up time.

Measuring Equipment

FPM520 , which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

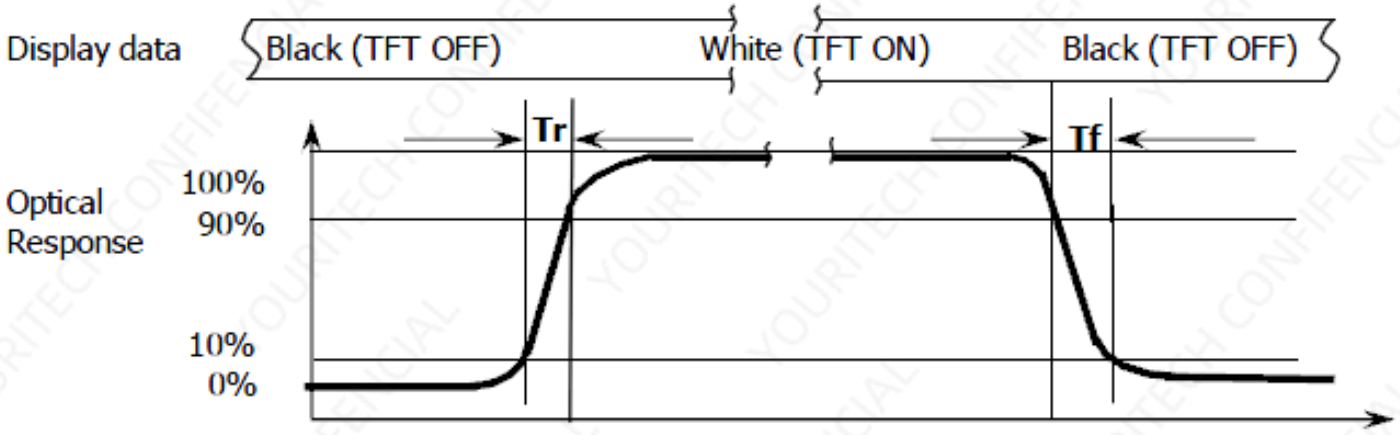
Note (1): Definition of Viewing Angle :



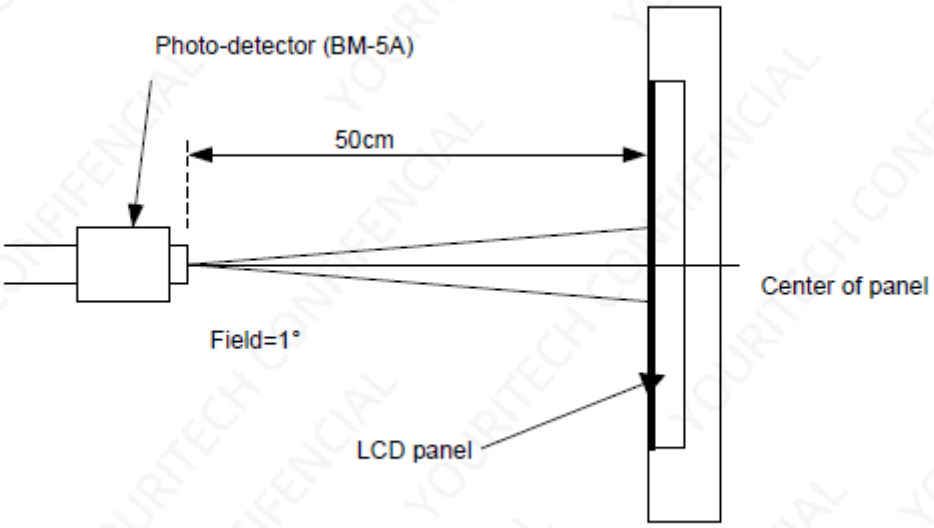
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



5. Electrical Characteristics

5.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VCI	-0.3	6.6	V	Note1
Digital interface supple Voltage	IOVCC	-0.3	4.5	V	Note1
Operating temperature	T_{OP}	-20	+70	℃	
Storage temperature	T_{ST}	-30	+80	℃	

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	3.3	3.6	V	
Digital interface supple Voltage	IOVCC	1.65	1.8	3.6	V	
Normal mode Current	IDD	--	10	20	mA	
Level input voltage	V_{IH}	0.7*IOVCC	--	IOVCC+0.3	V	
	V_{IL}	GND-0.3	--	0.3*IOVCC	V	
Level output voltage	V_{OH}	IOVCC-0.4	--	--	V	
	V_{OL}	GND	--	GND+0.4	V	

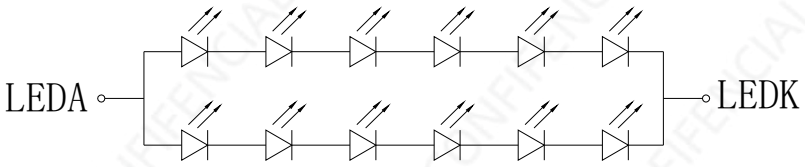
5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 12 chips LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	35	40	--	mA	
Forward Voltage	V_F	--	19.2	--	V	
LCM Luminance	LV	700	750	--	cd/m2	Note3
LED life time	Hr	--	50000	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

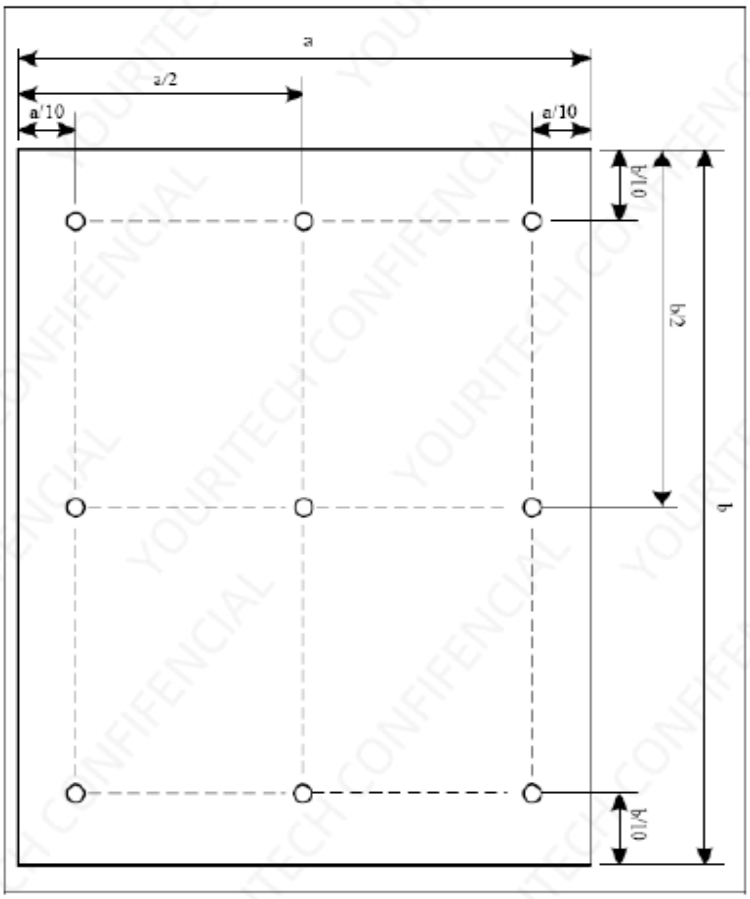
Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.



BLU CIRCUIT DIAGRAM

Note (3) Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

6. AC Characteristics

6.1 Serial interface characteristics (SPI)

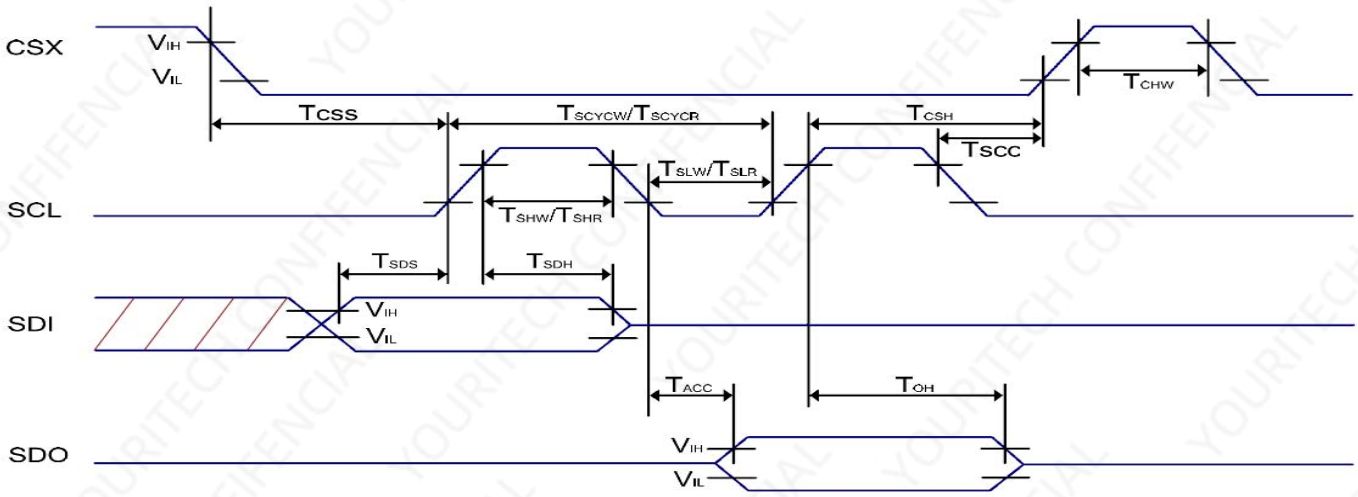


Figure: 3-pin Serial Interface Characteristics

Table: SPI Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	Tcss	Chip select setup time	15	-	ns	-
	Tcsh	Chip select hold time	15	-	ns	
	Tscc	Chip select setup time	20	-	ns	
	Tchw	Chip "H" pulse width	40	-	ns	
SCL	Tscycw	Serial clock cycle (Write)	66	-	ns	-
	Tshw	SCL "H" pulse width (Write)	10	-	ns	
	Tslw	SCL "L" pulse width (Write)	10	-	ns	
	Tscycr	Serial clock cycle (Read)	150	-	ns	-
	Tshr	SCL"H" pulse width (Read)	60	-	ns	
	Tslr	SCL"L" pulse width (Read)	60	-	ns	
SDI	TSDS	Data setup time	10	-	ns	-
	Tsdh	Data hold time	10	-	ns	
	Tacc	Access time	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	Toh	Output disable time	15	50	ns	

Note 1: IOVCC=1.65 to 3.6V, VCI=2.5 to 6V, VSSA=VSS=0V, Ta=-30 to 70℃

Note 2: The rise time and fall time (tr, tf) of input signal is specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

6.2 RGB Interface Selection

The RGB interface is operated with VS, HS, DE, PCLK, D[23:0] lines.It supports several pixel formats that can be selected by dpi [2:0] bits in “Interface Pixel Format (R3Ah)” of Page 0 command. The selection of a given interface is defined by dpi [2:0] as show in the below table.

RGB Interface Selection

dpi[2:0]			RGB Interface Mode	Used Pins
1	0	1	16-bit RGB interface	VS,HS,DE,PCLK,D[20:16],D[13:8],D[4:0]
1	1	0	18-bit RGB interface	VS,HS,DE,PCLK,D[21:16],D[13:8],D[5:0]
1	1	1	24-bit RGB interface	VS,HS,DE,PCLK,D[23:0]
Others			Setting prohibited	

16-bit DPI interface connection:set pixel format DPI[2:0]=3'h5

18-bit DPI interface connection:set pixel format DPI[2:0]=3'h6

24-bit DPI interface connection:set pixel format DPI[2:0]=3'h7

RGB Interface 16/18/24-bit pixel format selection

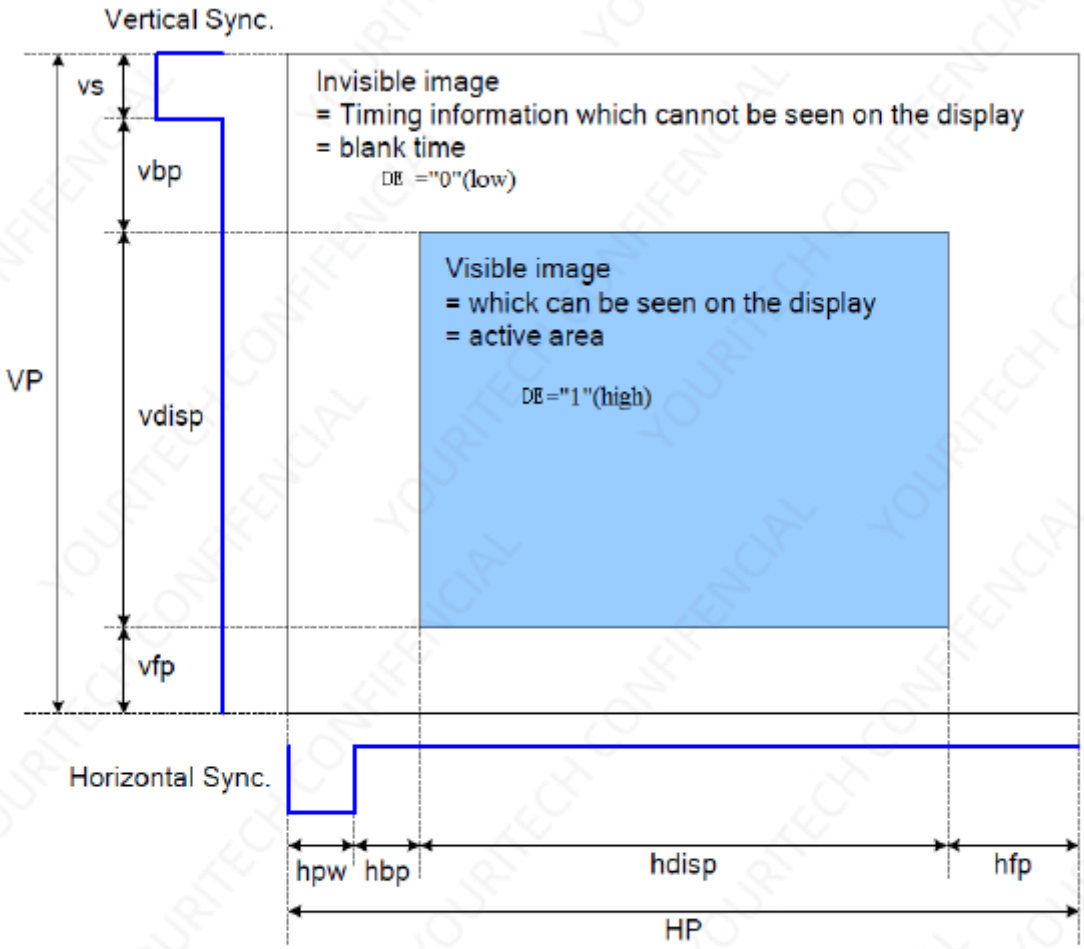
The Pixel clock (PCLK) is running all the time without stopping, it is used for entering VS, HS, DE and D[23:0] states when there is a rising edge of the PCLK. The PCLK can not be used as the internal clock for other functions of the display module.

Vertical sync hronization (VS) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

Horizontal synchroni zation (HS) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the PCLK signal .

DE (Data Enable) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the PCLK signal.

D[23:0] are used to tell what is the information of the image that is transferred on the display(When DE= ’0’ (low) and there is a rising edge of PCLK). D[23:0] can be ‘0’ (low) or ‘1’(high). These lines are read by a rising edge of the PCLK signal.



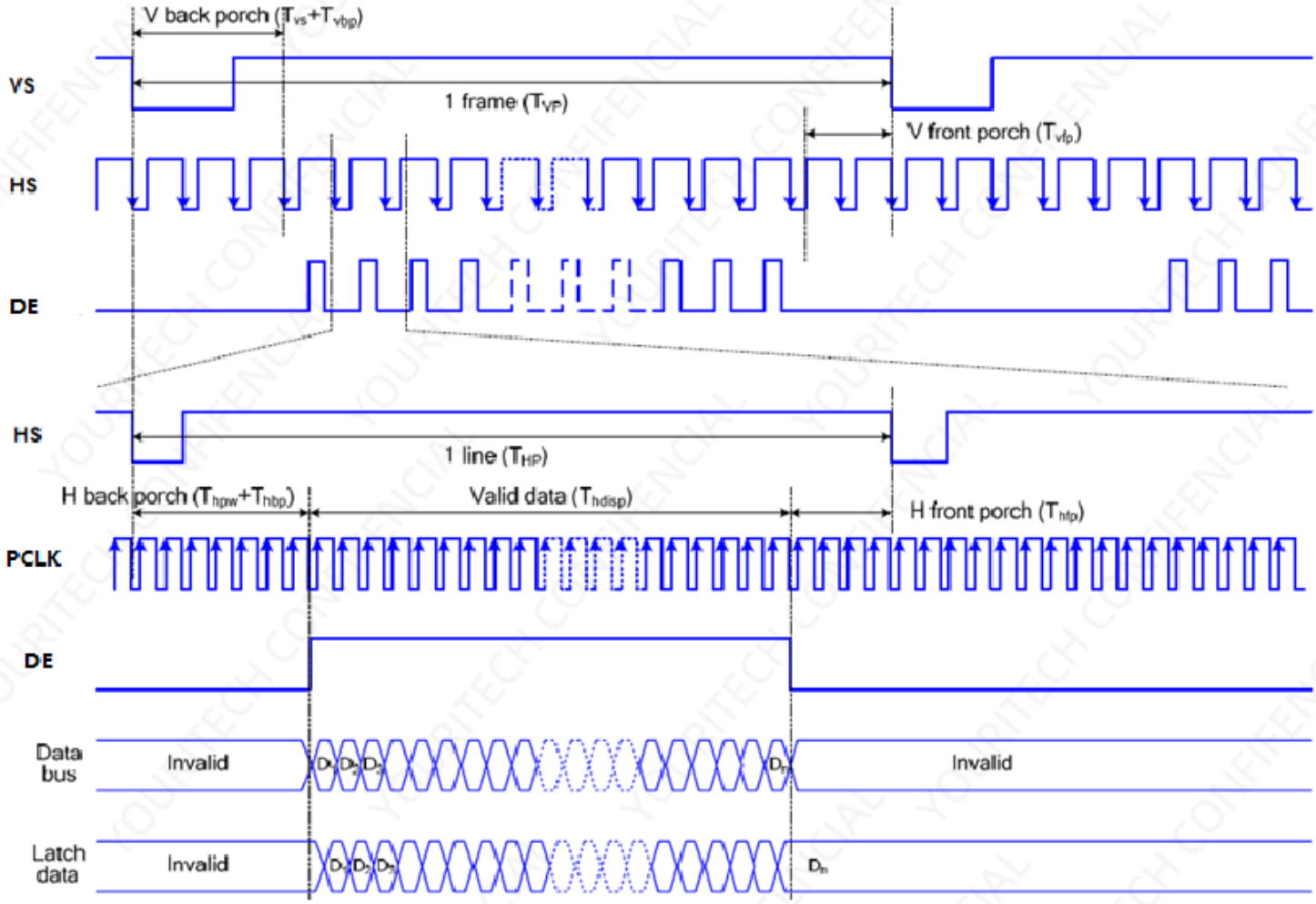
DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	FCLK	--	(21)	--	MHz
Horizontal display area	Hdisp	--	640	--	Clock
Horizontal Sync. Width	hpw	1	4	255	Clock
Horizontal Sync. Back Porch	hbp	1	20	255	Clock
Horizontal Sync. Front Porch	hfp	1	34	--	Clock
Vertical display area	Vdisp	--	480	--	Line
Vertical Sync. Width	vs	1	4	254	Line
Vertical Sync. Back Porch	vbp	1	6	254	Line
Vertical Sync. Front Porch	vfp	1	12	--	Line
Frame-Rate	Fr	--	60	--	Hz

6.3 RGB Interface Timing

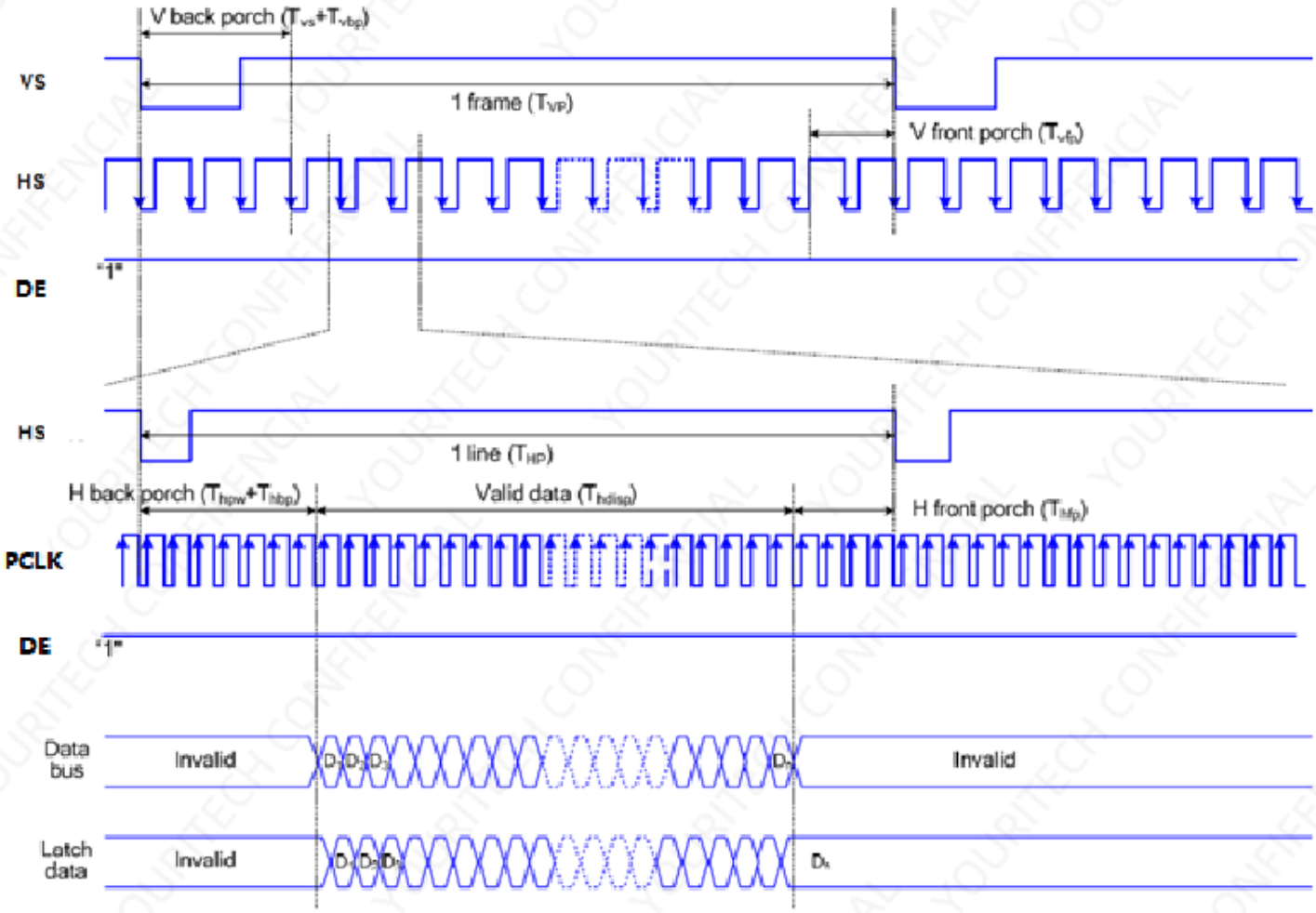
The timing chart of RGB interface DE mode is shown as follows.



Timing Chart of Signals in RGB Interface DE Mode

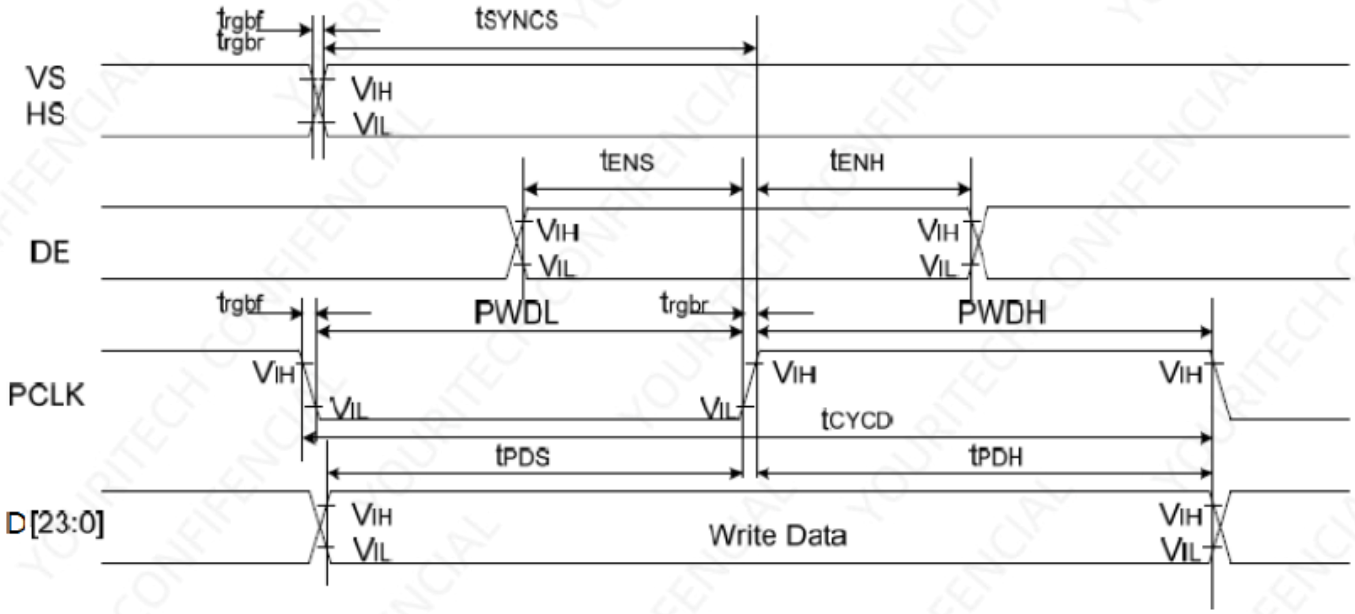
Note: The setting of front porch and back porch in host must match that in IC as this mode.

The timing chart of RGB interface SYNC mode is shown as follows.



Timing chart of RGB interface SYNC mode

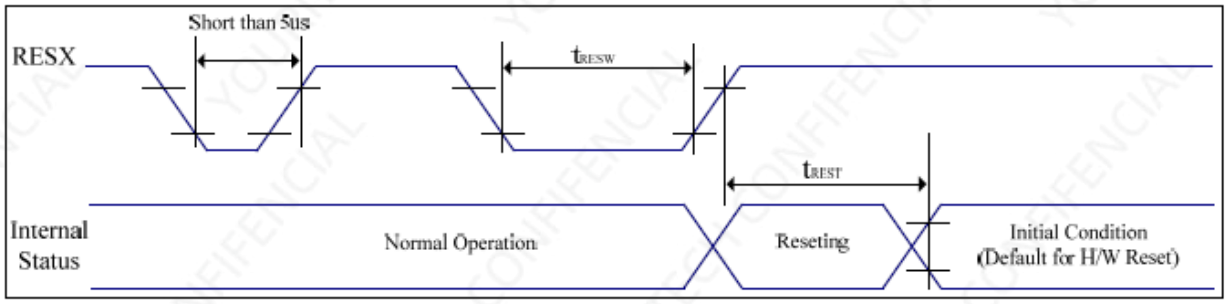
6.4 Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VS/HS	tSYNCS	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	tSYNCH	VS/HS hold time	5	-	ns	
DE	tENS	DE setup time	5	-	ns	
	tENH	DE hold time	5	-	ns	
D[23:0]	tPOS	Data setup time	5	-	ns	
	tPDH	Data hold time	5	-	ns	
PCLK	PWDH	PCLK high-level period	13	-	ns	
	PWDL	PCLK low-level period	13	-	ns	
	tCYCD	PCLK cycle time	28	-	ns	
	trgbr,trgbf	PCLK,HS,VS rise/fall time	-	15	ns	

Note 1: IOVCC=1.65 to 3.6V, VCI=2.5 to 6V, VSSA=VSS=0V, Ta=-30 to 70℃

6.5 Reset timing characteristics



VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V,Ta = -30℃ to 70℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	us
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

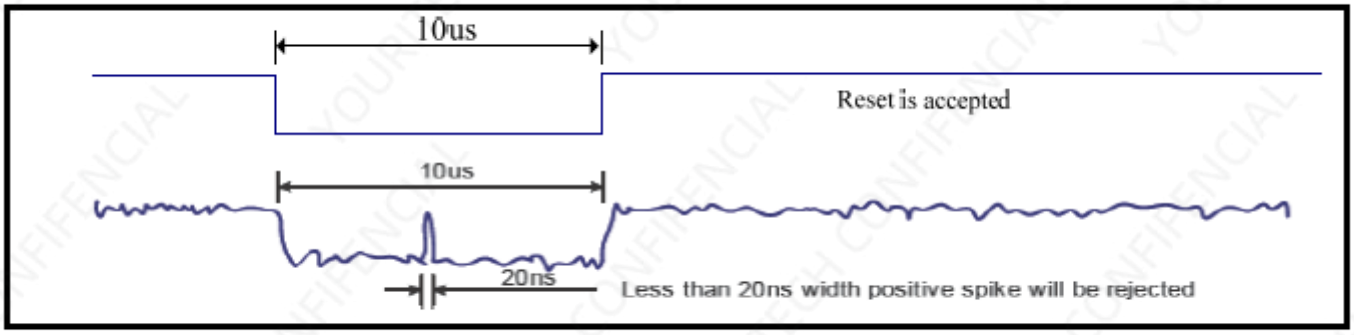
Note 1: Due to an electrostatic discharge on RESX line,spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode) , then return to default condition for H/W reset.

Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time (Trest) which lasted 5ms..The loading operation will be done every time during this reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

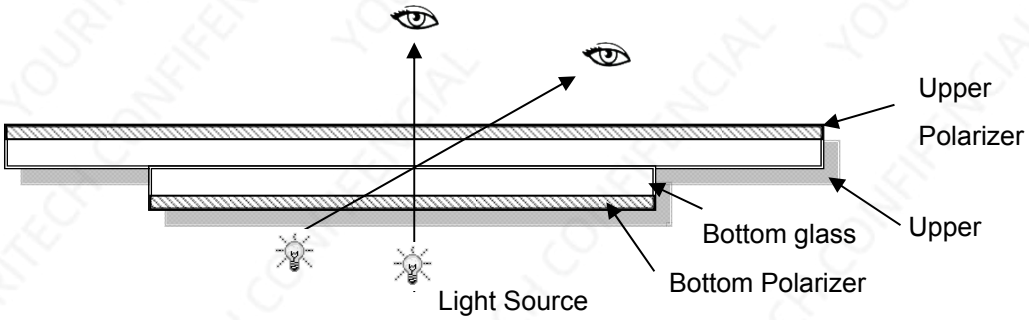
Temperature : 25±5℃

Humidity : 65%±10%RH

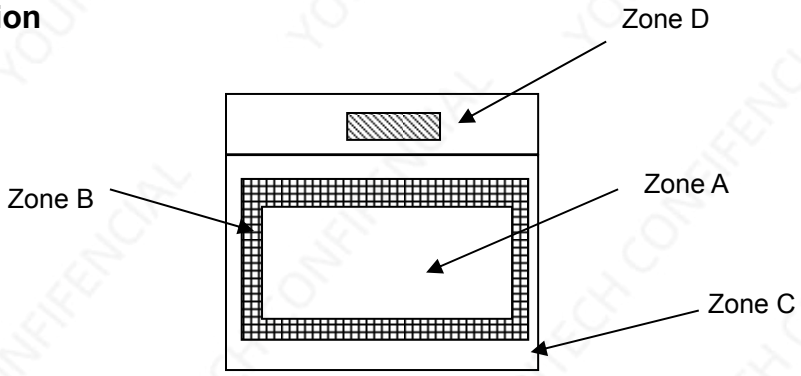
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ

AQL:

Major defect	Minor defect
0.65	1.5

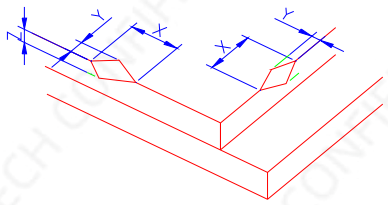
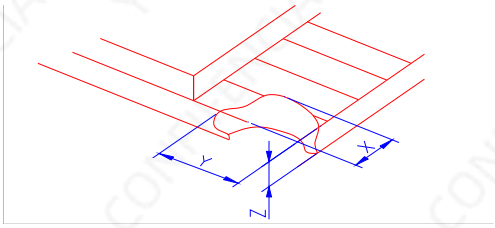
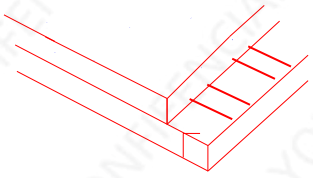
LCD: Liquid Crystal Display , LCM: Liquid Crystal Module,

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc…	Major
2	Missing	Missing components and etc…	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed,deformation and etc…	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot,Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

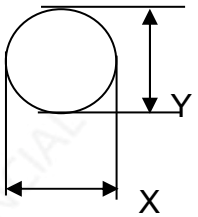
Note1: a) Light dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

7.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0 Spot defect



Φ=(X+Y)/2

① light dot（ black/white spot , pinhole, stain，etc.）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧10mm)		
0.25<Φ≤0.4	2(distance≧10mm)		
Φ>0.4	0		

② Dim spot（light leakage、dent、dark spot，etc）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧10mm)		
0.25<Φ≤0.4	2(distance≧10mm)		
Φ>0.4	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance≧10mm)		
Φ>0.5	0		

④Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	3(distance≧10mm)		
Φ>0.4	0		

3.0	LCD Pixel defect	Pixel bad points

Item	Zone A	Acceptable Qty
Bright dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Dark dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm
Total bright and dark dot		N≤4

Note:

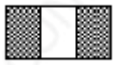
A) Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

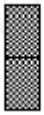
C) 2 dot adjacent = 1 pair = 2 dots

Picture:

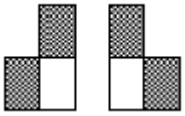
2 dot adjacent



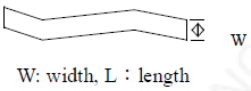
2 dot adjacent



2 dot adjacent (vertical)



2 dot adjacent (slant)

<table>
<tr>
<td>4.0</td>
<td>Line defect (LCD /Polarizer backlight black/white line, scratch, stain)
 

W: width, L：length
N：Count</td>
<td>
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Length(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤4.0</td><td colspan="2">N≤3</td></tr>
<tr><td>0.06<W≤0.08</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>W>0.08</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td>
</tr>
<tr>
<td>5.0</td>
<td>Electronic Components SMT.</td>
<td>Not allow missing parts，solderless connection，cold solder joint，mismatch，The positive and negative polarity opposite</td>
</tr>
<tr>
<td>6.0</td>
<td>Display color& Brightness.</td>
<td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td>
</tr>
<tr>
<td>7.0</td>
<td>LCD Mura/Waving/ Hot spot</td>
<td>Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.</td>
</tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

8. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20℃, 96HR	
High Temperature Storage	80℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Operating	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-30℃,30 min ↔ +80℃,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

Remark:

1.The test samples should be applied to only one test item.

2.Sample size for each test item is 5~10pcs.

3.For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.

4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.