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Project No. 项目编号	ET037VG06-T
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	**Standard LCD Module** **TFT：240*RGBx960Dots** **3.71”TFT LCD**

客户确认Customer Approval	
项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	

PREPARED BY	CHECKED BY	APPROVED BY

1. Introduction

1.1 Scope of application

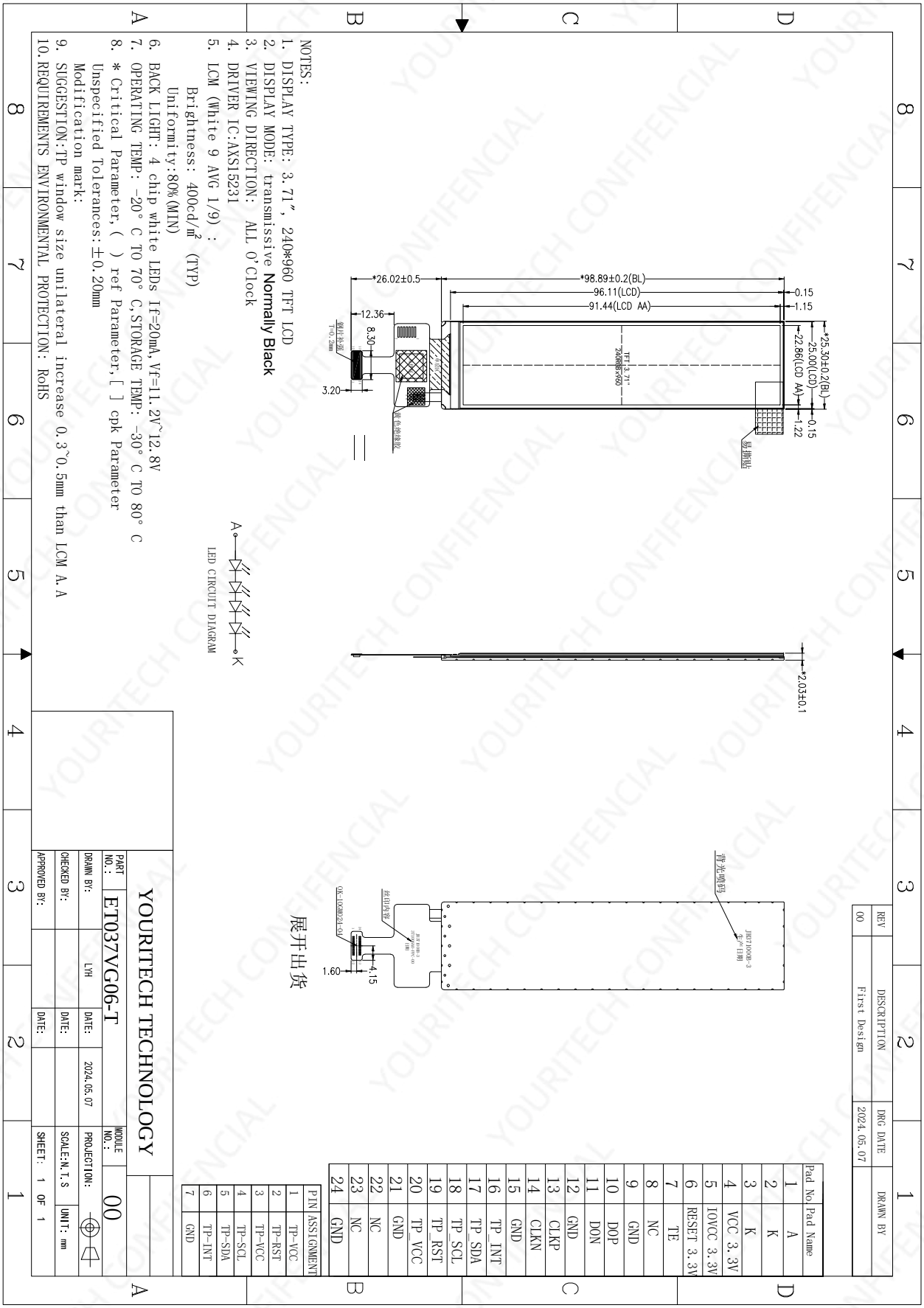
This specification applies to the LCD module that is supplied by YOURITECH TECHNOLOGY.
LCD specification: Dots 240xRGBx960.
As to basic specification of the driver IC, refer to the IC (AXS15231) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;
IPS Type LCD
240dot-segment and 960 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
1lane MIPI interface

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	240*3RGB(H)X960(V)	Dots
Pixel arrangement	RGB stripe	--
Pixel Pitch (W*H)	0.09525(W) × 0.09525 (H)	mm
Active area	22.86(W) × 91.44(H)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	AXS15231	--
TFT interface	1lane MIPI interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	25.30(W) ×98.89(H) ×2.03(T)	mm
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--



NOTES:
1. DISPLAY TYPE: 3.71", 240*960 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL O'Clock
4. DRIVER IC:AXS15231
5. LCM (White 9 AVG 1/9) :
   Brightness: 400cd/㎡ (TYP)
   Uniformity:80%(MIN)
6. BACK LIGHT: 4 chip white LEDs If=20mA, Vf=11.2V~12.8V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter, ( ) ref Parameter, [ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS

LED CIRCUIT DIAGRAM

Pad No.	Pad Name
1	A
2	K
3	K
4	VCC 3.3V
5	IOVCC 3.3V
6	RESET 3.3V
7	TE
8	NC
9	GND
10	DOP
11	DON
12	GND
13	CLKP
14	CLKN
15	GND
16	TP_INT
17	TP_SDA
18	TP_SCL
19	TP_RST
20	TP_VCC
21	GND
22	NC
23	NC
24	GND

PIN	ASSIGNMENT
1	TP-VCC
2	TP-RST
3	TP-VCC
4	TP-SCL
5	TP-SDA
6	TP-INT
7	GND

REV	DESCRIPTION	DRG DATE	DRAWN BY
00	First Design	2024.05.07	

YOURITECH TECHNOLOGY

PART NO.:	ET037VG06-T	MODULE NO.:	00
DRAWN BY:	LYH	DATE: 2024.05.07	PROJECTION:
CHECKED BY:		DATE:	SCALE:N.T.S UNIT: mm
APPROVED BY:		DATE:	SHEET: 1 OF 1

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.8	3.3	3.3	V
Supply Voltage for(DC/DC)	VDD	2.8	3.3	3.3	V

4.2 Back-Light Unit Characeristics

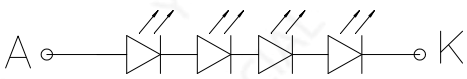
The back-light system is an edge-lighting type with 4 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	11.2	--	12.8	V	--
Forward current	I_F	--	20	--	mA	--
Luminance(With LCD)	Lv	--	400	--	cd/m^2	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	LCM Description
1	LEDA	Power supply for backlight anode input terminal.
2	LEDK	Power supply for backlight cathode input terminal.
3	LEDK	Power supply for backlight cathode input terminal.
4	VDD_3.3V	Power Supply For LCD.
5	IOVCC_3.3V	Power Supply For LCD.
6	RST_ 3.3V	Reset signal input terminal. Active at 'L'.
7	TE	Frame head pulse for tearing effect.
8	NC	No Connection.
9	GND	Power Ground
10	D0P	Positive polarity of low voltage differential data 0 signal
11	D0N	Negative polarity of low voltage differential data 0 signal
12	GND	Power Ground
13	CLKP	Positive polarity of low voltage differential clock signal
14	CLKN	Negative polarity of low voltage differential clock signal
15	GND	Power Ground
16	CTP_INT	Interrupt signal
17	CTP_SDA	Touch panel I2C data
18	CTP_SCL	Touch panel I2C clock
19	CTP_RST	Touch panel reset
20	CTP_VCC	Touch panel Power supply 2.8~3.3V
21	GND	Power Ground
22	NC	No Connection.
23	NC	No Connection.
24	GND	Power Ground

6. Timing Characteristics

Normal Power On/Off Se quence

VDDI and VCI can be applied in any order. VDDIand VCI can be powered down in any order. In a MCU system, VDDI is typically generated from VCI by a DC-DC or LDO converter. So generally speaking, VDDI is powered up after the VCI.

During power off, if LCD is in the Sleep Out mode, VDDI and VCI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

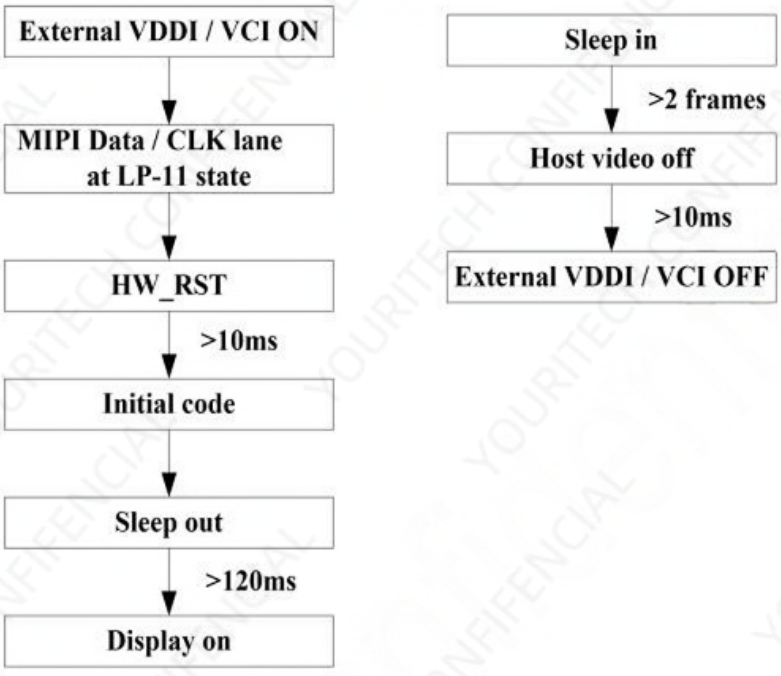
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

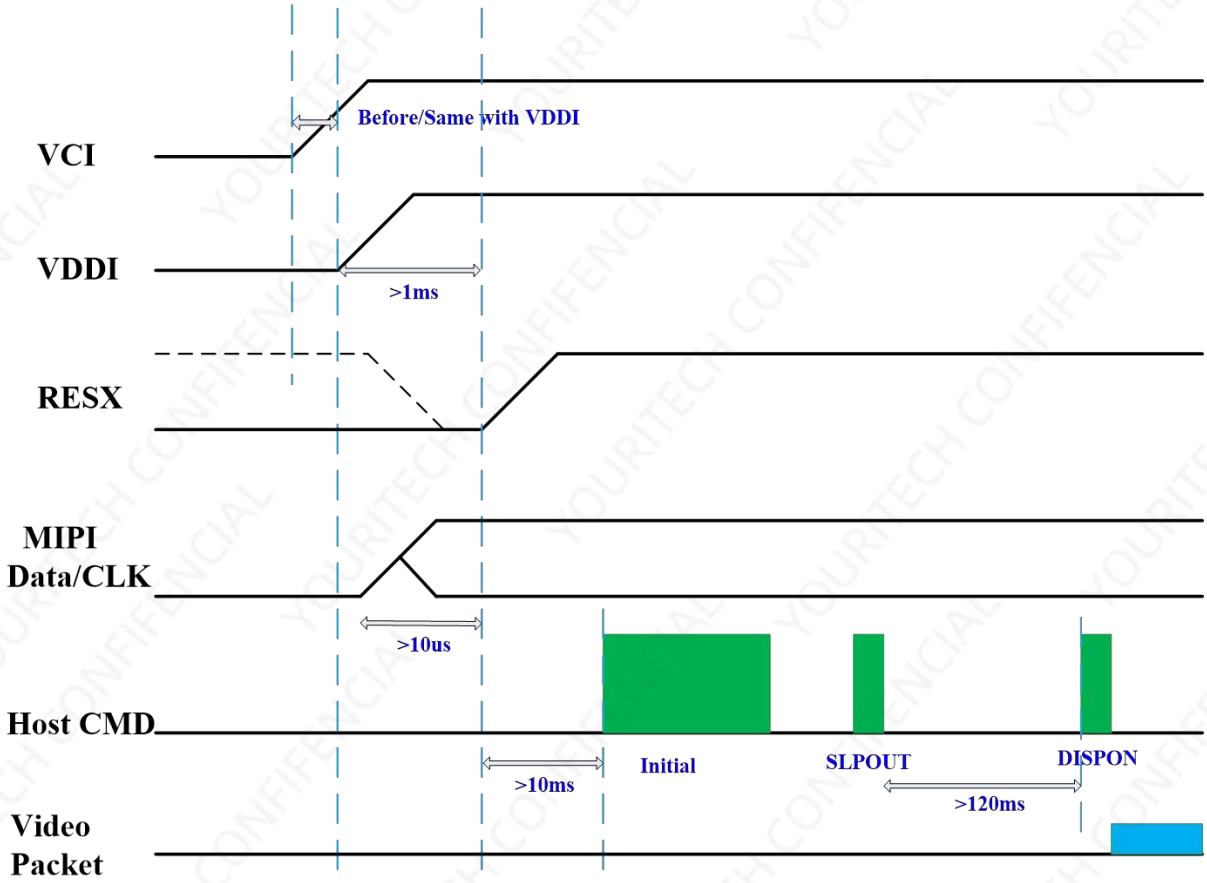
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command.

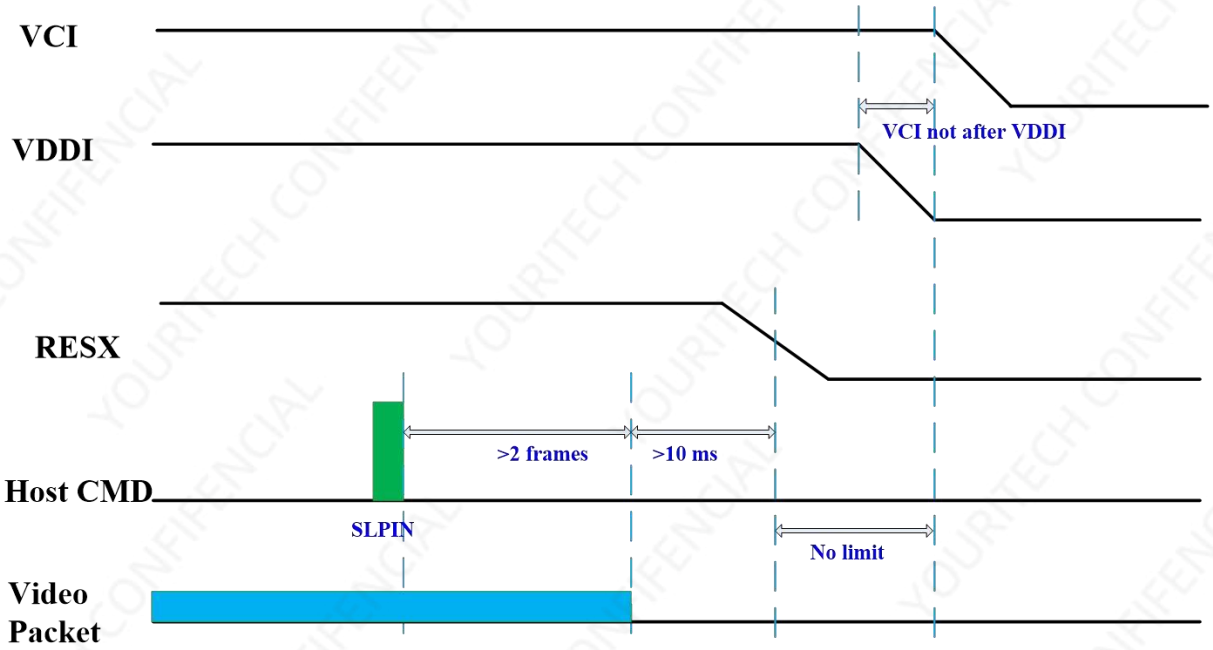
Also, between receiving Sleep In command and Power Off Sequence. If RESX line is not held stable by host during Power On Sequence, then it will be necessary to apply a Hardware Reset (RESX)

after Host Power On Sequence is complete to ensure correct operation. Otherwise, function is not guaranteed.

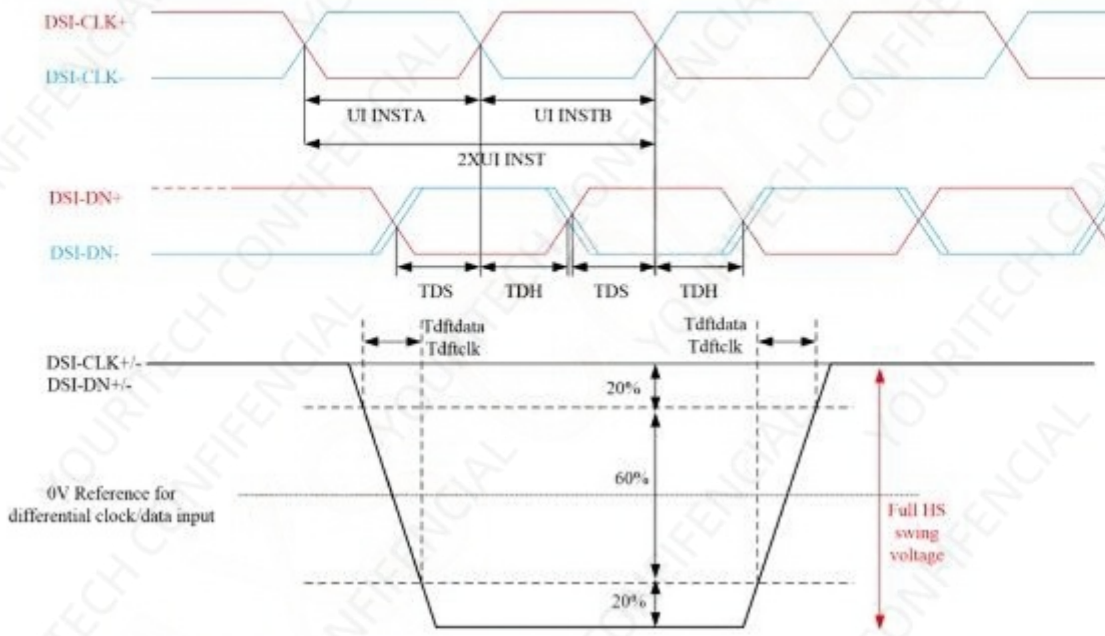
The power on/off sequence is illustrated below:




VCI
Before/Same with VDDI
VDDI
>1ms
RESX
MIPI
Data/CLK
>10us
Host CMD
>10ms
Initial
SLPOUT
DISPON
>120ms
Video
Packet


VCI
VCI not after VDDI
VDDI
RESX
>2 frames
>10 ms
Host CMD
SLPIN
No limit
Video
Packet

High speed mode



Parameter	Symbol	Parameter	Specification			Unit	Description
			MIN	TYP	MAX		
DSI-CLK+/-	2xUIINSTA	Double UI instantaneous	4		25	ns	
DSI-CLK+/-	UIINSTA UIINSTB	UI instantaneous halfs	2		12.5	ns	UI=UIINSTA-UIINSTB
DSI-D0+/-	TDS	Data to clock setup time	0.15	-		UI	
DSI-D0+/-	TDH	Data to clock hold time	0.15	-		UI	

Figure: AC characteristics for MIPI-DSI High speed mode

Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power Mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP -11 periods MPU Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP -11 periods Display Module MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T LPXD	-	2XT LPXD	ns
DSI-D0+/-	$T_{TA-GETD}$	Time to driver LP-00 by display module	5XT LPXD	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to driver LP-00 after turnaround request - MPU	4XT LPXD	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	

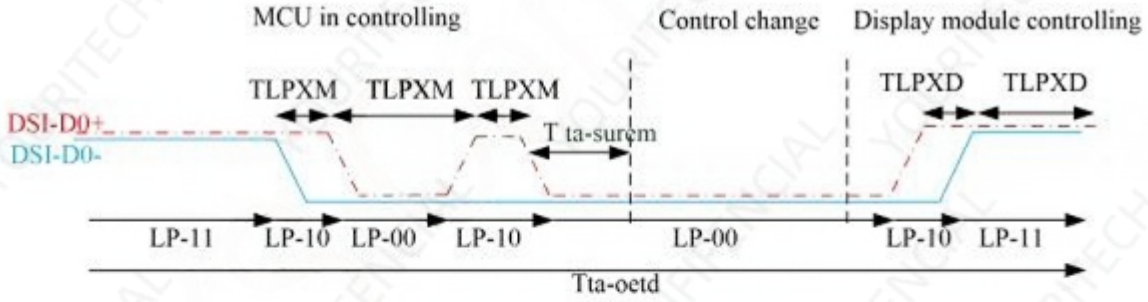


Figure: BTA from the MCU to the Display Module

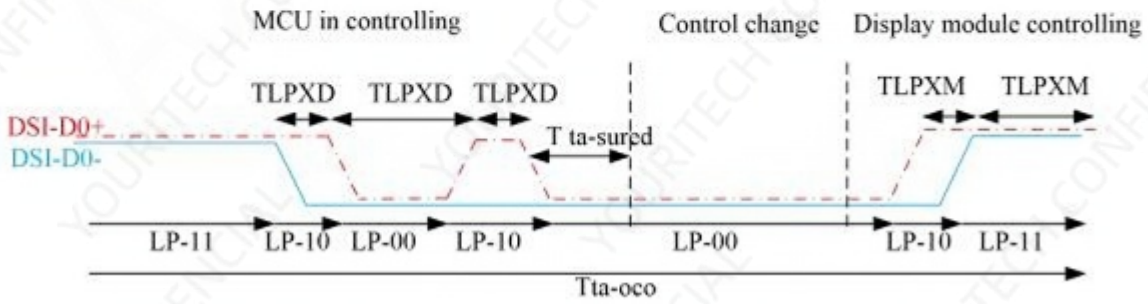


Figure: BTA from the Display Module to the MCU

Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to driver LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to driver HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lanereceiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to driver flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ Period to start of LP-11 state	-	-	105ns +12UI	ns

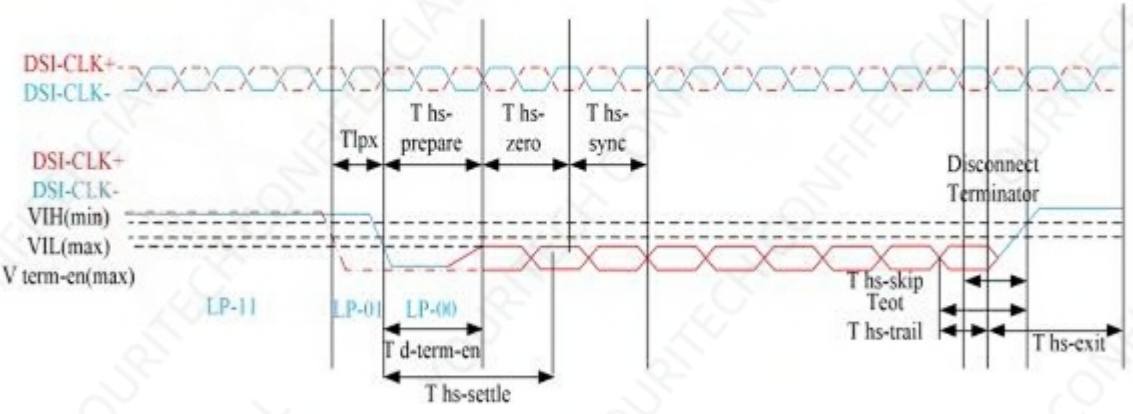


Figure: High Speed Data Transmission Bursts

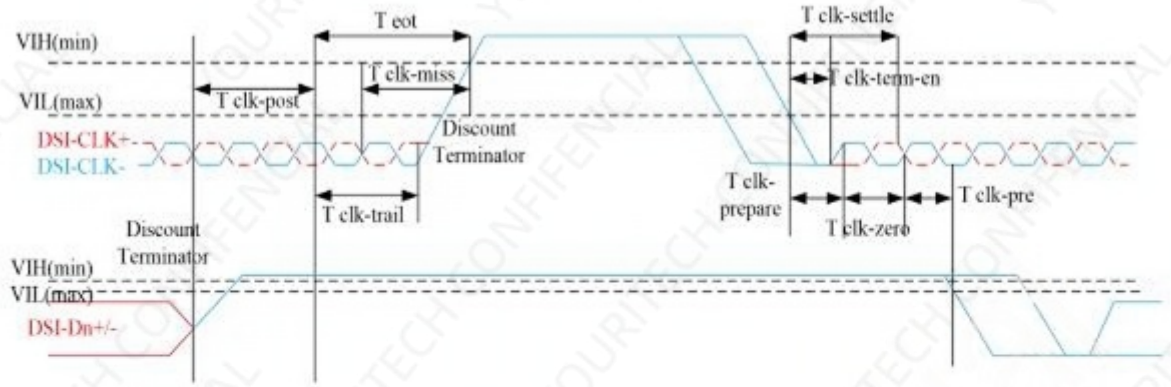


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lanehas transitioned to LP mode	60ns + 52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be drivern prior to any associated Data Lanebeginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to driver LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time to enable Clock Lanereceiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$+ time for lead HS-0 driver period before starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to driver HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK-TRAIL}$ periodto start of LP-11 state	-	-	105ns + 12UI	ns

LP-11 between High Speed and Low Power Modes

DSI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-11) when

different combinations, what are listed below, are possible:

1. High Speed Mode => Stop State (SS, LP-11) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-11) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-11) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-11) => Low Power Mode

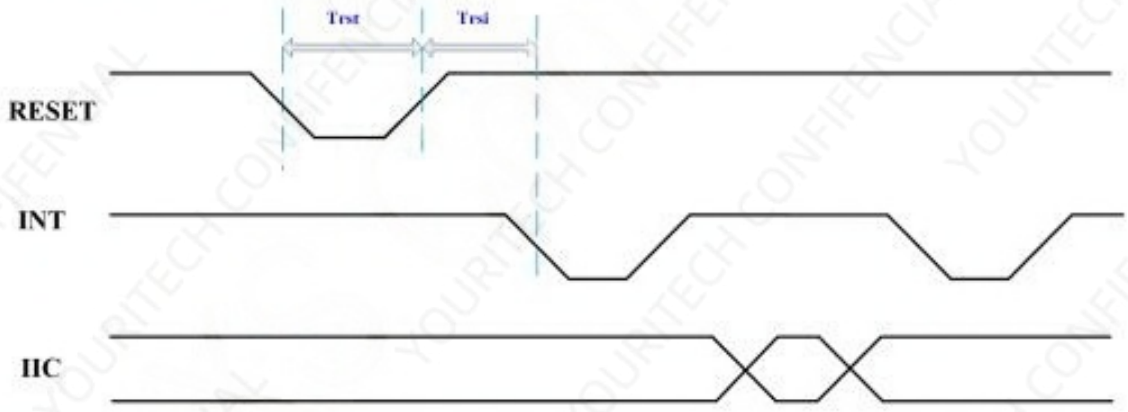
The Low Power Mode is also including 2 different functions:

1. Escape
2. Bus Turnaround (BTA)

Stop State (SS, LP-11) Timings from Previous mode to Next mode

Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100ns	-	100ns	-	100ns	-
HSDT	60ns+52UI	-	60ns+52UI	-	60ns+52UI	-
BTA	100ns	-	100ns	-	100ns	-

Reset time must be enough to guarantee reliable reset.



Parameter	Description	Min	Max	Units
Trsi	Time of starting to report point after resetting	200	--	ms
Trst	Reset time	5	--	ms

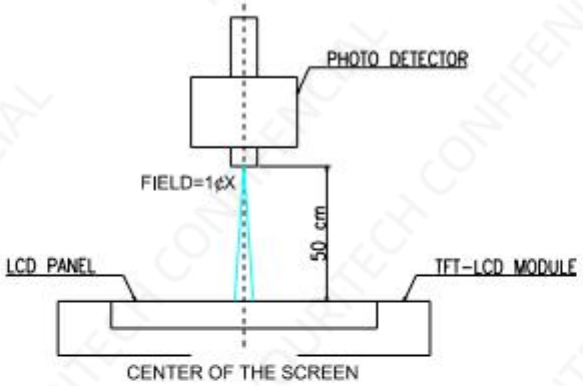
7.Optical Characteristics

All optical specification was simulated under typical condition (Note 1, 2), AUO will probably amend the data, when the actual Products output.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time		Tr+Tf	θ=0° Φ=0°	--	25	35	ms	Note 3
Contrast ratio		CR	At optimized viewing	1000	1500	--	--	Note 4
NTSC		%	θ=0°	56	61	--	%	Base on C-light
Viewing Angle	Top		CR ≧10	70	80	--	deg.	Note 5
	Bottom							
	Left							
	Right							
Transmittance		%	θ=0°	3.25	3.7		%	Base on Silicate_穗晶_UK1 BLU w/o:APF&BSITO&Haze
Crosstalk	%	25℃		--	--	2.5	%	Note 7 Base on Optimal Initial code
Chromaticity	White	Wx	θ=0°	0.292	0.312	0.332		Base on C-light
		Wy	θ=0°	0.347	0.367	0.387		
	Red	Rx	θ=0°	0.621	0.641	0.661		
		Ry	θ=0°	0.323	0.343	0.363		
	Green	Gx	θ=0°	0.257	0.277	0.297		
		Gy	θ=0°	0.575	0.595	0.615		
	Blue	Bx	θ=0°	0.112	0.132	0.152		
		By	θ=0°	0.143	0.163	0.183		

Note 1: Measured under Ambient temperature =25℃±2℃ in the dark room.

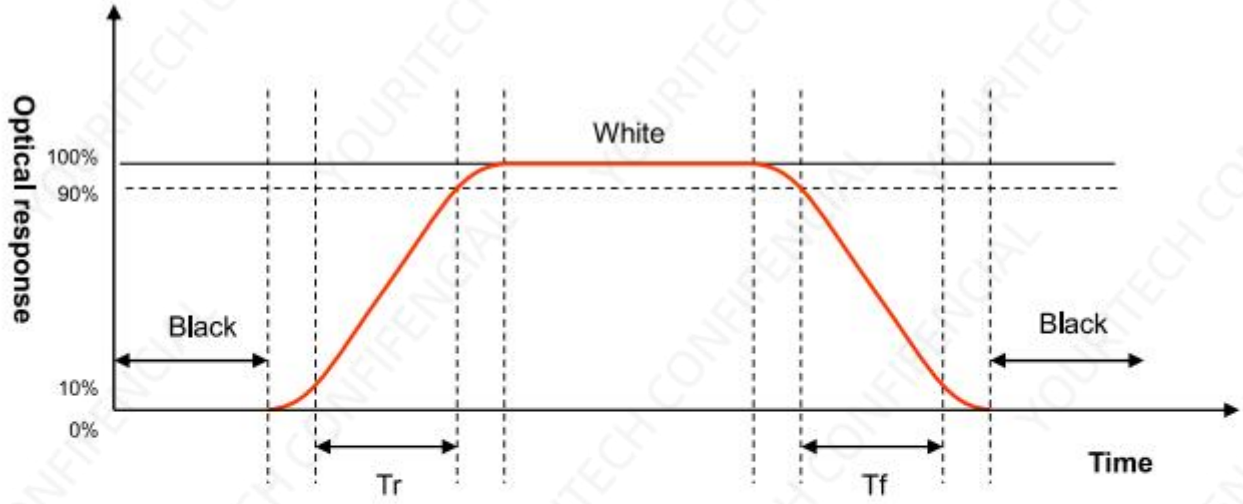
Note 2: To be measured on the center area of panel with a viewing cone of 1° by luminance meter, after 15 minutes operation.



Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (rising time) and from "white" to "black" (falling time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

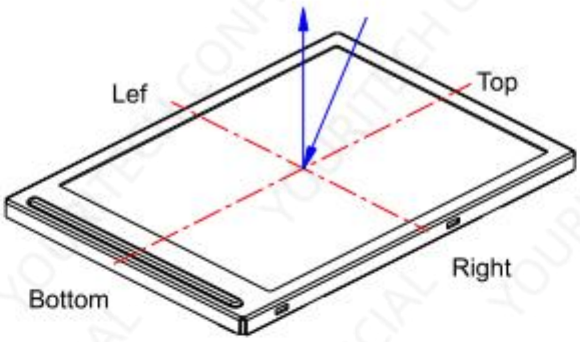


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

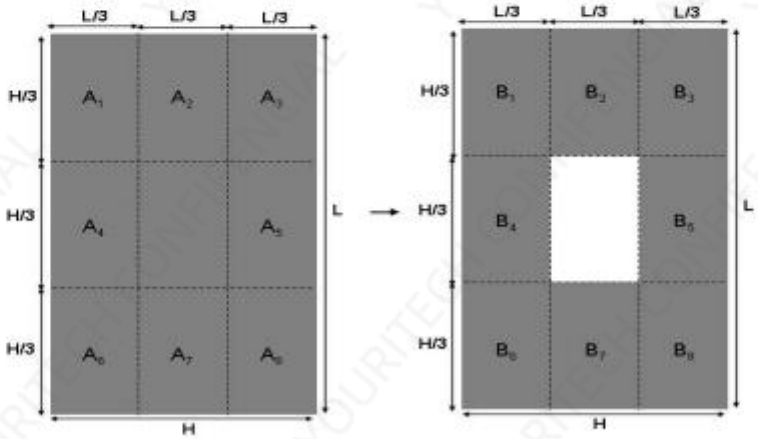
Note 5. Definition of viewing angle, θ, Refer to figure as below.



Note 6: The spec in table is for reference, different polarizer and APCF would make different performance for it. Transmitace will be adjusted 1st Sample

Note 7: Cross-talk ratio is measuring by follow pattern and formula

The test pattern of cross-talk is 128L gary around one white block, size is defined as picture.



$$\text{Cross talk Ratio} = \max_{i=1 \text{ to } 8} \frac{|A_i - B_i \text{ (Photo detector output when LCD is at test pattern)}|}{A_i \text{ (Photo detector output when LCD is at 128L gray pattern)}}$$

Note 8: Gamma value will be based on initial code.

8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	60°C x 90%RH / 96H	
6	Thermal and cold shock	Static state，-20℃（30min）~70℃（30min），10 cycles	