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Project No. 项目编号	ET039HV01-T
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	**Standard LCD Module** **TFT：320*RGBx320Dots** **3.92”TFT LCD**

客户确认Customer Approval	
项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	

PREPARED BY	CHECKED BY	APPROVED BY

1.1 Scope of application

LCD specification: Dots 320xRGBx320
As to basic specification of the driver IC, refer to the IC (ST7365P) specification and data book.
All material & processing of the LCD module should be Lead Free.

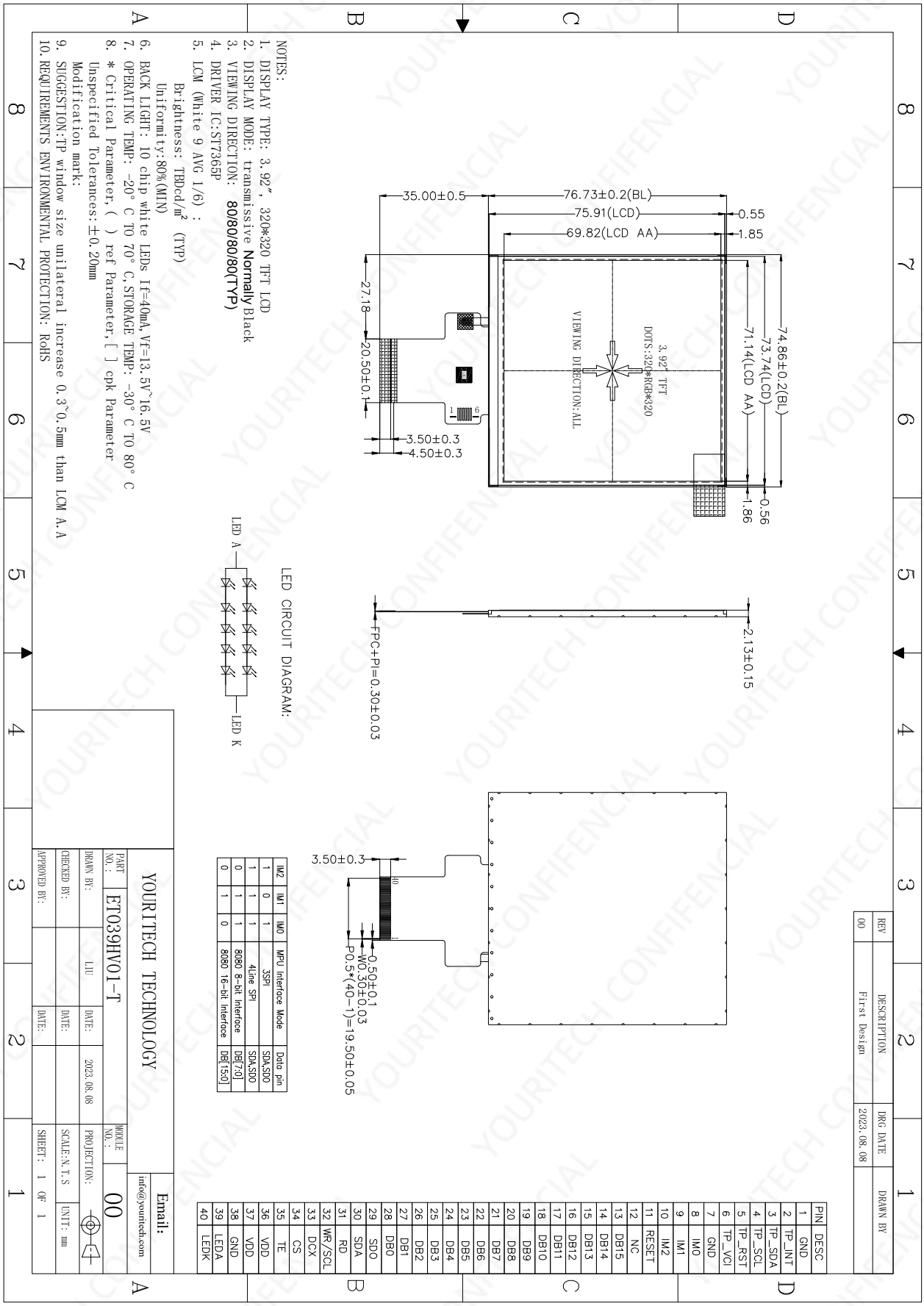
1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL +CTP;
ALL O'CLOCK Type LCD
320 dot-segment and 320 dot-common outputs;
262K Color can be selected by software;
White LED back light;
SPI or MCU interface

1.3 Applications:

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	320*3RGB(H)X320(V)	Dots
Pixel arrangement	RGB stripe	--
Pixel Pitch (W*H)	0.2223(H) x 0.2182(V)	mm
Active area	71.14(H) x 69.82(V)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	ST7365P	--
TFT interface	SPI or MCU Interface	--
LCM Size(W*H*T)	74.86(W) ×76.73(H) ×2.13(T)	mm
Approx. Weight	TBD	g
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--



IM2	IM1	IM0	MPU Interface Mode	Data pin
1	0	1	3SPI	SDA,SDO
1	1	1	4line SPI	SDA,SDO
0	1	1	8080 8-bit Interface	DB[7:0]
0	1	0	8080 16-bit Interface	DB[15:0]

PIN	DESC
1	GND
2	TP_INT
3	TP_SDA
4	TP_SCL
5	TP_RST
6	TP_VCI
7	GND
8	IM0
9	IM1
10	IM2
11	RESET
12	NC
13	DB15
14	DB14
15	DB13
16	DB12
17	DB11
18	DB10
19	DB9
20	DB8
21	DB7
22	DB6
23	DB5
24	DB4
25	DB3
26	DB2
27	DB1
28	DB0
29	SDO
30	SDA
31	RD
32	WR/SCL
33	DCX
34	CS
35	TE
36	VDD
37	VDD
38	GND
39	LEDA
40	LEDK

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	--	--	--	V
Supply Voltage for(DC/DC)	VDD	2.5	2.8	3.3	V

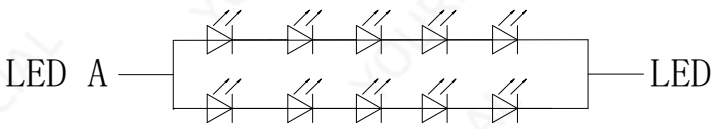
4.2 Back-Light Unit Characeristics

The back-light system is an edge-lighting type with 10 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	13.5	--	16.5	V	--
Forward current	I_F	--	40	--	mA	--
Luminance(With LCD)	Lv	--	TBD	--	cd/m^2	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.Backlight circuit diagram shown in below:



5. Module Function Description

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Functional</th><th>Notes</th></tr>
<tr><td>1</td><td>GND</td><td>Power Ground</td><td></td></tr>
<tr><td>2</td><td>CTP_INT</td><td>Interrupt signal</td><td></td></tr>
<tr><td>3</td><td>CTP_SDA</td><td>Touch panel I2C data</td><td></td></tr>
<tr><td>4</td><td>CTP_SCL</td><td>Touch panel I2C clock</td><td></td></tr>
<tr><td>5</td><td>CTP_RST</td><td>Touch panel reset</td><td></td></tr>
<tr><td>6</td><td>CTP_VCI</td><td>Touch panel Power supply 2.8~3.3V</td><td></td></tr>
<tr><td>7</td><td>GND</td><td>Power Ground</td><td></td></tr>
<tr><td>8-10</td><td>IM0-IM2</td><td>
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th><th>Data pin</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3SPI</td><td>SDA,SDO</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>4Line SPI</td><td>SDA,SDO</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>8080 8-bit Interface</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>8080 16-bit Interface</td><td>DB[15:0]</td></tr>
</table>
</td><td></td></tr>
<tr><td>11</td><td>RESET</td><td>Reset signal input terminal. Active at ‘L’.</td><td></td></tr>
<tr><td>12</td><td>NC</td><td>No Connection.</td><td></td></tr>
<tr><td>13</td><td>DB15</td><td>MCU parallel interface data bus.</td><td></td></tr>
<tr><td>14</td><td>DB14</td><td>MCU parallel interface data bus.</td><td></td></tr>
<tr><td>15</td><td>DB13</td><td>MCU parallel interface data bus.</td><td></td></tr>
<tr><td>16</td><td>DB12</td><td>MCU parallel interface data bus.</td><td></td></tr>
<tr><td>17</td><td>DB11</td><td>MCU parallel interface data bus.</td><td></td></tr>
<tr><td>18</td><td>DB10</td><td>MCU parallel interface data bus.</td><td></td></tr>
<tr><td>19</td><td>DB9</td><td>MCU parallel interface data bus.</td><td></td></tr>
<tr><td>20</td><td>DB8</td><td>MCU parallel interface data bus.</td><td></td></tr>
<tr><td>21</td><td>DB7</td><td>MCU parallel interface data bus.</td><td></td></tr>
<tr><td>22</td><td>DB6</td><td>MCU parallel interface data bus.</td><td></td></tr>
<tr><td>23</td><td>DB5</td><td>MCU parallel interface data bus.</td><td></td></tr>
<tr><td>24</td><td>DB4</td><td>MCU parallel interface data bus.</td><td></td></tr>
<tr><td>25</td><td>DB3</td><td>MCU parallel interface data bus.</td><td></td></tr>
<tr><td>26</td><td>DB2</td><td>MCU parallel interface data bus.</td><td></td></tr>
</table>

27	DB1	MCU parallel interface data bus.	
28	DB0	MCU parallel interface data bus.	
29	SDO	Serial data output pin.	
30	SDA	Serial data input/output pin.	
31	RD	Read data at the rising edge.	
32	WR/SCL	Write strobe signal	
33	DCX	Register select signal.	
34	CS	Chip select signal input pin	
35	TE	Frame head pulse for tearing effect.	
36	VDD	Power Supply For LCD.	
37	VDD	Power Supply For LCD.	
38	GND	Power Ground	
39	LEDA	Power supply for backlight anode input terminal.	
40	LEDK	Power supply for backlight cathode input terminal.	

6. Timing Characteristics

Power ON/OFF Sequence

VDDI and VDD can be applied in any order.

VDD and VDDI can be power down in any order.

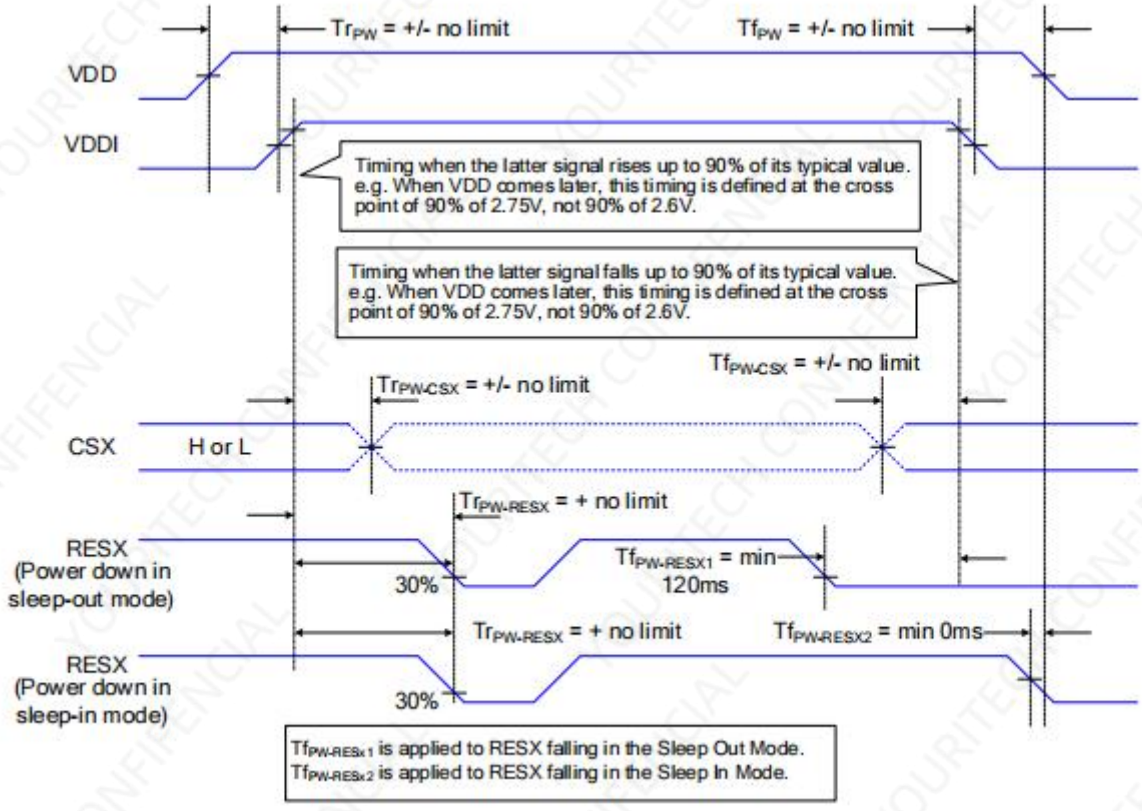
During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

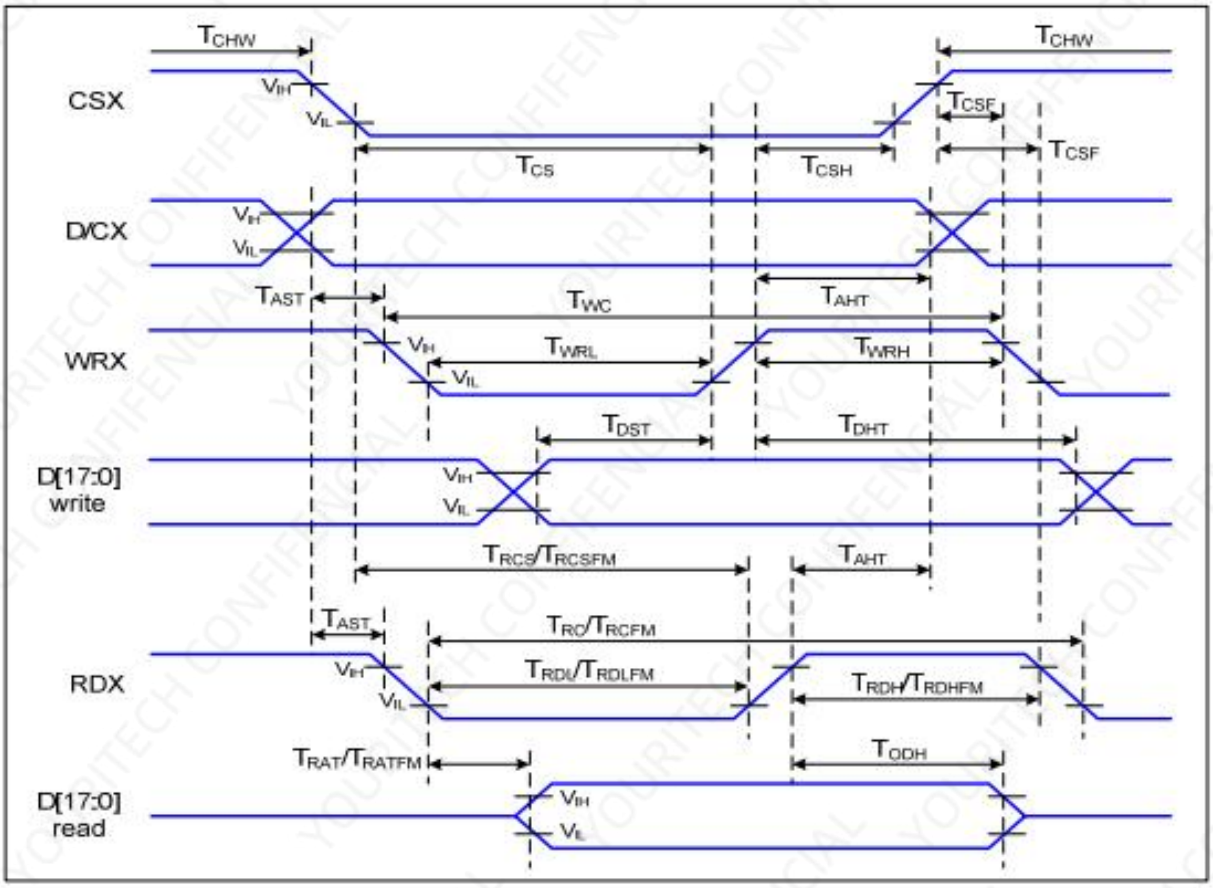
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus



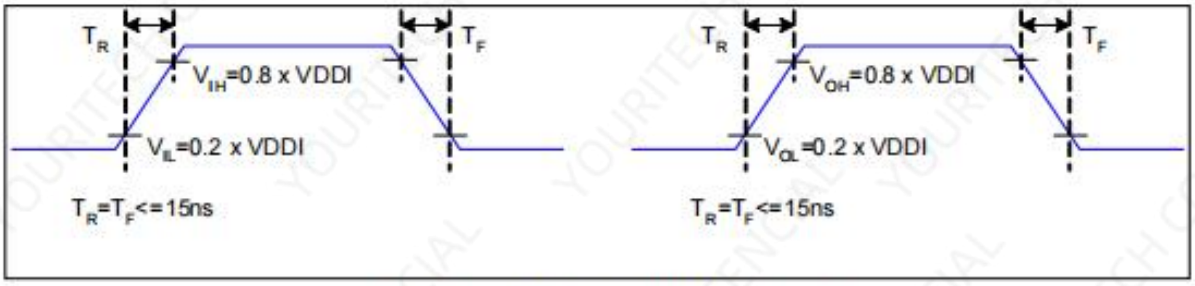
Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to VDD, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	TBD		ns	-
	T_{AHT}	Address hold time (Write/Read)	TBD		ns	
CSX	T_{CHW}	Chip select "H" pulse width	TBD		ns	-
	T_{CS}	Chip select setup time (Write)	TBD		ns	
	T_{RCS}	Chip select setup time (Read ID)	TBD		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	TBD		ns	
	T_{CSF}	Chip select wait time (Write/Read)	TBD		ns	
	T_{CSH}	Chip select hold time	TBD		ns	
WRX	T_{WC}	Write cycle	TBD		ns	
	T_{WRH}	Control pulse "H" duration	TBD		ns	

	T_{WRL}	Control pulse "L" duration	TBD		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	TBD		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	TBD		ns	
	T_{RDL}	Control pulse "L" duration (ID)	TBD		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	TBD		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	TBD		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	TBD		ns	
D[17:0]	T_{DST}	Data setup time	TBD		ns	For CL=30pF
	T_{DHT}	Data hold time	TBD		ns	
	T_{RAT}	Read access time (ID)	TBD	40	ns	
	T_{RATFM}	Read access time (FM)	TBD	340	ns	
	T_{ODH}	Output disable time	TBD	80	ns	

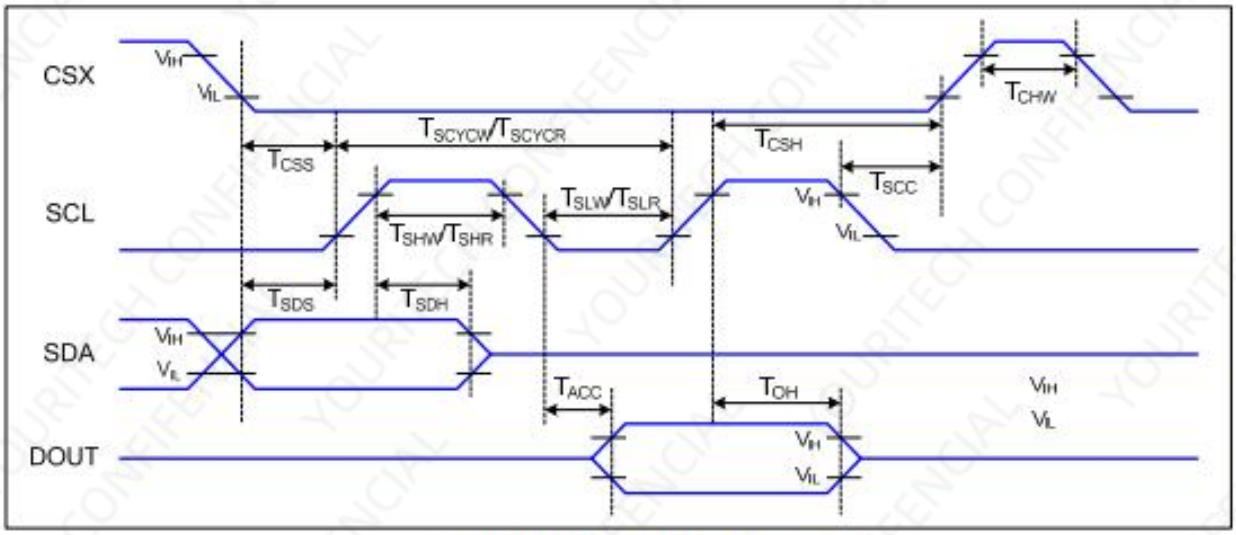
8080 Parallel Interface Characteristics



Rising and Falling Timing for I/O Signal

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

Serial Data Transfer Interface Characteristics:



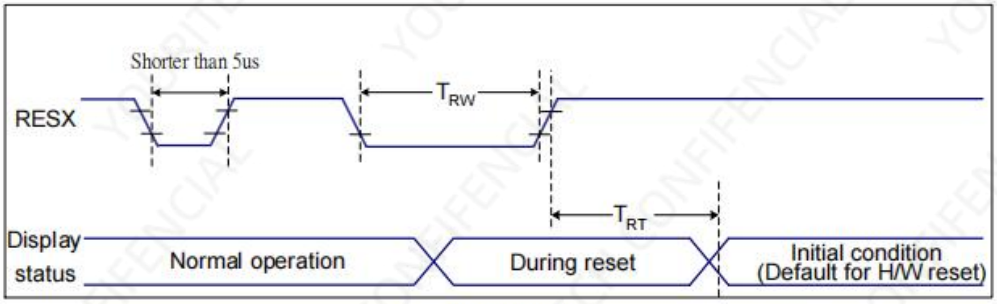
SPI Interface Timing Characteristics

VDDI=1.65 to VDD, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	TBD		ns	
	T_{CSH}	Chip select hold time (write)	TBD		ns	
	T_{CSS}	Chip select setup time (read)	TBD		ns	
	T_{SCC}	Chip select hold time (read)	TBD		ns	
	T_{CHW}	Chip select "H" pulse width	TBD		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	TBD		ns	
	T_{SHW}	SCL "H" pulse width (Write)	TBD		ns	
	T_{SLW}	SCL "L" pulse width (Write)	TBD		ns	
	T_{SCYCR}	Serial clock cycle (Read)	TBD		ns	
	T_{SHR}	SCL "H" pulse width (Read)	TBD		ns	
	T_{SLR}	SCL "L" pulse width (Read)	TBD		ns	
SDA (DIN)	T_{SDS}	Data setup time	TBD		ns	
	T_{SDH}	Data hold time	TBD		ns	
DOUT	T_{ACC}	Access time	TBD	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	TBD	50	ns	For minimum CL=8pF

SPI Interface Characteristics

Reset Timing



Reset Timing

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 1 Reset Timing

Notes:

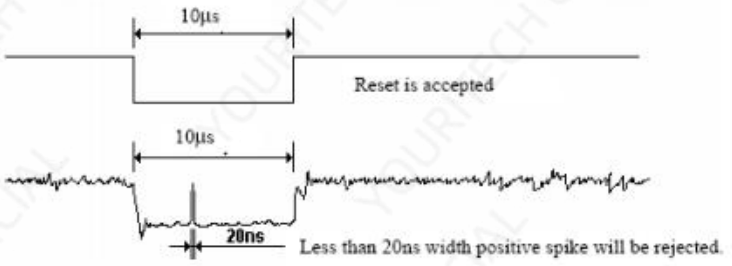
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Optical Specification

The test of view angle range shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2°C) with the equipment of Luminance meter system (Gonio meter system and TOPCON CS2000/CA310) and test unit shall be located at an appro ximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to θØ=0 (=θ3) as the 3 o'clock direction (the "right"), θ Ø=90 (= θ12) as the 12 o'clock direction ("upward"), θ Ø=180 (= θ9) as the 9 o'clock direction ("left") and θ Ø=270(= θ6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the cent er of the measuring spot on the Display surface shall stay fixed. The luminance, color a nd uniformity (etc) should be tested by CS2000/CA310. The backlight should be opera ting for 10 minutes prior to measurement. VDD shall be 3.3 ± 0.3V at 25°C. Optimum v iewing angle direction is 6 'clock

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	75	85	-	Deg.	Note 1
		Θ_9		75	85	-	Deg.	
	Vertical	Θ_{12}		75	85	-	Deg.	
		Θ_6		75	85	-	Deg.	
Contrast ratio		CR	Θ = 0°	800	1000	-	-	Note 2
Transmittance		Tr		4.0	4.8	-	%	Note 3
Color Gamut	NTSC	CIE1931	Θ = 0°	55	60	-	%	Note 4 C Light
Reproduction of color	White	Wx	Θ = 0°	Typ -0.03	0.292	Typ +0.03	-	
		Wy			0.328		-	
Response Time		Tr+Td	Ta= 25° C Θ = 0°	-	25	35	ms	Note 5

Notes : 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with APF and without CG.

4. The color chromaticity coordinates specified in Table 5. shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel and based on C Light

5. The electro-optical response time measurements shall be made as FIGURE 2. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~60℃（30min），10 cycles	

9. Packing Method----TBD

- END -