YOURITech
AN EUROTECH COMPANY

INDUSTRIAL STRENGTH...
Start Your Application From YOURITECH

Integration support
Obsolescence Management
PCAP
Embedded Systems
Human Machine Interface
Touch Solutions
Production
Custom designs
Installation
Software
Mechanical design
Quality Management
Open Frame Monitors
LCD Controller
Research & Development
Firmware
EMC tests
on-site service
In-house Manufacturing
Optical Bonding
Cover glass
System solutions
OEM Solutions
Custom Display

Erotech YOURITech AN EUROTECH COMPANY AOSHITE 奥视特 Your Reliable Display Panel and Smart Touch Embedded Solution Partner

For more information about comprehensive display panels and touch embedded solutions, welcome contact us at:

https://www.youritech.com
info@youritech.com

ET039XGH01-G

OLEDoS Micro Display

Data Sheet

2.1

Record of Revison

Version	Revise Date	Page	Content
1.0	2023-09-09		First Release
2.0	2024-02-20		Initial Release
2.1	2024-5-20		Modify initialization configuration

CONTENTS

1 Product Introduction

ET039XGH01-G is a top-emitting, high-efficiency, active matrix-driven silicon-based OLED microdisplay product independently developed by YOURITECH

The silicon substrate of the microdisplay is manufactured by 0.18μm CMOS process, integrating signal enhancement circuit, row and column drive circuit, logic control circuit and other modules, supporting 8/16/24bit digital video signal input, through the I2C serial bus programming interface, it can realize display mode, display position, brightness, contrast and other function control and status adjustment. This type of microdisplay has the characteristics of low power consumption, high resolution, high integration, miniaturization, etc., and can be widely used in various miniaturized, high-resolution, low-power and wide temperature range near-eye display systems.

1.1 Important features

- Low power consumption;
- High contrast;
- The communication interface supports the I2C universal serial protocol;
- The input interface supports RGB, YCbCr;
- Built-in temperature sensor;
- Built-in PWM mode dimming function;
- Support brightness adaptive adjustment function;
- It has the function of image brightness, contrast and digital signal enhancement;
- Support horizontal/vertical image mirroring, and timed movement function;
- It supports image display position adjustment and is compatible with low-resolution image display;

1.2 Product characteristic parameters

Table 1 List of product characteristic parameters

Product Type	Characteristic parameter values
Color	Full Color
Resolution	1024×768（1040×784 Active pixels ）
Color Pixel Arrangement	RGB Vertical Stripe
Pixel Size	7.8цm×7.8цm
Viewing Area	8.1325mm×6.1779mm
Gray Levels	8bits/256Levels
Luminance Uniformity @200cd/㎡	≥ 90%
Contrast	＞10000:1
Frame rate	25Hz～120Hz
Digital Video Interface	24bit-RGB、 8/16/24bit-YCbCr
Typical Luminance	200 cd/㎡
Advance Luminance	40 cd/㎡ ～ 400 cd/㎡
Power Supply	1.8V、5.0V
Typical Power Consumption	65mW @60Hz
	54mW @25Hz
Chromaticity (White)	CIE-x= 0.300, CIE-y = 0.310
Operating Humidity	≤85%RH（Non condensing）
Operating Temperature	-40℃ ～ +65℃
Weight	1g

2 Functional overview and interfaces

2.1 Block diagram

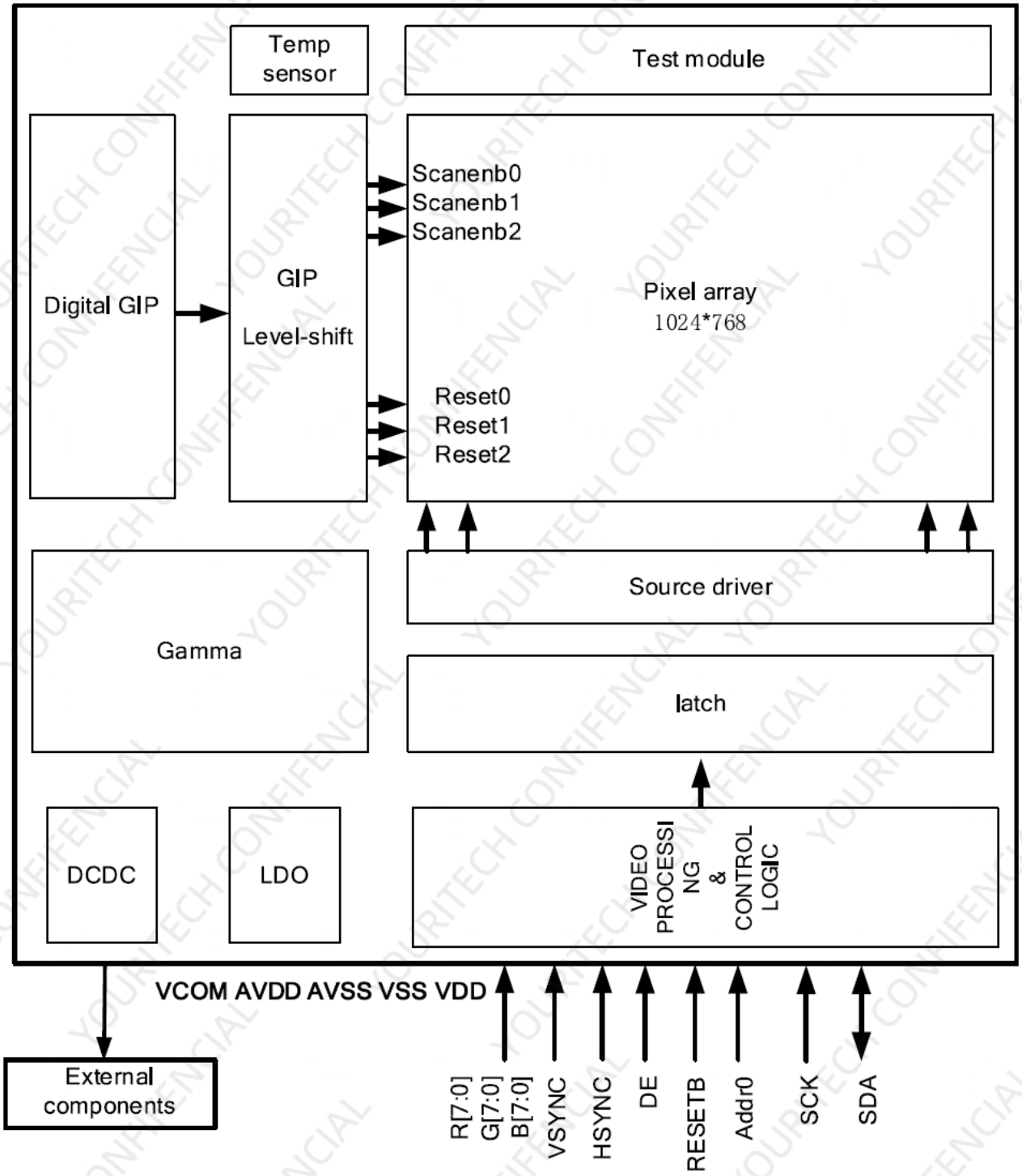


Figure 1 Functional block diagram of a microdisplay

2.2 Pin definition

The micro display electrical interface uses a 0.3mm pitch flip-top 45pin connector, as shown in Figure 2.

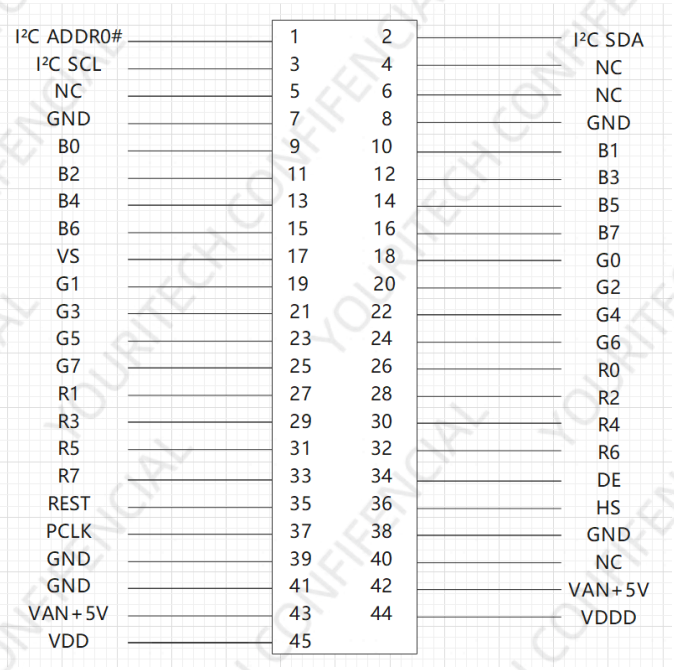


Figure 2 Schematic symbols for the micro display interface

Note: Refer to Section 6 for the detailed dimensions of the connector and the recommended design dimensions of the connector FPC.

The electrical interface pins for the micro display are defined as follows.

Table 2 Definition of electrical interfaces for micro displays

PIN	Symbol	Function
1	I²C ADDR0#	Serial Port Address select(Default pull-up）
2	I²C SDA	Serial port Data line
3	I²C SCL	Serial port clock line
4	NC	NC
5	NC	NC
6	NC	NC
7	GND	Power groung
8	GND	Power groung
9	B0	CbCr[0]，Cb[0]，Blue[0] Video Data Input
10	B1	CbCr[1]，Cb[1]，Blue[1] Video Data Input
11	B2	CbCr[2]，Cb[2]，Blue[2] Video Data Input
12	B3	CbCr[3]，Cb[3]，Blue[3] Video Data Input

PIN	Symbol	Function
13	B4	CbCr[4]，Cb[4]，Blue[4] Video Data Input
14	B5	CbCr[5]，Cb[5]，Blue[5] Video Data Input
15	B6	CbCr[6]，Cb[6]，Blue[6] Video Data Input
16	B7	CbCr[7]，Cb[7]，Blue[7] Video Data Input
17	VS	Vsync Signal Input
18	G0	YCbCr[0]，Y[0]，Green[0] Video Data Input
19	G1	YCbCr[1]，Y[1]，Green[1] Video Data Input
20	G2	YCbCr[2]，Y[2]，Green[2] Video Data Input
21	G3	YCbCr[3]，Y[3]，Green[3] Video Data Input
22	G4	YCbCr[4]，Y[4]，Green[4] Video Data Input
23	G5	YCbCr[5]，Y[5]，Green[5] Video Data Input
24	G6	YCbCr[6]，Y[6]，Green[6] Video Data Input
25	G7	YCbCr[7]，Y[7]，Green[7] Video Data Input
26	R0	Cr[0]，Red[0] Video Data Input
27	R1	Cr[1]，Red[1] Video Data Input
28	R2	Cr[2]，Red[2] Video Data Input
29	R3	Cr[3]，Red[3] Video Data Input
30	R4	Cr[4]，Red[4] Video Data Input
31	R5	Cr[5]，Red[5] Video Data Input
32	R6	Cr[6]，Red[6] Video Data Input
33	R7	Cr[7]，Red[7] Video Data Input
34	DE	Data Enable Signal Input
35	REST	Master Reset, Active Low, Can’t Floating
36	HS	Hsync Signal Input
37	PCLK	Pixel clock input
38	GND	Power groung
39	GND	Power groung
40	NC	NC
41	GND	Power groung
42	VAN+5V	5V Power Supply
43	VAN+5V	5V Power Supply
44	VDD	1.8V Power Supply
45	VDD	1.8V Power Supply

3 Electrical characteristics

3.1 Absolute maximum rating

Table 3 Absolute Maximum Rated Electrical Standards

VDD	1.8V Power Supply	-0.3	2.0	V
VAN	5.0V Power Supply	-0.3	6.0	V
Vcom	Cathode Voltage	-5.5	0	V
V_I	Digital Signal Voltage	-0.3	VAN+0.3	V
Tst	Storage Temperature	-55	+80	℃

3.2 DC characteristics

Table 4 DC Power Supply Characteristics Table

V_D	VDD Voltage	1.62	1.80	1.98	V
I_D	VDD Current	—	—	40	mA
V_A	VAN Voltage	4.50	5.00	5.50	V
I_A	VAN Current	—	—	25	mA
Vcom	Cathode Voltage	-4.8	-2	-0.2	V
V_{IL}	Digital signal low Voltage	-0.3	—	0.5	V
V_{IH}	Digital signal high Voltage	1.2	—	3.6[1]	V
Top	Operation Temperature	-40	+25	+65	℃

Note：The digital input signal is compatible with standards such as 1.8V and 3.3V, but is subject to the electrical standards in Table 4.

3.3 AC characteristics

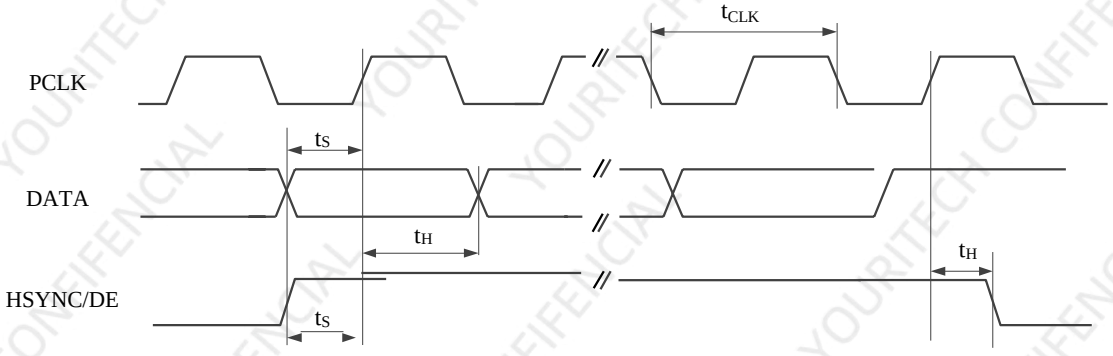


Figure 3 Digital Signal AC Constraints

Table 5 Table of requirements for digital AC parameters

t_S	Digital Video Data Setup	4	—	—	ns
t_H	Digital Video Data Setup	1.5	—	—	ns
t_{CLK}	Video Clock Period	—	15.4	—	ns
d_{CLK}	Video Clock Duty	45	50	55	%

3.4 Power consumption

Table 6 Power consumption of micro displays at different refresh rates

SYMBOL	DESCRIPTION	Typ. 60Hz	Typ. 25Hz	Unit
P_{VDD}	VDD Power consumption	28	24	mW
P_{VAN}	VAN Power consumption	37	30	mW
P_{POWER}	Total power consumption	65	54	mW

Note：The Luminous test condition is 200cd/㎡, the temperature test condition is +25℃±2℃, and the test pattern is full white point.

3.5 Power supply sequence

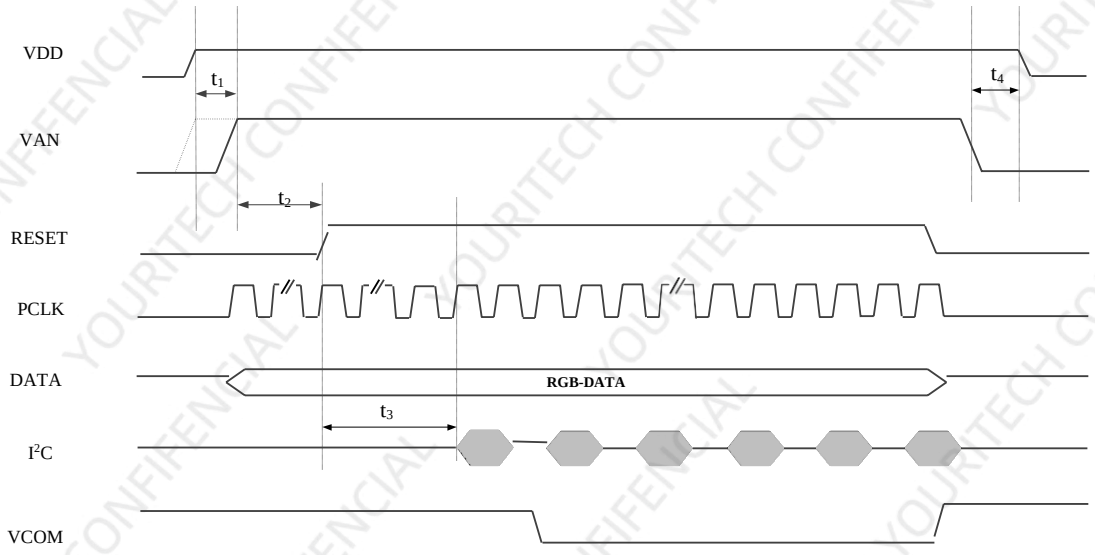


Figure 4 Schematic diagram of the power-on and power-up timing of the microdisplay

Table 7 Lists the parameters of the power supply timing requirements

t_1	VAN Power-on delay	0	—	—	ms
t_2	Power settling time	5	—	—	ms
t_3	OTP content loading and data refresh time	5 frames Time	—	—	—
t_4	power-down time	0	—	—	ms

3.6 Video signal timing constraints

When the timing of the video signal does not conform to the VESA standard, you can configure the timing requirements shown in Figure 5 according to the parameters in Table 8.

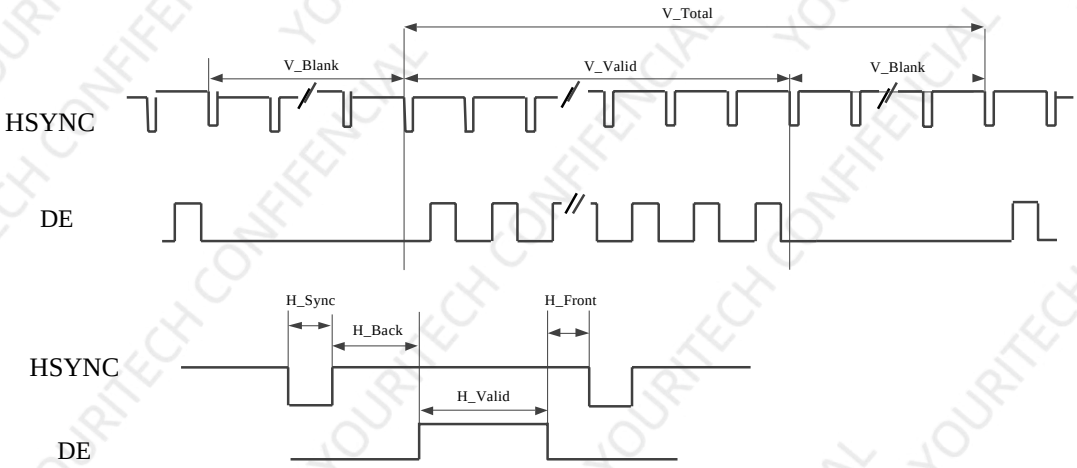


Figure 5 Digital Video Synchronization Signal Control Timing

Table 8 Non-standard timing parameter requirements for micro displays

V_Blank	Field blanking period	22	38	240	HSYNC
V_Valid	Expiration date	—	768	—	HSYNC
H_Sync	Perform the blanking period synchronization period	20	136	500	PCLK
H_Back	Posterior shoulder during the retreating period	20	160	500	PCLK
H_Front	Perform the fade period of the anterior shoulder	20	24	500	PCLK
H_Valid	Line expiration date	—	1024	—	PCLK

4 Function Description

4.1 Summary of Registers

Table 9 List of registers

Register	Bytes	DESCRIPTION	Default Value
0011H	1	Gamma Clock gating	03H
0016H	1	Gamma Enabled	01H
0019H	1	Video input enabled	01H
0069:0068H	2	Cathode voltage 10-bit register setting（Vcom[9:0]）	07FH
0080H	1	BIST Test Mode control on	00H
0095H	1	R channel Grayscale value	FFH
0096H	1	G channel Grayscale value	FFH
0097H	1	B channel Grayscale value	FFH
009BH	1	BIST test mode selection	3FH
009CH	1	BIST Test Mode Wait Time	02H
009DH	1	BIST test frame rate	3CH
00A1H	1	Video signal format selection	00H
00B0H	1	ADC enabled	00H
00B9H	1	ADC Sampling frequency control	00H
00BB:00BAH	2	Internal temperature test final ADC value	XXH
1000H	1	VS/HS Effective polarity	00H
1007H	1	Data gain contrast adjustment enabled	02H
1008:1009H	2	Data gain Contrast adjustment	FFFFH
1012:1010H	2	Starting point of ADC Sample one frame	FFFH
1011H	1	Reserved	FFH
1018H	1	Gamma control initiation	00H
1061H	1	System sleep out control	00H
1062H	1	System display on control	00H
1063H	1	System boot on control	00H
2000H	1	Vertical setting enabled	00H
2002H	1	Remap vertical effective start position	01H
2003H	1	Remap vertical effective end position	1BH
2004H	1	Remap vertical effective end and start position	40H
2005:2006H	2	Horizontal scan active pixels	8007H
2007:2008H	2	Vertical scan active pixels	3804H
2009:200BH	2	Vertical scan start line	800H
201A:201BH	2	255 grayscale adjustment	0C05H
2028H	1	Vertical data update bits	01H
2030H	1	Remap Enable	00H
2031H	1	Gamma LUT Adjust and enable	21H
2041H	1	Horizontal front dummy pixels	0CH
2042H	1	Horizontal back dummy pixels	0CH
2053H	1	Horizontal channel start block	00H
2054H	1	Horizontal channel end block	FFH
2058H	1	Gamma R/G channel Low-level voltage trimming	00H
2059H	1	Gamma B channel Low-level voltage trimming	00H

Register	Bytes	DESCRIPTION	Default Value
206DH	1	Horizontal scan	00H
206EH	1	Vertical scan	07H
206FH	1	Digital brightness adjustment	00H
2085:2086H	2	Digital brightness pwm_0 pulses	0001H
20D3:20D4H	2	Digital brightness pwm_0 pulses duty adjustment	200H
20D0H	1	Manual control digital brightness PWM pulse enabled	01H
20D1H	1	Manual control digital brightness PWM pulses	04H
20E9H	1	Gamma R channel Low-level voltage trimming	FFH
20EBH	1	Gamma G channel Low-level voltage trimming	FFH
20EDH	1	Gamma B channel Low-level voltage trimming	FFH
20F0H	1	Cathode voltage Vcom enabel	00H
2100:2101H	2	Gamma R channel High-level voltage trimming	000H
2106:2107H	2	Gamma G channel High-level voltage trimming	000H
210C:210DH	2	Gamma B channel High-level voltage trimming	000H
4000:4001H	2	Gamma_0 x inflection point grayscale binding point setting	000H
4002:4003H	2	Gamma_1 x inflection point grayscale binding point setting	000H
4004:4005H	2	Gamma_2 x inflection point grayscale binding point setting	000H
4006:4007H	2	Gamma_3 x inflection point grayscale binding point setting	000H
4008:4009H	2	Gamma_4 x inflection point grayscale binding point setting	000H
400A:400BH	2	Gamma_5 x inflection point grayscale binding point setting	000H
400C:400DH	2	Gamma_6 x inflection point grayscale binding point setting	000H
400E:400FH	2	Gamma_7 x inflection point grayscale binding point setting	000H
4010:4011H	2	Gamma_8 x inflection point grayscale binding point setting	000H
4012:4013H	2	Gamma_9 x inflection point grayscale binding point setting	000H
4014:4015H	2	Gamma_10 x inflection point grayscale binding point setting	000H
4016:4017H	2	Gamma_11 x inflection point grayscale binding point setting	000H
4018:4019H	2	Gamma_12 x inflection point grayscale binding point setting	000H
401A:401BH	2	Gamma_13 x inflection point grayscale binding point setting	000H
401C:401DH	2	Gamma_14 x inflection point grayscale binding point setting	000H
401E:401FH	2	Gamma_15 x inflection point grayscale binding point setting	000H
4020:4021H	2	Gamma_16 x inflection point grayscale binding point setting	000H
4022:4023H	2	Gamma_R channel 0 y inflection point data	000H
4024:4025H	2	Gamma_R channel 1 y inflection point data	000H
4026:4027H	2	Gamma_R channel 2 y inflection point data	000H
4028:4029H	2	Gamma_R channel 3 y inflection point data	1C5H
402A:402BH	2	Gamma_R channel 4 y inflection point data	1C5H
402C:402DH	2	Gamma_R channel 5 y inflection point data	1C5H
402E:402FH	2	Gamma_R channel 6 y inflection point data	0C5H
4030:4031H	2	Gamma_R channel 7 y inflection point data	1C5H
4032:4033H	2	Gamma_R channel 8 y inflection point data	1C5H
4034:4035H	2	Gamma_R channel 9 y inflection point data	1C5H
4036:4037H	2	Gamma_R channel 10 y inflection point data	1C5H
4038:4039H	2	Gamma_R channel 11 y inflection point data	1C5H
403A:403BH	2	Gamma_R channel 12 y inflection point data	1C5H
403C:403DH	2	Gamma_R channel 13 y inflection point data	1C5H
403E:403FH	2	Gamma_R channel 14 y inflection point data	0BBH
4040:4041H	2	Gamma_R channel 15 y inflection point data	3BBH

Register	Bytes	DESCRIPTION	Default Value
4042:4043H	2	Gamma_R channel 16 y inflection point data	3BBH
4044:4045H	2	Gamma_G channel 0 y inflection point data	3BBH
4046:4047H	2	Gamma_G channel 1 y inflection point data	3BBH
4048:4049H	2	Gamma_G channel 2 y inflection point data	3BBH
404A:	2	Gamma_G channel 3 y inflection point data	3BBH
404BH404C:	2	Gamma_G channel 4 y inflection point data	3BBH
404DH	2	Gamma_G channel 5 y inflection point data	3BBH
404E:404FH	2	Gamma_G channel 6 y inflection point data	3BBH
4050:4051H	2	Gamma_G channel 7 y inflection point data	3BBH
4052:4053H	2	Gamma_G channel 8 y inflection point data	3BBH
4054:5055H	2	Gamma_G channel 9 y inflection point data	3BBH
4056:4057H	2	Gamma_G channel 10 y inflection point data	3BBH
4058:4059H	2	Gamma_G channel 11 y inflection point data	3BBH
405A:	2	Gamma_G channel 12 y inflection point data	3BBH
405BH405C:	2	Gamma_G channel 13 y inflection point data	3BBH
505DH	2	Gamma_G channel 14 y inflection point data	3BBH
405E:505FH	2	Gamma_G channel 15 y inflection point data	3BBH
4060:4061H	2	Gamma_G channel 16 y inflection point data	3BBH
4062:4063H	2	Gamma_B channel 0 y inflection point data	3BBH
4064:4065H	2	Gamma_B channel 1 y inflection point data	3BBH
4066:4067H	2	Gamma_B channel 2 y inflection point data	3BBH
4068:4069H	2	Gamma_B channel 3 y inflection point data	0BBH
406A:	2	Gamma_B channel 4 y inflection point data	3BBH
406BH406C:	2	Gamma_B channel 5 y inflection point data	3BBH
406DH	2	Gamma_B channel 6 y inflection point data	3BBH
406E:406FH	2	Gamma_B channel 7 y inflection point data	3BBH
4070:4071H	2	Gamma_B channel 8 y inflection point data	3BBH
4072:4073H	2	Gamma_B channel 9 y inflection point data	3BBH
4074:4075H	2	Gamma_B channel 10 y inflection point data	3BBH
4076:4077H	2	Gamma_B channel 11 y inflection point data	373H
4078:4079H	2	Gamma_B channel 12 y inflection point data	373H
407A:	2	Gamma_B channel 13 y inflection point data	373H
407BH407C:	2	Gamma_B channel 14 y inflection point data	373H
407DH	2	Gamma_B channel 15 y inflection point data	373H
407E:407FH	2	Gamma_B channel 16 y inflection point data	373H
4080:4081H			
4082:4083H			
4084:4085H			
4086:4087H			

4.2 Detailed Information of Register

Register	W	Bite	Function	Value	Description
0011H	RW	0	Gamma clock	F3H	0：off，1：on
0016H	RW	0	Gamma enabled	01H	0：off，1：on
0019H	RW	0	Video input enabled	01H	0：off，1：on
0068H	RW	7:0	Vcom setting value low 8bit	7FH	10bite Vcom setting value
0069H	RW	9:8	Vcom setting value high 2bit	00H	
0080H	RW	0	BIST test mode enable	00H	0：off，1：on
0095H	RW	7:0	bist_r_gray[7:0]	FFH	bist R channel 8bit Grayscale values
0096H	RW	7:0	bist_g_gray[7:0]	FFH	bist G channel 8bit Grayscale values
0097H	RW	7:0	bist_b_gray[7:0]	FFH	bist B channel 8bit Grayscale values

Register	W	Bite	Function	Value	Description
009BH	RW	5:0	bist_pattern [5:0]	3FH	BIST test pattern mode 01: All white 02: All black 04: Horizontal grayscale gradient 08:Vertical grayscale gradient 10:Checkerboard 20:Light and dark stripes
009CH	RW	2:0	bist_pattern_time[2:0]	02H	BIST mode display hold time
009DH	RW	7:0	bist_pattern_frame_rate[7:0]	3CH	BIST mode frame rate setting
00A1H	RW	2:0	image_format_sel[2:0]	00H	Video signal format selection 0:RGB,24bits 1:YCbCr,4:4:4 2:YCbCr,4:2:2,16bit 3:Mono 4:YCbCr,4:2:2,8bit
00B0H	RW	0	adc_en[0]	00H	ADC enable 0:off 1:on
00B9H	RW	5:0	adc_frame_div	00H	ADC sampling frequency 60Hz, register set 2, and ADC sampling frequency is 30Hz
00BAH	OR	7:0	adc_sample_posi[7:0]	XXH	Final ADC value for Internal temperatrure detection
00BBH	OR	1:0	adc_sample_posi[11:8]	0XH	
1000H	RW	1	hs_polar	00H	VS/HS Effective polarity 0: Valid low 1: Valid high
	RW	0	vs_polar		
1007H	RW	0	shrinker_en	02H	Ddata_gain Contrast adjustment enabled 0: off 1: on
1008H	RW	7:0	shrinker_gain_0[15:8]	FFH	Data_gain Contrast adjustment ffffH is the brightest; 0000H is the darkest
1009H	RW	7:0	shrinker_gain_0[7:0]	FFH	
1010H	RW	7:0	adc_sample_posi[7:0]	FFH	Where in a frame of the ADC is sampled
1012H	RW	3:0	adc_sample_posi[11:8]	0FH	
1011H	RW	X	reserved	FFH	Reserved
1018H	RW	5	dgma_lut_rw_en	00H	Gamma Data Update 0:End of update 1:Initiate the update
	RW	4	dgma_mode		Gamma enabled 0:off 1:on
	RW	1:0	luminance_rw_sel[1:0]		Gamma Group selection(total 3 sets) 1:No. 1 2: No. 2 3: No. 3
1061H	RW	7	System sleep out	00H	System sleep out control
1062H	RW	7	Display on	00H	System display on control
1063H	RW	7	System boot on	00H	System boot on control
2000H	RW	0	vsetting_en	00H	Vertical setting enable 0:off 1:on
2002H	RW	7:0	remap_vactive_ss[7:0]	01H	Remap vertical valid starting position
2003H	RW	7:0	remap_vactive_se[7:0]	1BH	Remap vertical valid end position
2004H	RW	7:4	remap_vactive_se[11:8]	40H	Remap vertical valid end position
		3:0	remap_vactive_ss[11:8]		Remap vertical valid starting position

Register	W	Bite	Function	Value	Description
2005H	RW	7:0	hactive[7:0]	80H	Horizontal active pixels
2006H	RW	3:0	hactive[11:8]	07H	
2007H	RW	7:0	vactive[7:0]	38H	Vertical active pixels
2008H	RW	3:0	vactive[11:8]	04H	
2009H	RW	7:0	vstart[7:0]	08H	Vertical scan starting line
200BH	RW	7:4	vstart[11:8]	00H	
201AH	RW	7:0	255_gray_set[7:0]	0CH	255 grayscale adjustment
201BH	RW	3:0	255_gray_set[3:0]	05H	
2028H	RW	0	update_vsetting	01H	Vertical Data update 0:off，1:on
2030H	RW	0	remap_en	00H	Remap enabled 0:off，1:on
2031H	RW	4	dgma_en	31H	Gamma_LUT adjustment enabled
		1:0	dgma_lut_sel		Gamma Data sets selection 1:No.1，2:No.2，3:No.3
2041H	RW	5:0	h_front_dummy	08H	Horizontal front dummy pixels
2042H	RW	5:0	h_back_dummy	08H	Horizontal back dummy pixels
2053H	RW	7:0	h_channel_start	00H	Horizontal channel start block
2054H	RW	7:0	h_channel_end	81H	Horizontal channel end block
2058H	RW	5:3	vgam_gbtm_trim	00H	Gamma G channel Low-level voltage trimming
2058H	RW	2:0	vgam_rbtm_trim		Gamma R channel Low-level voltage trimming
2059H	RW	2:0	vgam_bbtm_trim	00H	Gamma B channel Low-level voltage trimming
206DH	RW	2:0	lr_sel	00H	Horizontal scanning 0~6: left to right, 7: right to left
206EH	RW	2:0	ud_se	07H	Vertical scanning 0~6: bottom to top, 7: top to bottom
206FH	RW	1:0	luminance_sel[1:0]	00H	Digital brightness configuration scheme selection 0:No.1 1:No.2 2:No.3
2085H	RW	7:0	pwm_en_0[15:8]	00H	The first scheme of digital brightness pwm_0 the number of pulses
2086H	RW	7:0	pwm_en_0[7:0]	01H	
20D3H	RW	3:0	pwm_duty_0[10:8]	00H	Digital Brightness pwm_0 Pulse Duty Adjustment Range (0~1024) ex.: 50%=0.5*1024=512(200H)
20D4H	RW	7:0	pwm_duty_0[7:0]	00H	
20D0H	RW	4	pwm_force_en	11H	Manual control the number of PWM pulses in digital brightness
20D1H	RW	4:0	pwm_ force_num	01H	Manual control the number of PWM pulses for digital brightness
20E9H	RW	3:0	vgam_rbtm_set_0	FFH	No.1 Gamma R channel Low-level voltage regulation
20EBH	RW	3:0	vgam_gbtm_set_0	FFH	No.1 Gamma G channel Low-level voltage regulation
20EDH	RW	3:0	vgam_bbtm_set_0	FFH	No.1 Gamma B channel Low-level voltage regulation
20F0H	RW	0	Vcom_set_en	00H	Internal cathode voltage enabled
2100H	RW	2:0	vgam_rtop_set_0[9:8]	00H	Gamma R channel High-level voltage regulation
2101H	RW	7:0	vgam_rtop_set_0[7:0]	00H	
2106H	RW	2:0	vgam_gtop_set_0[9:8]	00H	Gamma G channel High-level voltage regulation
2107H	RW	7:0	vgam_gtop_set_0[7:0]	00H	
210CH	RW	2:0	vgam_btop_set_0[9:8]	00H	Gamma B channel High-level voltage

Register	W	Bite	Function	Value	Description
210DH	RW	7:0	vgam_btop_set_0[7:0]	00H	regulation
4000~401FH	RW	9:0	dgma_x_lut0~17[9:0]	000H	Gamma_0~17 x inflection point data, position [1:0], and the odd address
4022:4043H	RW	9:0	dgma_y_r0_lut0~17[9:0]	1C5H	Gamma_R channel 0~17y inflection point data, the even address bit is the high position [1:0], and the odd address is the low position [7:0]
4044:4065H	RW	9:0	dgma_y_g0_lut0~17[9:0]	3BBH	Gamma_G channel 0~17y inflection point data, the even address bit is the high position [1:0], and the odd address is the low position [7:0]
4066:4087H	RW	9:0	dgma_y_b0_lut0~17[9:0]	3BBH	Gamma_B channel 0~17y inflection point data, the even address bit is the high position [1:0], and the odd address is the low position [7:0]

4.3 Internal Test Chart Settings

The Register 009BH has 6 built-in test pattern modes, which are All white test image, All black test image, horizontal grayscale test image, vertical grayscale test image, checker board test image and light and dark stripe test pattern. The host selects a different test mode by configuring the bist_pattern, as shown below:

Table 10 Description of internal test graph registers

Bist mode test pattern	Mode selection(009BH)	R (0095H)	G (0096H)	B (0097H)
All white	0x01	255	255	255
All Red	0x01	255	0	0
All Green	0x01	0	255	0
All Blue	0x01	0	0	255
All black	0x02	0	0	0
Horizontal grayscale	0x04	255	255	255
Vertical grayscale	0x08	255	255	255
Checker board（40*40）	0x10	255	255	255
Light and dark stripes	0x20	255	255	255

If the host wants to test only one pattern individually, such as a checkerboard image test. Then the host can configure 009BH to 0x10, 0080H can be set to 0x01, if you want to realistically pure white or pure black at the same time, and cycle the display, just configure 009BH to 0x03, and adjust the display time through bist_pattern_time and bist_pattern_frame_rate.

4.4 Digital video input signal format

4.4.1 Input data format selection

The micro display supports a variety of digital video signal format inputs, which are detailed below.

Table 11 Description of the input data format registers

Addr	bit	Description
00a1H	bit2~0	000: 24bit-RGB, 4:4:4 mode; 001: 24bit-YCbCr, 4:4:4 mode; 010: 16bit-YCbCr, 4:2:2 mode; 011: 8bit-MONO Y[7:0]; 100: 8bit-YCbCr,4:2:2 mode.

When video signals of different formats are inputted, the pin-to-pin correspondence is as follows.

Table 12 List of input pins for each digital signal format

PIN	8bit-4:2:2	8bit	16bit-4:2:2	24bit-4:4:4	24bit-4:4:4
DATA23	GND	GND	GND	Y[7]	R[7]
DATA22				Y[6]	R[6]
DATA21				Y[5]	R[5]
DATA20				Y[4]	R[4]
DATA19				Y[3]	R[3]
DATA18				Y[2]	R[2]
DATA17				Y[1]	R[1]
DATA16				Y[0]	R[0]
DATA15	Y/Cb/Cr[7]	Y/Cb/Cr[7]	Y[7]	Cb[7]	G[7]
DATA14	Y/Cb/Cr[6]	Y/Cb/Cr[6]	Y[6]	Cb[6]	G[6]
DATA13	Y/Cb/Cr[5]	Y/Cb/Cr[5]	Y[5]	Cb[5]	G[5]
DATA12	Y/Cb/Cr[4]	Y/Cb/Cr[4]	Y[4]	Cb[4]	G[4]
DATA11	Y/Cb/Cr[3]	Y/Cb/Cr[3]	Y[3]	Cb[3]	G[3]
DATA10	Y/Cb/Cr[2]	Y/Cb/Cr[2]	Y[2]	Cb[2]	G[2]
DATA9	Y/Cb/Cr[1]	Y/Cb/Cr[1]	Y[1]	Cb[1]	G[1]
DATA8	Y/Cb/Cr[0]	Y/Cb/Cr[0]	Y[0]	Cb[0]	G[0]
DATA7	GND	GND	Cb/Cr[7]	Cr[7]	B[7]
DATA6			Cb/Cr[6]	Cr[6]	B[6]
DATA5			Cb/Cr[5]	Cr[5]	B[5]
DATA4			Cb/Cr[4]	Cr[4]	B[4]
DATA3			Cb/Cr[3]	Cr[3]	B[3]
DATA2			Cb/Cr[2]	Cr[2]	B[2]
DATA1			Cb/Cr[1]	Cr[1]	B[1]
DATA0			Cb/Cr[0]	Cr[0]	B[0]

4.4.2 YCbCr format signal description

When the input digital video signal is in YCbCr encoding format, the color space transformation of the YCbCr digital signal needs to be performed inside the chip, and the conversion relationship is as follows.

R = Y + Cr×179/128−179

G = Y − Cb×44/128–Cr×91/128 + 135

B = Y + Cb×227/128–227

Note： The use status of YCbCr encoding mode is not compatible with the default 24bit-RGB mode when leaving the factory, and the scope and method of use need to be redefined.

4.5 Image up/down, left/right mirroring

The micro display supports the image of the video image to be mirrored in the horizontal and vertical directions.

Table 14 Image top/bottom/left mirror register description

0x206E	Bit2~0	Vertical display settings 0x00~0x06: Vertical mirror display(bottom to top) 0x07(default): Vertical normal display(top to bottom)
0x206D	Bit2~0	Horizontal display settings 0x00(default),0x01~0x06: The level is displayed normally(left to right) 0x07: Horizontal mirroring(right to left)

The following diagram shows the horizontal and vertical mirror image displays.

4.6 Image display Setting

The micro display supports the display of the whole screen image in any position, and the horizontal and vertical offset position values can be set separately.

Table 15 Description of the position registers displayed horizontally/vertically for the image

Name	Addr	Bits	value(Hex)	Description
Vs_polar	0x1000	B[0]	00H	VS active polar, when vs=1 is active, vs_polar=1
Hs_polar		B[1]		HS active polar, when hs=1 is active, vs_polar=1
h_channel_start	0x2053	B[7:0]	00H	Horizontal channel enable start
h_channel_end	0x2054	B[7:0]	81H	Horizontal channel enable end
h_front_dummy	0x2041	B[5:0]	08H	Horizontal front dummy pixels
h_back_dummy	0x2042	B[5:0]	08H	Horizontal back dummy pixels
vactive[11:8]	0x2008	B[3:0]	04H	Vertical active pixel number
vactive[7:0]	0x2007	B[7:0]	38H	
vstart[11:8]	0x200b	B[11:8]	00H	The start line of vertical
vstart[7:0]	0x2009	B[7:0]	08H	
ud_sel	0x206e	B[2:0]	07H	Vertical scan driection
lr_sel	0x206d	B[2:0]	00H	Horizontal scan driection

Note：

*1.The position of the first pixel in the horizontal direction: h_channel_start*8 + h_front_dummy the position of the last pixel in the horizontal direction: (h_channel_end + 1)*8 - h_back_dummy – 1;*

2.The position of the first line in the vertical direction is determined by the value of vstart(0x2009/0x200b). The number of lines displayed vertically is determined by the value of vactive (0x2008 / 0x2007), as shown above is h'300=d'768.

For example, if you want to display a 1024x768 image from row 8 and column 4 on the screen, you can set it as follows according to the default values of horizontal and vertical resolution above.

First, in the horizontal direction, configure the h_channel_start to 0x0, h_front_dummy to 0x4, h_channel_end to 0x80, and h_back_dummy to 0x4According to the above formula, the position of the first pixel in the horizontal direction is 0x0*8+0x4=0x4=4, and the position of the last pixel in the horizontal direction is (0x80+1)*8-0x4-1=0x403=1027. That is, the horizontal display pixel is 1027+1-4 = 1024.

Vertically, it will be simpler, the starting column is row 8 = 0x8, and the number of valid columns is 0x300 = 768.

0x2053 0x00;(h_channel_start=0x0)

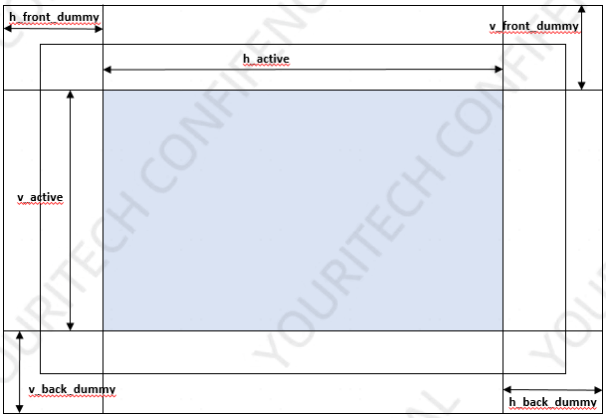
0x2041 0x04;(h_front_dummy=0x4)

0x2054 0x80;(h_channel_end=0x80)

0x2042 0x04;(h_back_dumy=0x4)

0x2009 0x08; 0x200b 0x00;(vstart=0x8)

0x2007 0x00; 0x2008 0x03;(vactive=0x300)



4.7 Temperature Sensor

The micro-display has a temperature detection function, and the temperature conversion formula is:

$$T = 0.65 \times Reg(H) - 375.5$$

Including， T is the actual temperature value， Reg(H) is a temperature register 00BAH and 00BBH readings.

Note:

1.The temperature reading changes greatly during the power-on initialization of the microdisplay, so it is recommended to read the temperature value after it has been stable for a few seconds.

2.During normal operation, the temperature readings are updated on a four-frame image cycle.

4.8 luminance adjustment

The default luminance of the micro display is about 200cd/㎡ when it leaves the factory, and the recommended brightness range is 40cd/㎡~400cd/㎡, and users can adjust the brightness appropriately according to their needs.

Luminance adjustment supports 2 debugging methods, gamma voltage regulation and data gain regulation (DDP digital data processing), in these two brightness adjustment methods, each of which has three options to choose from, and the scheme is selected through the b[1:0] of register 206FH, and the first scheme is adopted by our default.

Table 16 Description of Luminance adjustment registers

Name	Address	Bits	value	Description
luminance_sel[1:0]	0x206f	[1:0]	0x0	brightness adjust configure data choose
vgam_rbtm_set_0	0x20E9	[3:0]	0xf	gamma bottom red voltage0 adjust
vgam_gbtm_set_0	0x20EB	[3:0]	0xf	gamma bottom green voltage0 adjust
vgam_bbtm_set_0	0x20ED	[3:0]	0xf	gamma bottom blue voltage0 adjust
vgam_rbtm_trim	0x2058	[2:0]	0x7	gamma_bottom red voltage trim
vgam_gbtm_trim	0x2058	[5:3]	0x7	gamma_bottom green voltage trim
vgam_bbtm_trim	0x2059	[2:0]	0x7	gamma_bottom blue voltage trim
vgam_rtop_set_0[9:8]	0x2100	[2:0]	0x000	gamma top red voltage0 adjust
vgam_rtop_set_0[7:0]	0x2101	[7:0]		
vgam_gtop_set_0[9:8]	0x2106	[2:0]	0x000	gamma top green voltage0 adjust
vgam_gtop_set_0[7:0]	0x2107	[7:0]		
vgam_btop_set_0[9:8]	0x210c	[2:0]	0x000	gamma top blue voltage0 adjust
vgam_btop_set_0[7:0]	0x210d	[7:0]		
vcom_vset _0[7:0]	0x0068	[7:0]	0x07f	Vcom0 adjust
vcom_vset _0[9:8]	0x0069	[1:0]		
255_gray_set[7:0]	0x201a	[7:0]	0x0c	255 gray adjust
255_gray_set[3:0]	0x201b	[3:0]	0x05	

4.8.1 Digital luminance adjustment PWM

PWM dimming can adjust the brightness of the display pixel by adjusting the duty cycle of the luminous light. There are three sets of registers that control PWM duty cycle dimming, which are 11-bit registers with 10 decimal places. The configuration range (0~1024) represents a duty cycle of 0~1.0, assuming that the desired duty cycle is 0.5, the configured register value is 0.5*1024=512. The three sets of registers are as follows, and the specific choice of which group is determined by the register luminance_sel [1:0]. In general, the parameters of each PWM are automatically obtained by calculation, and only when the pwm_force_en is configured to 1, the number of PWM pulses is determined by the pwm_force_num.

Table 19 PWM dimming register description

Name	Address	Bits	value	Description
pwm_force_en	0x20d0	[4]	0x11	Manual control the number of pwm_pulse enabled
pwm_force_num	0x20d1	[4:0]	0x01	Manual control the number of pwm_pulse
pwm_en_0	0x2085	[15:8]	0x01	The number of pwm0 pulse enable
	0x2086	[7:0]		
pwm_duty_0	0x20d3	[10:8]	0x00	PWM has a duty cycle of 100%.
	0x20d4	[7:0]		

The number of pulses in PWM can be set to 1 in bit4 in the pwm_force (0x20d0) first, and then it can be configured[4:0] in pwm_force_num (0x20d1) is the number of pwm_pulse.

4.8.2 Digital contrast data gain adjustment

The number has three sets of 16-bit decimal data gain registers, and the specific choice of one is determined by the register luminance_sel [1:0]. Data gain linearly adjusts the pixel value from 0~65535, where 0 represents the data gain value of 0, and 65535 represents the data gain value of 65535/65536. Data gain adjusts the pixel value linearly.

Name	Address	Bits	Default	Description
shrinker_en	0x1007	[0]	0x0	data gain adjust enable
shrinker_gain_0[15:8]	0x1008	[7:0]	0xff	first group gain
shrinker_gain_0[7:0]	0x1009	[7:0]	0xff	

4.9 Gating related configurations

After configuring the image resolution and initial brightness, you need to complete the relevant registers such as gray adjustment, DGMA clock enablement, vsetting enablement, and update, as follows.

Name	Address	Bits	value	Description
rgb_gray_en	0x0060	[2]	0X0b	RGB channel gray enable
updata_vsetting[b]	0x2028	[0]	0x01	Vertical data update bit
vsetting_en	0x2000	[0]	0x01	Vertical setting enable control
gamma_en_control	0x1018	[5]	0x10	dgma_lut_rw_en
		[4]		dgma_mode

Name	Address	Bits	value	Description
		[1:0]		luminance_rw_sel
B[0]=remap_en	0x2030	[0]	0x01	remap enable
dgma_lut_en	0x2031	[5:0]	0x31	gamma lut adjust enable
dgma_clock_en	0x0011	[0]	0xff	gamma clock enable
dgma_en	0x0016	[0]	0x01	gamma enable
B[7:0]=255_gray_set[7:0]	0x201a	[7:0]	0x99	255 gray seting
B[3:0]=255_gray_set[11:8]	0x201b	[3:0]	0x04	
Vcom_set_en	0x20f0	[0]	0x01	vcom seting enable
Power related Register	0x0055	[3:2]	0x29	System configuration
	0x0026	[0]	0x01	
	0x0012	[0]	0x00	
	0x2080	[0]	0x01	

4.10 Internal state control of the system

The system goes through a series of states after powering up, such as system_initial, system_boot_on, system_sleep_in, system_sleep_out, display_on and image_transmission. The system boot on, system sleep out and display on are controlled by the host, and after the ET039XGH01-G is configured and the image is prepared, it will enter the image transmission state and transmit the image until the host stops.

In the above state, the host can control the state machine jump of the system through the following three registers.

Name	Address	Bits	Default	Description
System boot on	0x1063	[7]	0x0	System prepare to operate after host configures the system
System sleep out	0x1061	[7]	0x0	System wake up internal circuit
Display on	0x1062	[7]	0x0	System prepare to display picture

After the system is powered up, it is in system_initial, and the host can configure the relevant registers according to the needs, such as the resolution of the image, the clock, etc. After the system configuration is completed, the system enters the system_boot_on state, and when the host configures the address 0x1063 to 1, the internal state machine jumps to the system_sleep_in state and waits for the host to wake up. After the host is ready , the system jumps from the system_sleep_in state to the system_sleep_out state and waits for the host to wake up the system. When the host is ready, 0x1061 the address out of the highest register of 1, ET039XGH01-G enter the state of display_on, and wait for the host to be ready for the image that needs to be realistic. When the host has the image ready, it can set the address 0x1062 at the highest position in the register.

The microdisplay automatically receives the signal from the image transmission and starts the image transmission. If the microdisplay does not receive a signal for the image display, or if the host sets the register at 0x1061 to 0, the internal state machine jumps back to the system_sleep_out state and waits for further operations by the host.

4.11 Gamma-related configurations

The built-in EEPROM memory chip of the microdisplay can store 128 sets of data, and users can store the relevant register configurations such as VCOM voltage, TOP, and Gamma binding points in order to EEPROM.

At the same time, users can also read and write the stored EEPROM data to the OLED in turn, and the EEPROM data can be directly called when the panel is powered on without manual reconfiguration, the specific read and write configuration methods are as follows:

1. Create an empty array.
2. Use the I2C function to access the eeprom_addr (0xa0) and read the eeprom data into the new array.
3. Use the for statement to write the Vcom voltage and gamma-related registers to the display in turn, and call the solidified EEPROM data after the screen is powered on.

Note： When our OLED leaves the factory, 128 groups of registers have been solidified into the EEPROM, if the user needs to write the EEPROM data to the OLED panel in turn when programming by himself, we can provide technical support and assist the user in test verification.

The following is the order in which we solidify the relevant registers to EEPROM:

No	EEPROM Addr(8bits)	E_Storage_ Addr_ Allocation(Bytes)	DDIC_Reg	Reg_functions_Description
0	0x50	0x0	0068	VCOM L
1	0x50	0x1	0069	VCOM H
2	0x50	0x2	2100	VGAM_R_TOP_SET H
3	0x50	0x3	2101	VGAM_R_TOP_SET L
4	0x50	0x4	2106	VGAM_G_TOP_SET H
5	0x50	0x5	2107	VGAM_G_TOP_SET L
6	0x50	0x6	210C	VGAM_B_TOP_SET H
7	0x50	0x7	210D	VGAM_B_TOP_SET L
8	0x50	0x8	4022	R_gamma 0 H
9	0x50	0x9	4023	R gamma 0 L
10	0x50	0xA	4024	R_gamma 1 H
11	0x50	0xB	4025	R gamma 1 L
12	0x50	0xC	4026	R_gamma 2 H
13	0x50	0xD	4027	R gamma 2 L
14	0x50	0xE	4028	R_gamma 3 H
15	0x50	0xF	4029	R gamma 3 L
16	0x50	0x10	402A	R_gamma 4 H
17	0x50	0x11	402B	R gamma 4 L
18	0x50	0x12	402C	R_gamma 5 H
19	0x50	0x13	402D	R gamma 5 L
20	0x50	0x14	402E	R_gamma 6 H
21	0x50	0x15	402F	R gamma 6 L
22	0x50	0x16	4030	R_gamma 7 H
23	0x50	0x17	4031	R gamma 7 L
24	0x50	0x18	4032	R_gamma 8 H

No	EEPROM Addr(8bits)	E_Storage_ Addr_ Allocation(Bytes)	DDIC_Reg	Reg_functions_Description
25	0x50	0x19	4033	R gamma 8 L
26	0x50	0x1A	4034	R_gamma 9 H
27	0x50	0x1B	4035	R gamma 9 L
28	0x50	0x1C	4036	R_gamma 10 H
29	0x50	0x1D	4037	R gamma 10 L
30	0x50	0x1E	4038	R_gamma 11 H
31	0x50	0x1F	4039	R gamma 11 L
32	0x50	0x20	403A	R_gamma 12 H
33	0x50	0x21	403B	R gamma 12 L
34	0x50	0x22	403C	R_gamma 13 H
35	0x50	0x23	403D	R gamma 13 L
36	0x50	0x24	403E	R_gamma 14 H
37	0x50	0x25	403F	R gamma 14 L
38	0x50	0x26	4040	R_gamma 15 H
39	0x50	0x27	4041	R gamma 15 L
40	0x50	0x28	4042	R_gamma 16 H
41	0x50	0x29	4043	R gamma 16 L
42	0x50	0x2A	4044	G_gamma 0 H
43	0x50	0x2B	4045	G gamma 0 L
44	0x50	0x2C	4046	G_gamma 1 H
45	0x50	0x2D	4047	G gamma 1 L
46	0x50	0x2E	4048	G_gamma 2 H
47	0x50	0x2F	4049	G gamma 2 L
48	0x50	0x30	404A	G_gamma 3 H
49	0x50	0x31	404B	G gamma 3 L
50	0x50	0x32	404C	G_gamma 4 H
51	0x50	0x33	404D	G gamma 4 L
52	0x50	0x34	404E	G_gamma 5 H
53	0x50	0x35	404F	G gamma 5 L
54	0x50	0x36	4050	G_gamma 6 H
55	0x50	0x37	4051	G gamma 6 L
56	0x50	0x38	4052	G_gamma 7 H
57	0x50	0x39	4053	G gamma 7 L
58	0x50	0x3A	4054	G_gamma 8 H
59	0x50	0x3B	4055	G gamma 8 L
60	0x50	0x3C	4056	G_gamma 9 H
61	0x50	0x3D	4057	G gamma 9 L
62	0x50	0x3E	4058	G_gamma 10 H
63	0x50	0x3F	4059	G gamma 10 L
64	0x50	0x40	405A	G gamma 11 H
65	0x50	0x41	405B	G gamma 11 L
66	0x50	0x42	405C	G_gamma 12 H
67	0x50	0x43	405D	G gamma 12 L
68	0x50	0x44	405E	G_gamma 13 H

No	EEPROM Addr(8bits)	E_Storage_ Addr_ Allocation(Bytes)	DDIC_Reg	Reg_functions_Description
69	0x50	0x45	405F	G gamma 13 L
70	0x50	0x46	4060	G_gamma 14 H
71	0x50	0x47	4061	G gamma 14 L
72	0x50	0x48	4062	G_gamma 15 H
73	0x50	0x49	4063	G gamma 15 L
74	0x50	0x4A	4064	G_gamma 16 H
75	0x50	0x4B	4065	G gamma 16 L
76	0x50	0x4C	4066	B_gamma 0 H
77	0x50	0x4D	4067	B gamma 0 L
78	0x50	0x4E	4068	B_gamma 1 H
79	0x50	0x4F	4069	B gamma 1 L
80	0x50	0x50	406A	B_gamma 2 H
81	0x50	0x51	406B	B gamma 2 L
82	0x50	0x52	406C	B_gamma 3 H
83	0x50	0x53	406D	B gamma 3 L
84	0x50	0x54	406E	B_gamma 4 H
85	0x50	0x55	406F	B gamma 4 L
86	0x50	0x56	4070	B_gamma 5 H
87	0x50	0x57	4071	B gamma 5 L
88	0x50	0x58	4072	B_gamma 6 H
89	0x50	0x59	4073	B gamma 6 L
90	0x50	0x5A	4074	B_gamma 7 H
91	0x50	0x5B	4075	B gamma 7 L
92	0x50	0x5C	4076	B_gamma 8 H
93	0x50	0x5D	4077	B gamma 8 L
94	0x50	0x5E	4078	B_gamma 9 H
95	0x50	0x5F	4079	B gamma 9 L
96	0x50	0x60	407A	B_gamma 10 H
97	0x50	0x61	407B	B gamma 10 L
98	0x50	0x62	407C	B_gamma 11 H
99	0x50	0x63	407D	B gamma 11 L
100	0x50	0x64	407E	B_gamma 12 H
101	0x50	0x65	407F	B gamma 12 L
102	0x50	0x66	4080	B_gamma 13 H
103	0x50	0x67	4081	B gamma 13 L
104	0x50	0x68	4082	B_gamma 14 H
105	0x50	0x69	4083	B gamma 14 L
106	0x50	0x6A	4084	B_gamma 15 H
107	0x50	0x6B	4085	B gamma 15 L
108	0x50	0x6C	4086	B gamma 16 H
109	0x50	0x6D	4087	B gamma 16 L
110	0x50	0x6E	4021	Gamma Point 255
111	0x50	0x6F	401F	Gamma Point 239
112	0x50	0x70	401D	Gamma Point 223

No	EEPROM Addr(8bits)	E_Storage_ Addr_ Allocation(Bytes)	DDIC_Reg	Reg_functions_Description
113	0x50	0x71	401B	Gamma Point 207
114	0x50	0x72	4019	Gamma Point 191
115	0x50	0x73	4017	Gamma Point 175
116	0x50	0x74	4015	Gamma Point 159
117	0x50	0x75	4013	Gamma Point 143
118	0x50	0x76	4011	Gamma Point 127
119	0x50	0x77	400F	Gamma Point 111
120	0x50	0x78	400D	Gamma Point 95
121	0x50	0x79	400B	Gamma Point 79
122	0x50	0x7A	4009	Gamma Point 63
123	0x50	0x7B	4007	Gamma Point 47
124	0x50	0x7C	4005	Gamma Point 15
125	0x50	0x7D	4003	Gamma Point 1
126	0x50	0x7E	4001	Gamma Point 0
127	0x50	0x7F	20E9/20EB/20ED	Gamma bottom

4.12 Serial interface

The I2C serial interface allows the user to set or read the values of the registers inside the screen. The I2C serial interface communication mode conforms to the standard communication protocol, and the host can realize the functions of test screen selection, brightness adjustment, contrast adjustment, temperature reading and other functions by reading and writing the internal registers of the micro display. The communication rate supports 10KHz~400KHz.

note:

When the I2C communication signal transmission distance is long, attention should be paid to the signal integrity and

When the I2C communication signal is seriously interfered with, I2C communication can be carried out during the field

4.12.1 Select the slave address

The microdisplay is used as a slave and the address can be selected by the I²C ADDR0 pin level, and in binocular applications, connect one of the displays, I²C ADDR0, to ground. Table 20 shows the read/write addresses of the corresponding displays.

Table 20 Microdisplay I2C Slave Address Description Table

	A6	A5	A4	A3	A2	(I²C ADDR0)	(R/$\overline{w}$)	(R/$\overline{w}$)
0	0	0	1	1	1	0	1/0	1DH/1CH
0	0	0	1	1	1	1(default)	1/0	1FH/1EH

4.12.2 Data Transfer Format

4.12.2.1 Description of the flag

Start Signal (S): The change of the SDA line from high to low during the period when the SCL line is high;

Termination Signal (P): The change of the SDA line from low to high during the period when the SCL line is high, as shown in Figure 8;

Effected Response (ACK): SDA is low to indicate active response;

No Response (NAK): SDA is high to indicate no response;

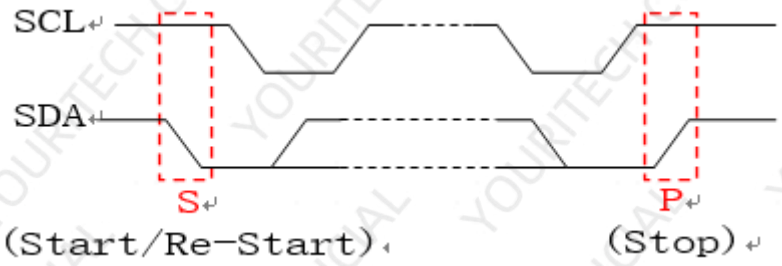


Figure 8 Diagram of the start and end signals on the I2C bus

4.12.2.2 Write data

S	Slave Addr	$\overline{W}$	A	Register	A	Data	A	P

Figure 9 Schematic diagram of the format in which the master writes data to the slave

4.12.2.3 Read data

S	Slave Addr	$\overline{W}$	A	Register	A	Sr	Slave Addr	R	A	Data	$\overline{A}$	P

Figure 10 Schematic diagram of the master-to-slave machine-readable data format

4.13 Example register configuration

4.13.1 Initialization reference code

```
#define  OLED039_slaveadr       0x1E    //7bit, selAdr = 1(0x1E), selAdr = 0(0x1C)
#define  unsigned char          u8

void oled039_WriteData(u8 regadr_h,  u8 regadr_l, u8 data)
{
        Write1byte(OLED039_slaveadr, regadr_h, regadr_l, data);
}

void oled039_init(void)
{
   oled039_WriteData(0x00,0x60,0x0b);//clock_control
```

```
oled039_WriteData(0x20,0x6f,0x00);//luminance_sel[1:0]
oled039_WriteData(0x10,0x18,0x10);//dgma_lut_rw_en[5],luminance_rw_sel[1:0]
oled039_WriteData(0x20,0x30,0x01);//remap_en[0]
oled039_WriteData(0x20,0x53,0x00);//h_channel_start[7:0]
oled039_WriteData(0x20,0x54,0x81);//h_channel_end[7:0]
oled039_WriteData(0x20,0x41,0x08);//h_front_dummy[5:0]
oled039_WriteData(0x20,0x42,0x08);//h_back_dummy[5:0]
oled039_WriteData(0x20,0xd3,0x00);//pwn_duty_0[10:8]
oled039_WriteData(0x20,0xd4,0x00);//pwn_duty_0[7:0]
oled039_WriteData(0x20,0xd0,0x11);//pwn_force_en
oled039_WriteData(0x20,0xd1,0x01); //pwn_force_num[4:0]
oled039_WriteData(0x20,0x31,0x31);//dgma_en
oled039_WriteData(0x00,0x12,0x00);
oled039_WriteData(0x20,0x80,0x01);
oled039_WriteData(0x20,0x86,0x03);//pwm_en_0[7:0]
oled039_WriteData(0x20,0x85,0x00);//pwm_en_0[15:8]
oled039_WriteData(0x20,0x1a,0x99);//255 gray adjust [7:0]
oled039_WriteData(0x20,0x1b,0x04);//255 gray adjust [3:0]
oled039_WriteData(0x20,0x07,0x00);//vactive[7:0](Vertical active pixel)
oled039_WriteData(0x20,0x08,0x03);//vactive[11:8]
oled039_WriteData(0x20,0x6e,0x07);//ud_sel[2:0] Vertical scan direction  +
oled039_WriteData(0x20,0x6d,0x00);//lr_sel[2:0] Horizontal scan direction +
oled039_WriteData(0x20,0x28,0x00);//
oled039_WriteData(0x20,0x28,0x01);//update_vsetting[0]
oled039_WriteData(0x20,0x00,0x01);//vsetting_en[0]
oled039_WriteData(0x20,0x5c,0x37);
oled039_WriteData(0x10,0x00,0x03);//hs/vs_polar=1 active high
oled039_WriteData(0x00,0x11,0xff);//en dgma clock
oled039GammaRead();
oled039_WriteData(0x20,0xf0,0x01);//vcom_en
oled039_WriteData(0x00,0x55,0x29);
oled039_WriteData(0x00,0x26,0x01);
oled039_WriteData(0x10,0x07,0x07);//Anode_pixel_en
oled039_WriteData(0x10,0x08,0xff);//Anode_pixelg_gain
DELAY_milliseconds(1000);
oled039_WriteData(0x10,0x63,0x80);//system_boot_on
oled039_WriteData(0x10,0x61,0x80);//system_sleep_out
oled039_WriteData(0x10,0x62,0x80);//display_on
}
```

4.13.2 Eeprom read and write reference code

```
#define  eeprom_adr          0xA0    //7bit
#define  unsigned char        u8

void EEPROM_ReadBlock (u8 address,  u8  regaddress, u8 *tab, u8  bytelength)
{
        ReadNbyte(address, regaddress, tab, bytelength);
}

void oled039GammaRead(void)  // gamma read
{
```

```
    static unsigned char gammaTab[128];
    static unsigned char j = 0 ; // X_GAMMA
    EEPROM_ReadBlock(eeprom_adr, 0, &gammaTab, 128); // Read EEPROM storage data once
    __delay_ms(10);
    if((gammaTab[8]==0)&&(gammaTab[42]==0)&&(gammaTab[76]==0)) //dgam write in oled sequentially
    {
       oled039_WriteData(0x00, 0x68, gammaTab[0]);//vcom_L[7:0]
       oled039_WriteData(0x00, 0x69, gammaTab[1]);//vcom_H[1:0]

  //gamma_top 0x2100~0x2101, 0x2106~0x2107, 0x210c~0x210d
       for(unsigned char i=0; i<2; i++)
       {
          oled039_WriteData(0x21, i, gammaTab[i+2]);// red voltage0 adjust
          oled039_WriteData(0x21, i+6, gammaTab[i+4]);//green voltage0 adjust
          oled039_WriteData(0x21, i+12, gammaTab[i+6]);//blue voltage0 adjust
       }
  //gamma_bottom 0x20e9~0x20ed
       for(unsigned char i=0; i<5; i=i+2)
       {
          oled039_WriteData( 0x20, i+233, gammaTab[127]);//R/G/B voltage0 adjust
       }
       oled039_WriteData( 0x10, 0x18, 0x31);//config dgma_upgrade [5:4]

    //Y GAMMA_R_G_B  0x4022~0x4087
       for(unsigned char i=0; i<102; i++)
       {
          oled039_WriteData(0x40, i+34, gammaTab[i+8]);//[1:0]
       }
  //X_GAMMA 绑点 0x4021~0x4001
       for(unsigned char i=0; i<17; i++)
       {
          oled039_WriteData( 0x40, 33-j, gammaTab[i+110]);//[7:0]
          j = j + 2;
       }
       oled039_WriteData( 0x10, 0x18, 0x11);//config dgma_upgrade_done [5]
    }
    else
    {
       printf("eeprom0_write_fail!\r\n");
    }
    }
```

5 Optical characteristics

5.1 Optical specifications

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Luminance	Lbr	Using Built-in test pattern under typical test conditions and all pixels are fully on	-	200	-	cd/㎡
Power consumption	Pt		-	65	-	mW
luminance uniformity		The average of five test points	90	95	100	%
Chromaticity (W)	CIE-x	all pixels are fully on	0.28	0.31	0.34	-
	CIE-y		0.30	0.33	0.36	-
Chromaticity (R)	CIE-x	all red are sub-pixels fully on	0.57	0.60	0.63	-
	CIE-y		0.30	0.33	0.36	-
Chromaticity (G)	CIE-x	all green are sub-pixels fully on	0.20	0.23	0.26	-
	CIE-y		0.60	0.63	0.66	-
Chromaticity (B)	CIE-x	all blue are sub-pixels fully on	0.11	0.14	0.17	-
	CIE-y y		0.04	0.07	0.10	-
Contrast	CR	Highest gray: Minimum gray	≥31000:1	-	-	-

5.2 Pixel Array

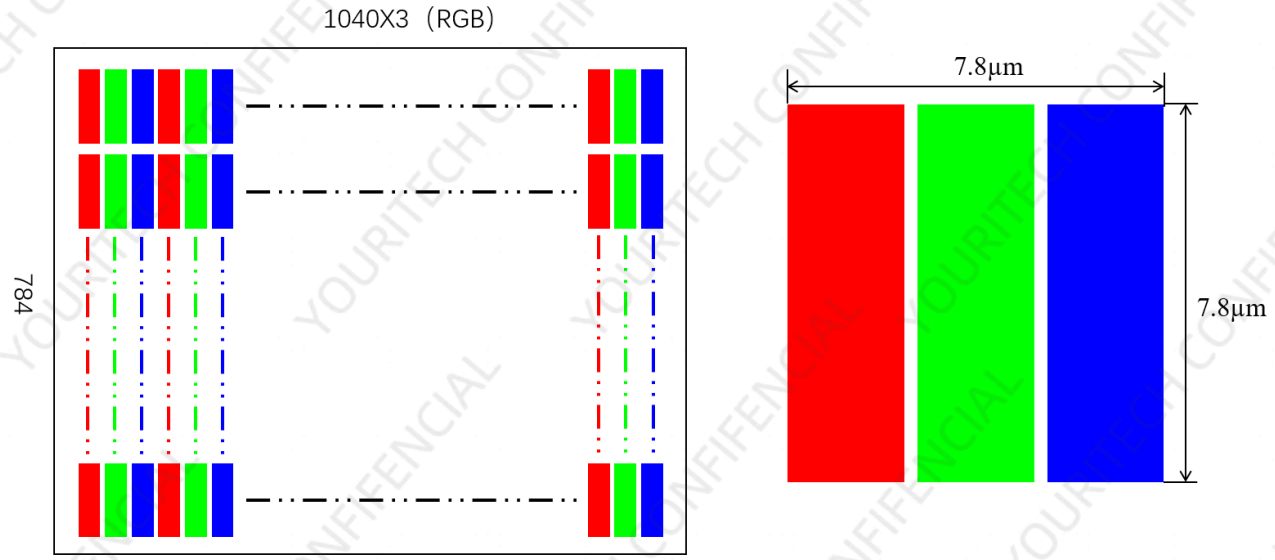


Figure 11 Schematic diagram of the pixel array

The pixel arrangement of a ET039XGH01-G is shown in Figure 11, where every three subpixels form a pixel with a pixel size of 7.8цm×7.8цm.

5.3 Display quality standards

5.3.1 Display area definition

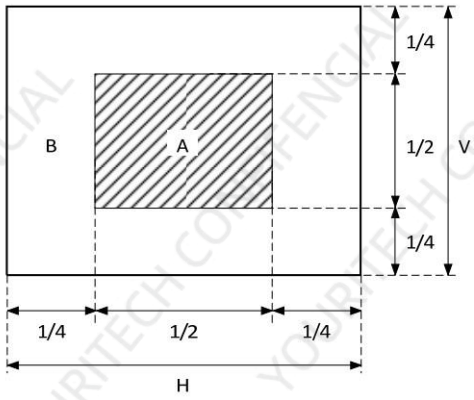


Figure 12 Display area definition

5.3.2 Defect inspection criteria

Blemishes and defects are subpixels that don't display correctly, such as solid light pixels or often dark pixels. The inspection criteria for defects shall be carried out in accordance with the requirements of Table 21.

Table 21 Requirements for visual defect inspection

No.	Items	requirements
1	2 consecutive pixel dead pixels	Area A no more than 1, and no more than 3 full-screen
2	3 or more consecutive dead pixels	No more than 1 full-screen
3	bright spot	30 Grayscales have no bright spots
4	bad wires	None

5.3.3 Inspection conditions

2) Use a special test fixture to light up the microdisplay, which shows black point, and use a 12× eyepiece

6 Structure & Packaging

6.1 Product Structure

The micro display is 16.6mm×14.2mm, and the other dimensions are shown in Figure 13.

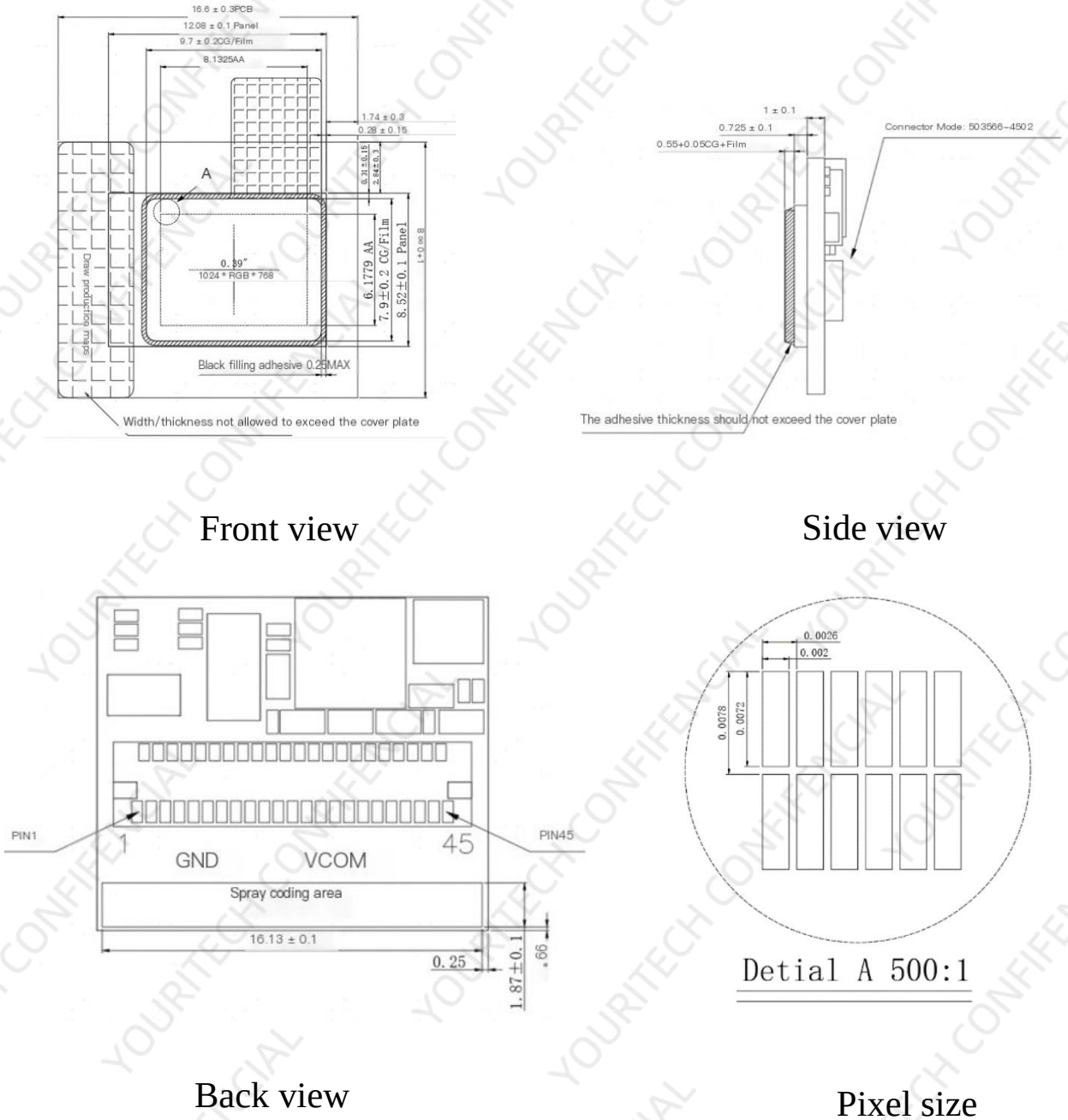


Figure 13 Microdisplay dimensions

6.2 Connector size and FPC design recommendations

Unit：mm

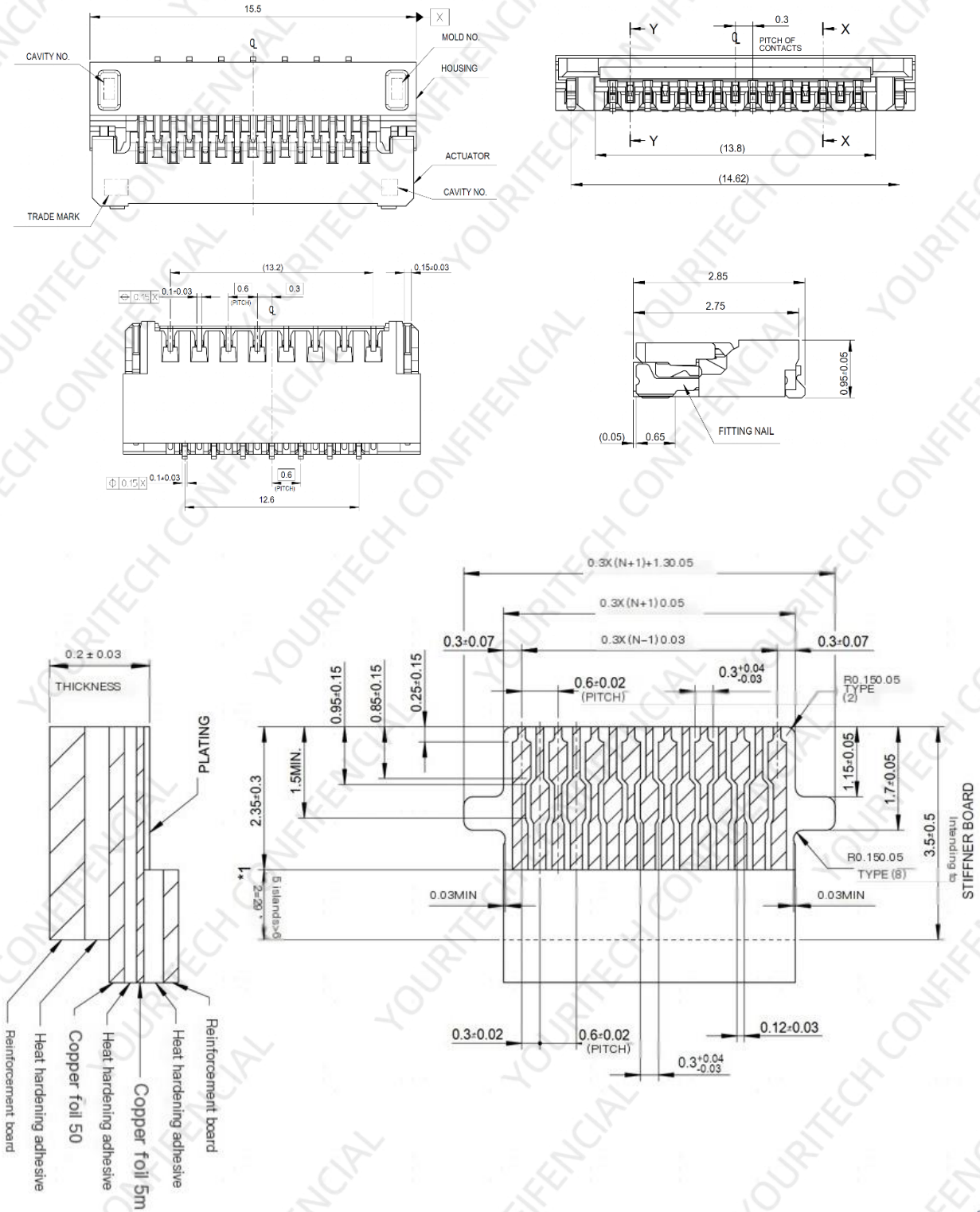


Figure 14 Connector size and FPC layout recommended size

Note： When the FPC is plugged in, the gold finger is facing the carrier board frontally.

7 Product Considerations

7.1 Cleaning

- Avoid using any acid, alkali and organic solvent to clean or contact to the display.
- Using the lens paper or clean cloth to clean the surface is recommend.

7.2 General Handling Considerations

- Do not expose the display to strong acids, alkalis, or solvents.
- Do not expose the display surface to UV or other strong ionizing radiation.
- Do not using sharp objects to contact the glass and silicon regions of display.
- Avoid applying force to the any region except the PCB backplane, especially apply the force to the region of sealing, silicon edge and cover glass is not allowed.
- Avoid immersion of the display in any liquid.
- Handing with PVC clean gloves is recommended.

7.3 Static Charge Prevention

The microdisplay is sensitive to electro-static discharge due to integrated CMOS circuit in the display. The following measures are recommended to minimize ESD occurrences:

- Operate on a region which is equipped with electro-static eliminator, such as ionizing air blowers.
- Wear the anti-static wrist strap.
- wear the non-chargeable clothes.
- Keep away from charged region.

7.4 Storage

7.4.1 Short Term Storage:

The display should be stored in a dry environment with temperature range from -50℃ to 90℃ for a short period(≤100hrs).

7.4.2 Long Term Storage:

If the display is stored in such an environment with excessive heat or cold or moisture, the lifetime of display will be shorten, even the environment can cause permanent damage to the display. Recommended long-term storage condition as follows:

- Room temperature: 25℃±5℃.
- Dry environment: dry nitrogen or vacuum sealing cabinet.
- Static placing: avoid violent vibration.
