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**MODEL NO : ET040VG01-T**

**MODEL VERSION: 01**

**SPEC VERSION : 1.0**

**ISSUED DATE: 2022-12-20**

**□Preliminary Specification**

**■Final Product Specification**

**Customer :**

| Approved by | Notes |
|---|---|
| | |

**Youri Confirmation**

| Prepared by | Reviewed by | Approved by |
|---|---|---|
| John | Johnny | Wang |

# 1. Introduction

## 1.1 Scope of application

LCD specification: Dots 640xRGBx480
As to basic specification of the driver IC, refer to the IC (NV3051F1) specification and data book.
All material & processing of the LCD module should be Lead Free.

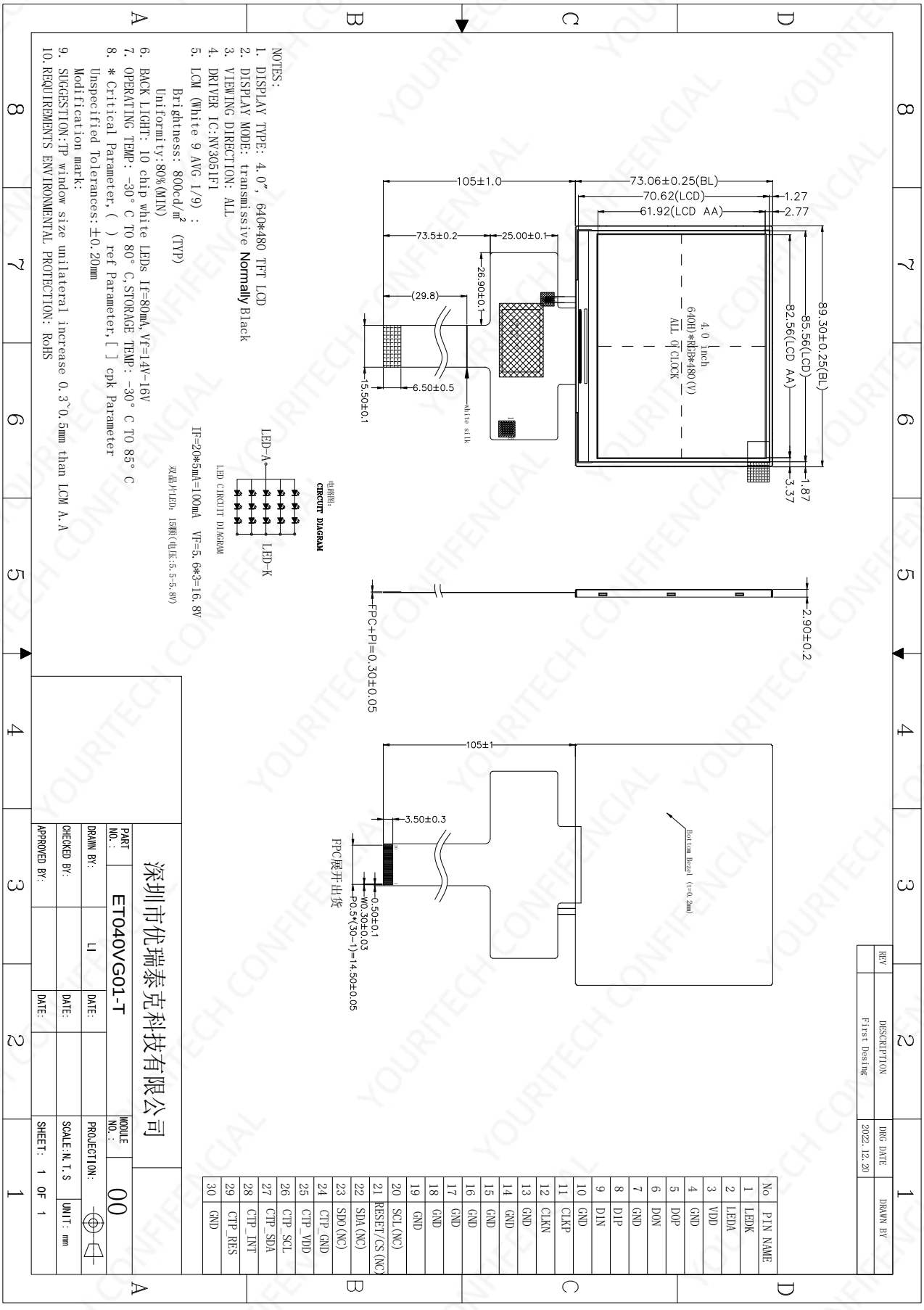
## 1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;
ALL Viewing Type LCD
640 dot-segment and 480 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
2lane MIPI interface

## 1.3 Applications:

## 2. LCM General specification

| ITEM | Sandard value | Unit |
|---|---|---|
| LCD Type | Normally Black | -- |
| Drive element | TFT active matrix | -- |
| Number of pixels | 640*3RGB(H)X480(V) | Dots |
| Pixel arrangement | RGB Vertical Stripe | -- |
| Pixel Pitch (W*H) | 0.129H) X 0.129(V) | mm |
| Active area | 82.56(H) x 61.92(V) | mm |
| Viewing direction | ALL O'CLOCK | -- |
| TFT Driver IC | NV3051F1 | -- |
| TFT interface | 2lane MIPI interface | -- |
| Approx. Weight | TBD | g |
| LCM Size(W*H*T) | 89.30(W) ×73.06(H) ×2.90(T) | mm |
| Touch structure | -- | -- |
| Touch Driver IC | -- | -- |
| Touch Interface | -- | -- |




NOTES:

1. DISPLAY TYPE: 4.0", 640*480 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL
4. DRIVER IC:NV3051F1
5. LCM (White 9 AVG 1/9) :
   Brightness: 800cd/$m^2$ (TYP)
   Uniformity:80%(MIN)
6. BACK LIGHT: 10 chip white LEDs If=80mA,Vf=14V-16V
7. OPERATING TEMP: -30° C TO 80° C,STORAGE TEMP: -30° C TO 85° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS

| No | PIN NAME |
|---|---|
| 1 | LEDK |
| 2 | LEDA |
| 3 | VDD |
| 4 | GND |
| 5 | DOP |
| 6 | DON |
| 7 | GND |
| 8 | D1P |
| 9 | D1N |
| 10 | GND |
| 11 | CLKP |
| 12 | CLKN |
| 13 | GND |
| 14 | GND |
| 15 | GND |
| 16 | GND |
| 17 | GND |
| 18 | GND |
| 19 | GND |
| 20 | SCL(NC) |
| 21 | RESET/CS (NC) |
| 22 | SDA(NC) |
| 23 | SDO(NC) |
| 24 | CTP_GND |
| 25 | CTP_VDD |
| 26 | CTP_SCL |
| 27 | CTP_SDA |
| 28 | CTP_INT |
| 29 | CTP_RES |
| 30 | GND |

| REV | DESCRIPTION | DRG DATE | DRAWN BY |
|---|---|---|---|
| | First Desing | 2022.12.20 | |

深圳市优瑞泰克科技有限公司

| | | | |
|---|---|---|---|
| PART NO.: | ET040VG01-T | MODULE NO.: | 00 |
| DRAWN BY: | LI | PROJECTION: | |
| CHECKED BY: | | SCALE:N.T.S | UNIT: mm |
| APPROVED BY: | | SHEET: 1 OF 1 | |

# 3.Absolute Maximum Rating

| Characteristics | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| LCM Operating Temperature | $T_{OPR}$ | -30 | +80 | °C |
| LCM Storage Temperature | $T_{STG}$ | -30 | +85 | °C |
| Humidity | RH | -- | 90 | % |

# 4.Electrical Characteristics

## 4.1 TFT DC Characteristics

| Characteristics | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply Voltage for I/O | I/O | -- | -- | -- | V |
| Supply Voltage for(DC/DC) | VDD | 2.7 | 2.8 | 3.6 | V |
| Current Consumption | $I_{DD}$ | -- | -- | -- | mA |
| | $I_{DD-SLEEP}$ | -- | -- | -- | uA |

## 4.2 Back-Light Unit Characeristics

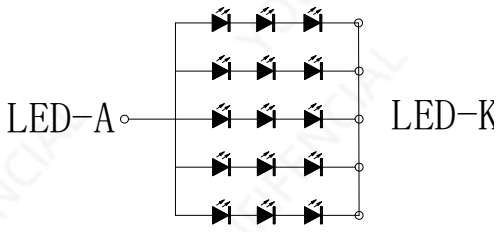
The back-light system is an edge-lighting type with 15 white LEDs. The characteristics of the back-light are shown in the following tables.

| Characteristics | Symbol | Min. | Type | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Forward Voltage | $V_F$ | 14 | -- | 16 | V | -- |
| Forward current | $I_F$ | -- | 80 | -- | mA | -- |
| Luminance(With LCD) | Lv | -- | 800 | -- | $cd/m^2$ | -- |
| LED life time | N/A | ---- | 30,000 | -- | Hr | Note 1 |

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at $I_L$=20mA/LED. The LED life time could be decreased if operating $I_L$ is larger than 25mA/LED.

**Backlight circuit diagram shown in below:**



# 5. Module Function Description

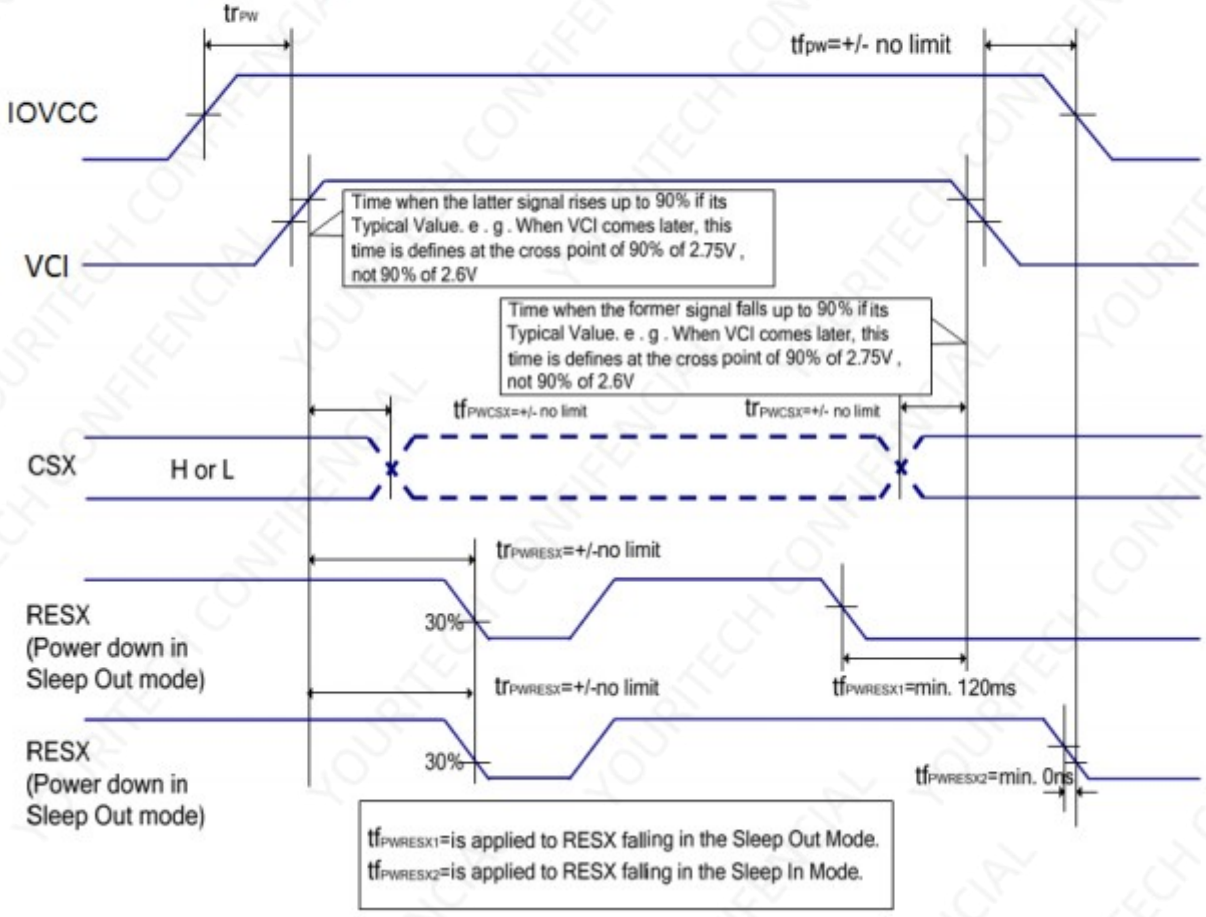
| Pin No. | Symbol | LCM Functional | Notes |
|---|---|---|---|
| 1 | LEDK | Power supply for backlight cathode input terminal. | |
| 2 | LEDA | Power supply for backlight anode input terminal. | |
| 3 | VDD | Power Supply For LCD. | |
| 4 | GND | Power Ground | |
| 5 | MIPI_D0P | MIPI-DSI Data differential signal input pins | |
| 6 | MIPI_D0N | MIPI-DSI Data differential signal input pins | |
| 7 | GND | Power Ground | |
| 8 | MIPI_D1P | MIPI-DSI Data differential signal input pins | |
| 9 | MIPI_D1N | MIPI-DSI Data differential signal input pins | |
| 10 | GND | Power Ground | |
| 11 | CLKP | MIPI-DSI CLOCK differential signal input pins | |
| 12 | CLKN | MIPI-DSI CLOCK differential signal input pins | |
| 13-19 | GND | Power Ground | |
| 20 | SCL(NC) | NC | |
| 21 | RESET/CS(NC) | NC | |
| 22 | SDA(NC) | NC | |
| 23 | SDO(NC) | NC | |
| 24 | GND | Power Ground | |
| 25 | CTP_VDD | Power Supply For LCD. | |
| 26 | CTP_SCL | Touch panel I2C clock | |
| 27 | CTP_SDA | Touch panel I2C data | |
| 28 | CTP_INT | Touch panel interrupt output | |
| 29 | CTP_RESET | Reset pin. Setting either pin low initializes the LSI | |
| 30 | GND | Power Ground | |

# 6. Timing Characteristics

## Power On/Off Sequence

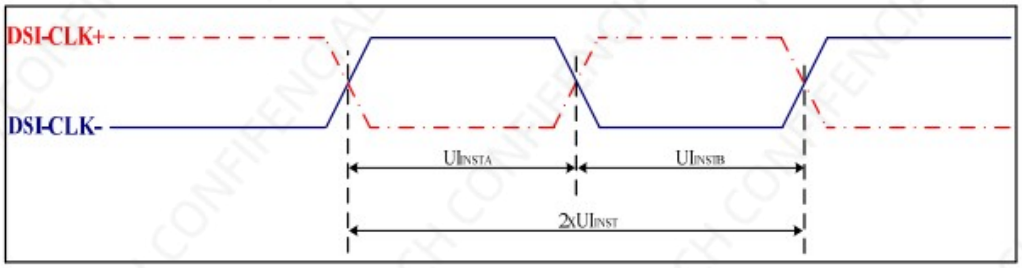
### Case 1 – RESX line is held high or unstable by host at power on

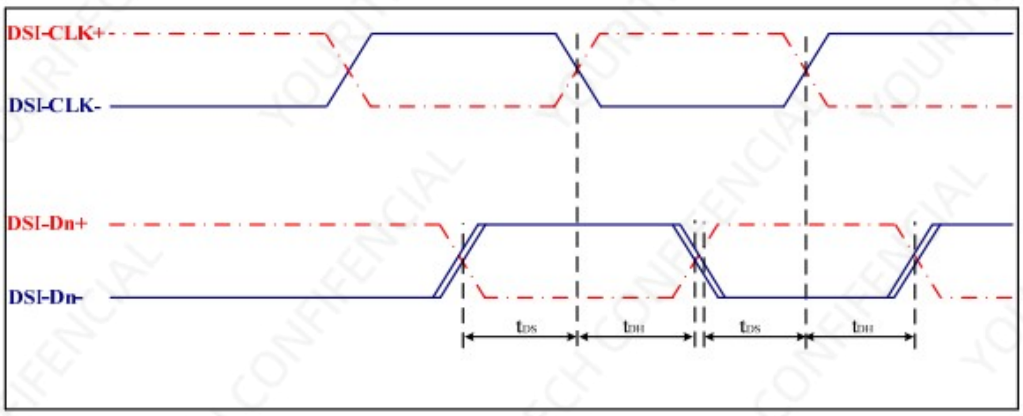
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



**High speed mode**

| Parameter | Symbol | Parameter | Specification | | | Unit |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **High Speed Mode** | | | | | | |
| DSI-CLK+/- | $2Xui_{inst}$ | Double UI instantaneous | 2.22 | - | 25 | ns |
| DSI-CLK+/- | $UI_{INSTA}$ , $UI_{INSTB}$ | UI instantaneous Halfs | 1.11 | - | 12.5 | ns |
| DSI-Dn+/- | $T_{ds}$ | Data to clock setup time | 0.15 | - | - | UI |
| DSI-Dn+/- | $T_{dh}$ | Data to clock hold time | 0.15 | - | - | UI |
| DSI-CLK+/- | $T_{drclk}$ | Differential rise time for clock | 150 | - | 0.3UI | ps |
| DSI-Dn+/- | $T_{drdata}$ | Differential rise time for data | 150 | - | 0.3UI | ps |
| DSI-CLK+/- | $T_{dfclk}$ | Differential fall time for clock | 150 | - | 0.3UI | ps |
| DSI-Dn+/- | $T_{dfdata}$ | Differential fall time for data | 150 | - | 0.3UI | ps |



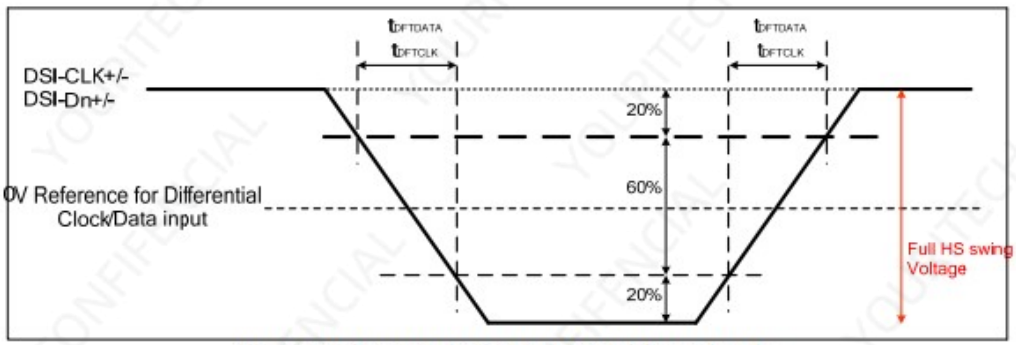




Figure: AC characteristics for MIPI-DSI High speed mode

**Low power mode**

| Parameter | Symbol | Parameter | Specification | | | Unit |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **Low Power Mode** | | | | | | |
| DSI-D0+/- | TLPXM | Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module | 50 | - | - | ns |
| DSI- D0+/- | TLPXD | Length of LP-00, LP-01, LP-10 or LP-11 periods Display Modulen MPU | 58 | - | - | ns |
| DSI- D0+/- | TTA-SURED | Time-out before the MPU start driving | TLPXD | - | 2XTLPXD | ns |
| DSI- D0+/- | TTA-GETD | Time to drive LP-00 by display module | 5XTLPXD | - | - | ns |
| DSI- D0+/- | TTA-GOD | Time to drive LP-00 after turnaround request – MPU | 4XTLPXD | - | - | ns |
| DSI- D0+/- | Ratio TLPX | Ratio of TLPXM / TLPXD between MCU and display module | 2/3 | - | 3/2 | |

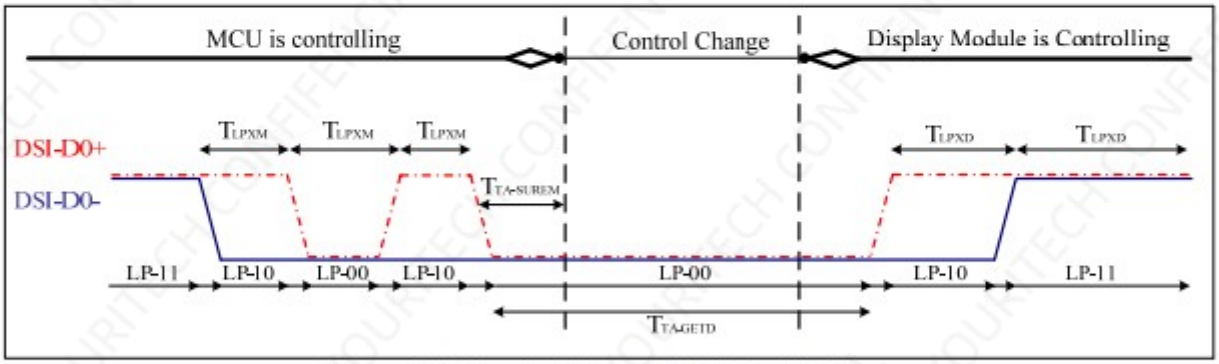



Figure: BTA from the MCU to the Display Module

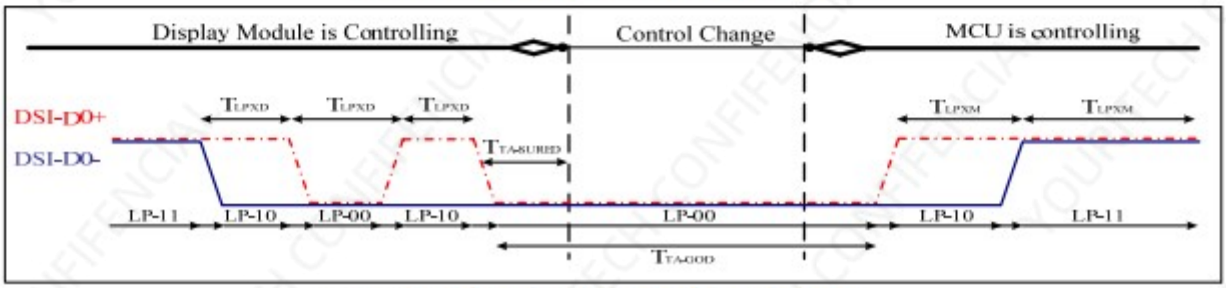



Figure: BTA from the Display Module to the MCU

**Bursts**

| Parameter | Symbol | Parameter | Specification | | | Unit |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **High Speed Data Transmission Bursts** | | | | | | |
| DSI-Dn+/- | TLPX | Length of any low-power state period | 50 | - | - | ns |
| DSI- Dn+/- | THS- PREPARE | Time to drive LP-00 to prepare for HS transmission | 40ns+4UI | - | 85ns+6UI | ns |
| DSI- Dn+/- | THS-PREPARE+THS-ZERO | THS-PREPARE+time to drive HS-0 before the sync sequence | 145ns+10UI | - | - | ns |
| DSI- Dn+/- | TD-TERM- EN | Time to enable Data Lane receiver line termination measured from when Dn crosses VIL(max) | Time for Dn to reach VTERM-EN | - | 35ns+4UI | ns |
| DSI- Dn+/- | THS-SKIP | Time-out at RX to ignore transition period of EoT | 40 | - | 55ns+4UI | ns |
| DSI- Dn+/- | THS-TRAIL | Time to drive flipped differential state after last payload data bit of a HS transmission burst | max (8UI, 60ns+4UI) | - | - | ns |
| DSI- Dn+/- | THS-EXIT | Time to drive LP-11 after HS burst | 100 | - | - | ns |
| DSI- Dn+/- | TeoT | Time from start of THS-TRAIL period to start of LP-11 state | - | - | 105ns+12UI | ns |

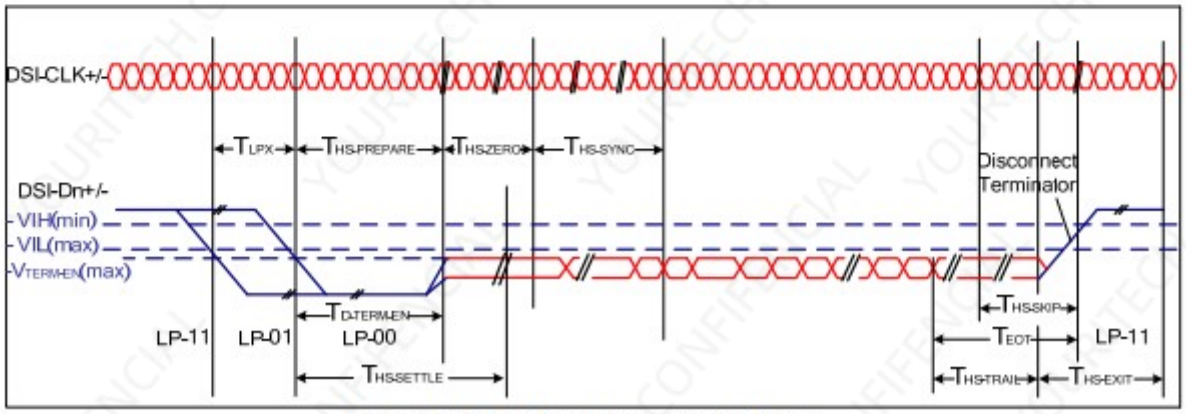



Figure: High Speed Data Transmission Bursts

| Parameter | Symbol | Parameter | Specification | | | Unit |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **Switching the clock Lane between clock Transmission and Low Power Mode** | | | | | | |
| DSI-CLK+/- | TCLK-POST | Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode | 60ns+52UI | - | - | ns |
| DSI-CLK+/- | TCLK-PRE | Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode | 8 | - | - | UI |
| DSI-CLK+/- | TCLK-PREPARE | Time to drive LP-00 to prepare for HS clock transmission | 38 | - | 95 | ns |
| DSI-CLK+/- | TCLK-TERM- EN | Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$ | Time for Dn to reach VTERM-EN | - | 38 | ns |
| DSI- CLK+/- | TCLK-PREPARE +TCLK-ZERO | TCLK-PREPARE + time for lead HS-0 drive period before starting Clock | 300 | - | - | ns |
| DSI- CLK+/- | TCLK-TRAIL | Time to drive HS differential state after last payload clock bit of a HS transmission burst | 60 | - | - | ns |
| DSI-CLK+/- | TeoT | Time from start of TCLK-TRAIL period to start of LP-11 state | - | - | 105ns+ 12UI | ns |

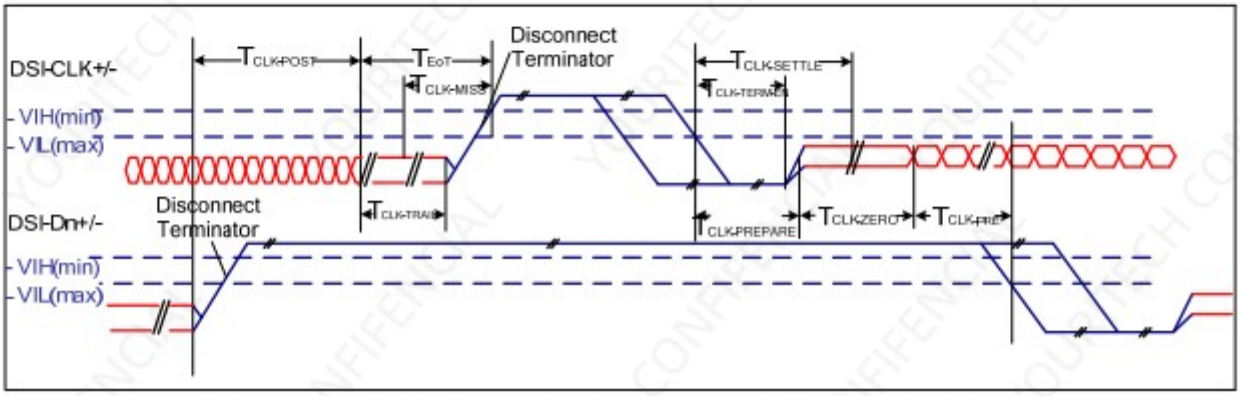
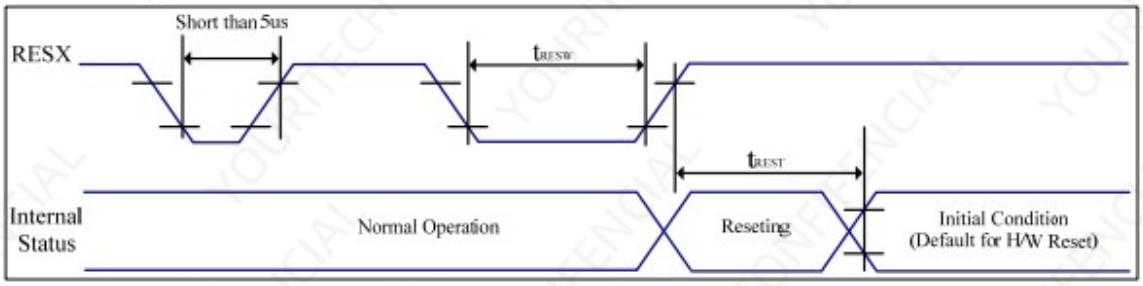



Figure: Switching the clock Lane between clock Transmission and Low Power Mode

**Reset timing characteristics**




VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V, Ta = -30℃ to 70℃

| Symbol | Parameter | Related Pins | MIN | TYP | MAX | Note | Unit |
|---|---|---|---|---|---|---|---|
| $T_{resw}$ | *1) Reset low pulse width | RESX | 10 | - | - | - | us |
| $T_{rest}$ | *2) Reset complete time | - | - | - | 5 | When reset applied during Sleep in mode | ms |
| | | - | - | - | 120 | When reset applied during Sleep out mode | ms |

Table: Reset input timing

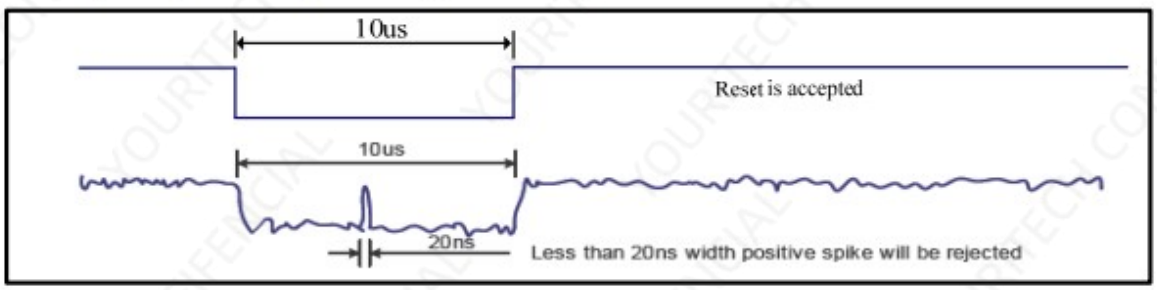
Note 1: Due to an electrostatic discharge on RESX line,spike does not cause irregular system reset according to the table below.

| RESX Pulse | Action |
|---|---|
| Shorter than 5us | Reset Rejected |
| Longer than 10us | Reset |
| Between 5us and 10us | Reset starts (It depends on voltage and temperature condition.) |

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode) , then return to default condition for H/W reset.

Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time (Trest) which lasted 5ms.The loading operation will be done every time during this reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:

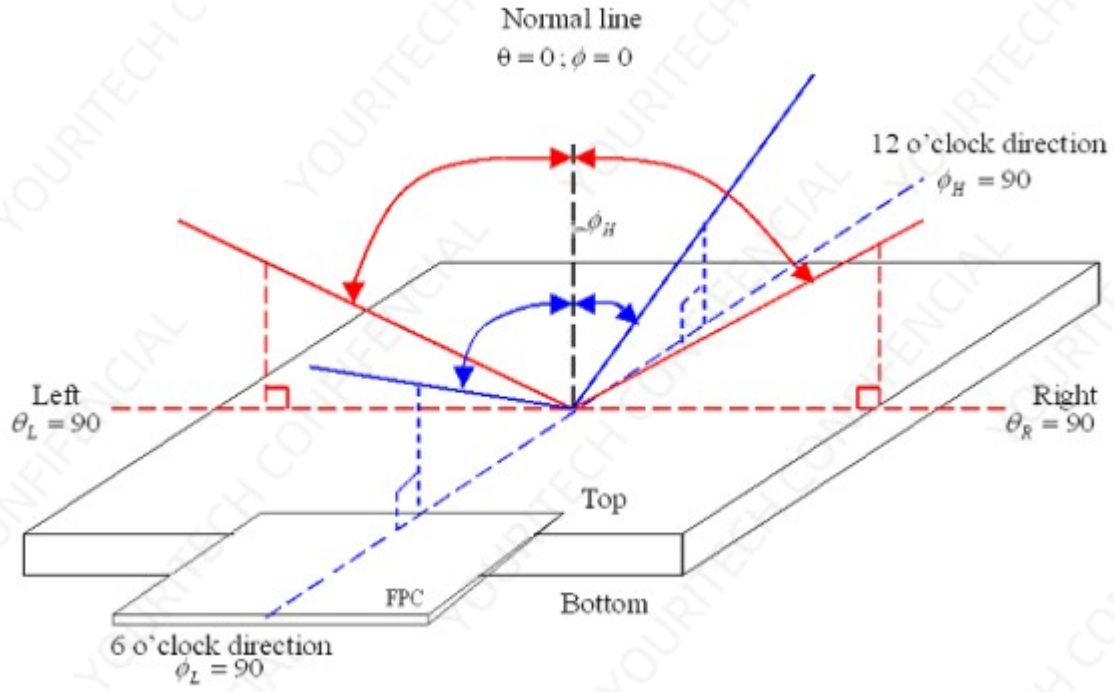



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

## 7. Optical Characteristics

**( Color Filter Chromaticity ) :**

| ITEM | | SYMBOL | CONDITION | MIN. | TYP. | MAX. |
|---|---|---|---|---|---|---|
| Color Filter Chromaticity | White | x | θ=ϕ= 0° | 0.298 | 0.318 | 0.338 |
| | | y | | 0.308 | 0.328 | 0.348 |
| | Red | x | θ=ϕ= 0° | 0.631 | 0.651 | 0.671 |
| | | y | | 0.321 | 0.341 | 0.361 |
| | Green | x | θ=ϕ= 0° | 0.238 | 0.258 | 0.278 |
| | | y | | 0.533 | 0.553 | 0.573 |
| | Blue | x | θ=ϕ= 0° | 0.123 | 0.143 | 0.163 |
| | | y | | 0.063 | 0.083 | 0.103 |
| | Gamut | | | 66.9% | | |
| Measured by C light | | | | | | |
| Transmittance | | θ=ϕ= 0° | | 2.7% | 3.1% | |
| Measured by GP standard backlight | | | | | | |



## 8. Reliability Test Item

| No. | Test Item | Test Condition | Notes |
|---|---|---|---|
| 1 | High Temp. Storage | +85°C / 96H | 1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed.<br>2. No low temperature bubbles,end seal loose andfall, frame rainbow. |
| 2 | Low Temp. Storage | -30°C / 96H | |
| 3 | High Tempe. Operating | +80°C / 96H | |
| 4 | Low Tempe. Operating | -30°C / 96H | |
| 5 | High Temperature /Humidity storage | 50°C x 90%RH /96H | |
| 6 | Thermal and cold shock | Static state，-20℃（30min）~70℃（30min），50 cycles | |

## 9. Packing Method----TBD

- END -