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Custom Display

Production Custom designs Installation

Mechanical design



MODEL NO : ET040WV02-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-05-06

☐ Preliminary Specification

☒ Final Product Specification

Customer : _____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 480xRGBx800.

As to basic specification of the driver IC, refer to the IC (Sitronix:ST7701S) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;;

IPS Type LCD

480dot-segment and 800 dot-common outputs;

16.7M Color can be selected by software;

White LED back light;

24bit RGB interface

1.3 Applications:

2. LCM General specification

ITEM	Standard value	Unit
LCD Type	Normally black	--
Drive element	TFT active matrix	--
Number of pixels	480*3RGB(H)X800(V)	Dots
Pixel arrangement	RGB stripe	--
Pixel Pitch (W*H)	0.108x0.108	mm
Active area	51.84(H) x 86.40(V)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	ST7701S	--
TFT interface	24bit RGB Interface	--
Module Size(W*H*T)	55.50(H) x 96.20(V) x2.06(T)	mm
Approx. Weight	TBD	g
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--



3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T _{OPR}	-20	+70	°C
LCM Storage Temperature	T _{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.6	2.8	3.6	V
Supply Voltage for(DC/DC)	AVDD	--	--	--	V
Supply Voltage for(DC/DC)	AVEE	--	--	--	V

4.2 Back-Light Unit Characeristics

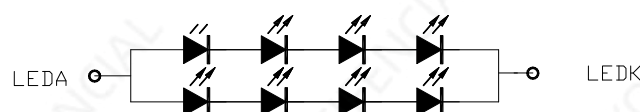
The back-light system is an edge-lighting type with 8 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V _F	11.2	--	12.8	V	--
Forward current	I _F	--	40	--	mA	--
Luminance(With LCD)	L _v	--	300	--	cd/m ²	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

- (1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	Functional	Notes
1	LEDA	Power supply for backlight anode input terminal.	
2	LEDA	Power supply for backlight anode input terminal.	
3	LEDK	Power supply for backlight cathode input terminal.	
4	LEDK	Power supply for backlight cathode input terminal.	
5	GND	Power Ground	
6	RESET	Reset signal input terminal. Active at 'L'.	
7	CS	Chip select signal input pin	
8	SCL	Serial interface clock	
9	SDA	Input/Output signal pin	
10~33	DB0-DB24	RGB interface data bus.	
34	HSYNC	Horizontal (Line) synchronizing input signal for RGB interface operation.	
35	VSYNC	Vertical (Frame) synchronizing input signal for RGB interface operation.	
36	PCLK	Dot clock signal for RGB interface operation.	
37	DE	Data enable signal for RGB interface operation.	
38	VCI	Power supply: 2.6V ~ 3.3V	
39	IOVCC	I/O Voltage: 1.65V ~ 3.3V	
40	GND	Power Ground	

6. Timing Characteristics

POWER ON/OFF SEQUENCE

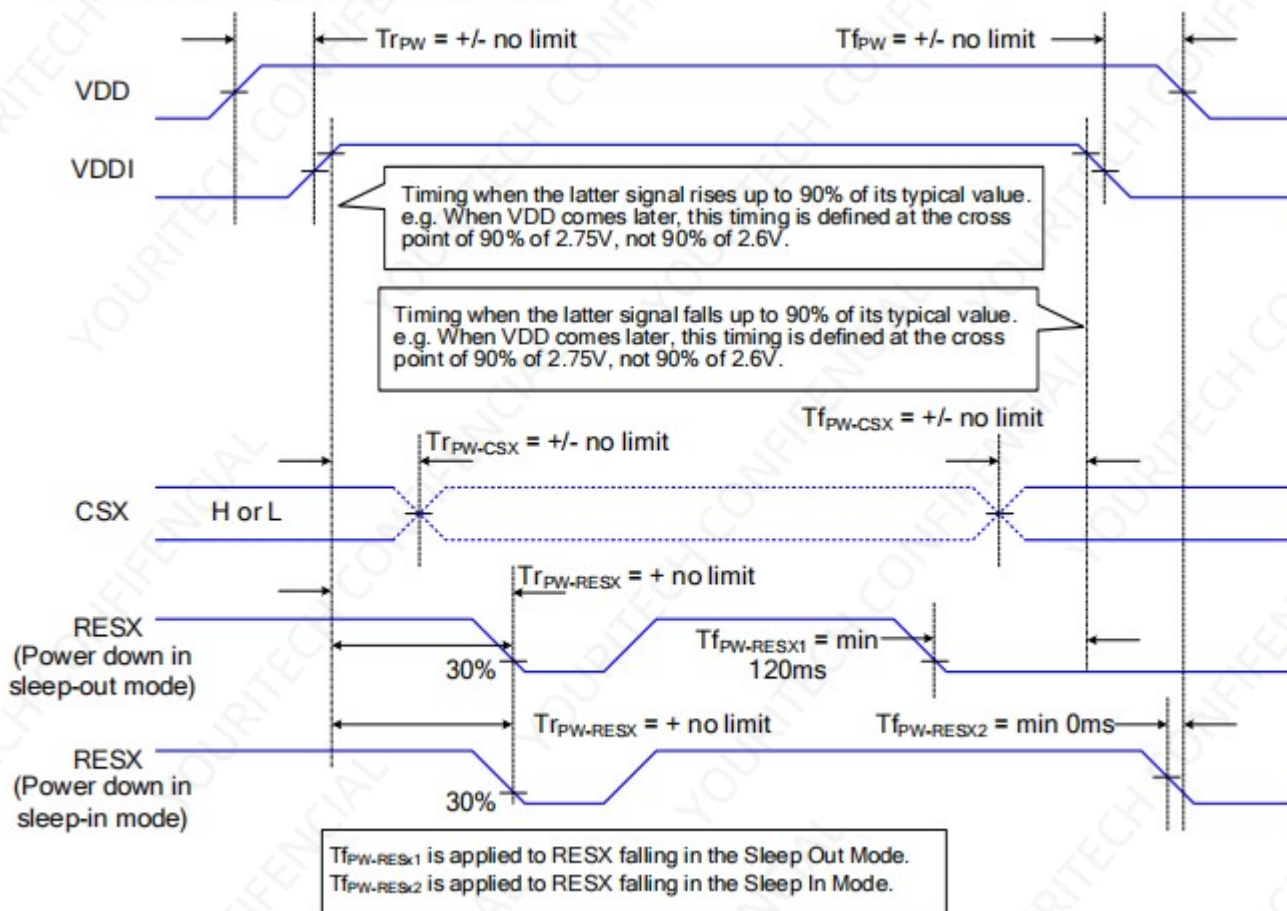
VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released.

CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

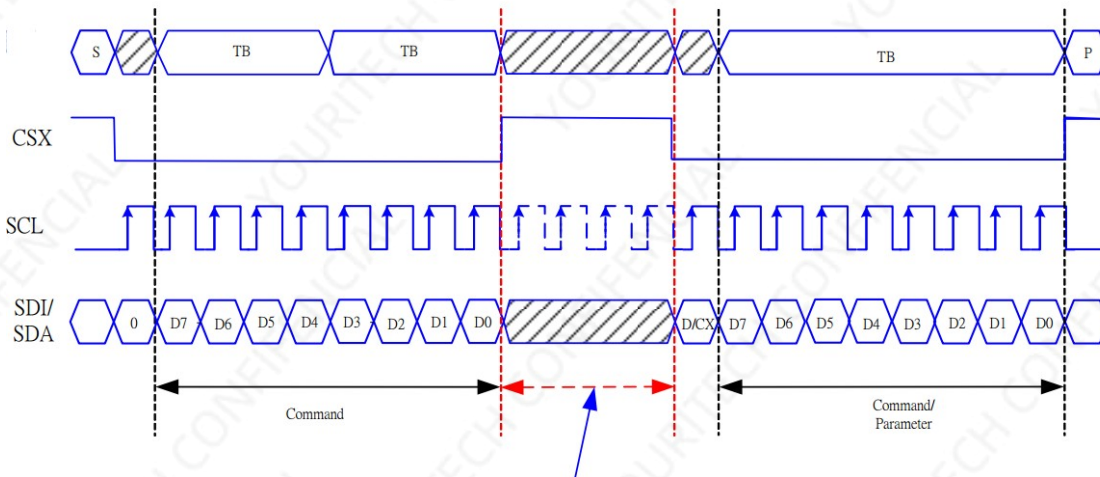
Notes:

1. There will be no damage to the ST7701S if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

The power on/off sequence is illustrated below

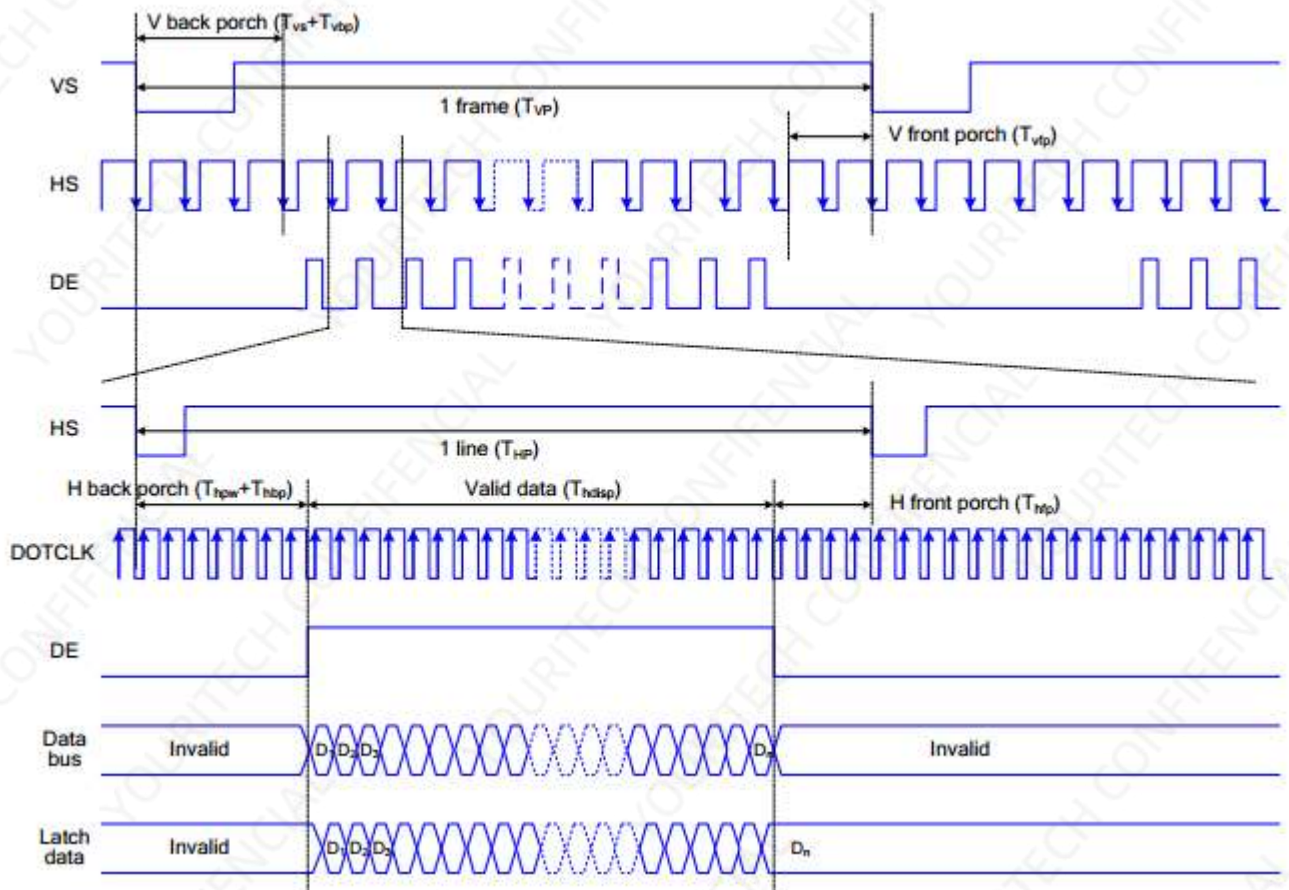


SPI interface pause



The CSX can be in high level between the data and the next command.
 The SDI(SDA) and SCL are invalid if the CSX is in high level.

The timing chart of RGB interface DE mode is shown as follows.



Reset Description:

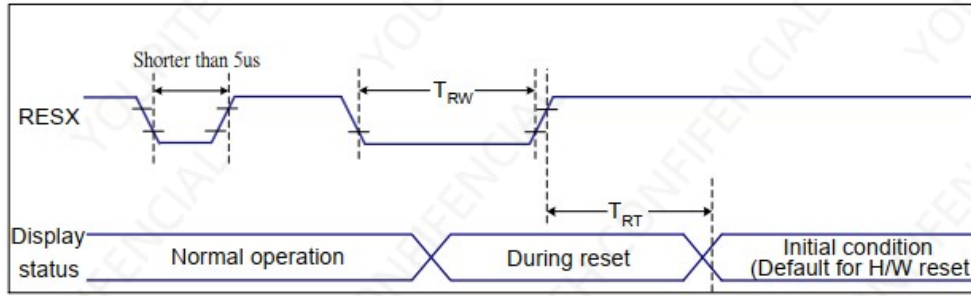


Figure 9 Reset Timing

VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25 °C

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5) 120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

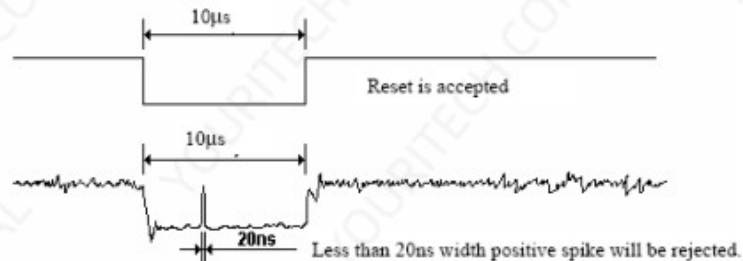
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T (%)	Θ=0 Normal viewing angle	—	4.14	—	%	Measuring with Polarizer , Reference Only
Transmittance (without Polarizer)		T (%)		—	13.13	—	%	
Contrast		CR		720	900	—	—	(1)(2)
Response time	Rising	T _R		—	16	21	msec	(1)(3)
	Falling	T _F		—	19	24		
Color gamut	(%)			—	70	—	%	C-light
Color chromaticity (CIE1931)	White	W _x		-0.02	0.310	+0.02	—	(1)(4) CF glass
		W _y			0.336		—	
	Red	R _x			0.647		—	
		R _y			0.317		—	
	Green	G _x	0.275		—			
		G _y	0.582		—			
	Blue	B _x	0.140		—			
		B _y	0.088		—			
Viewing angle	Hor.	Θ _L	CR>10	—	80	—	(1)(4) Measuring with Polarizer , Reference Only	
		Θ _R		—	80	—		
	Ver.	Θ _U		—	80	—		
		Θ _D		—	80	—		
Optima View Direction		Free						(5)

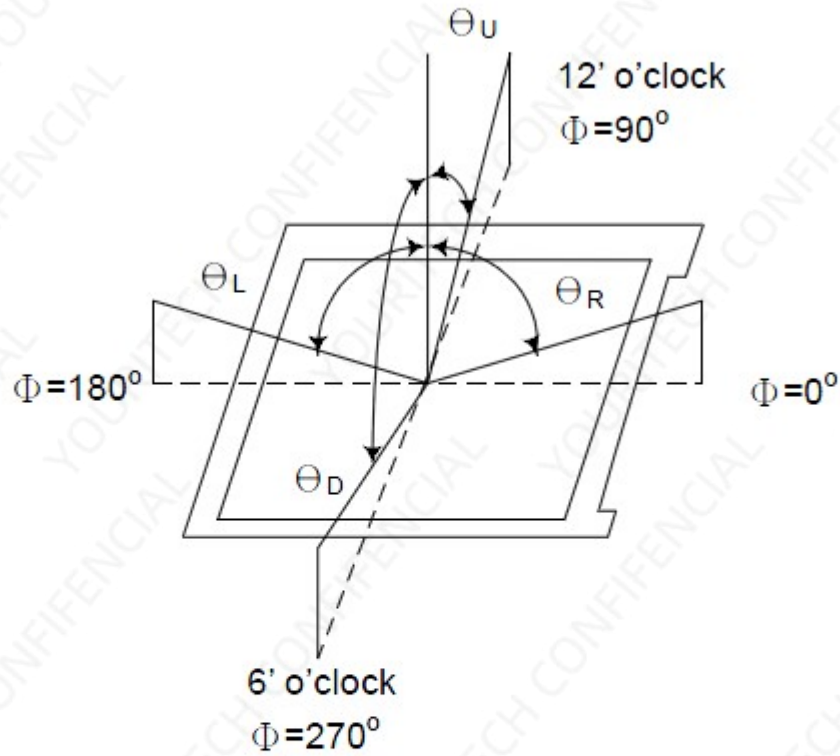
Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : $25\pm 2^\circ\text{C}$
- 15min. warm-up time.

Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

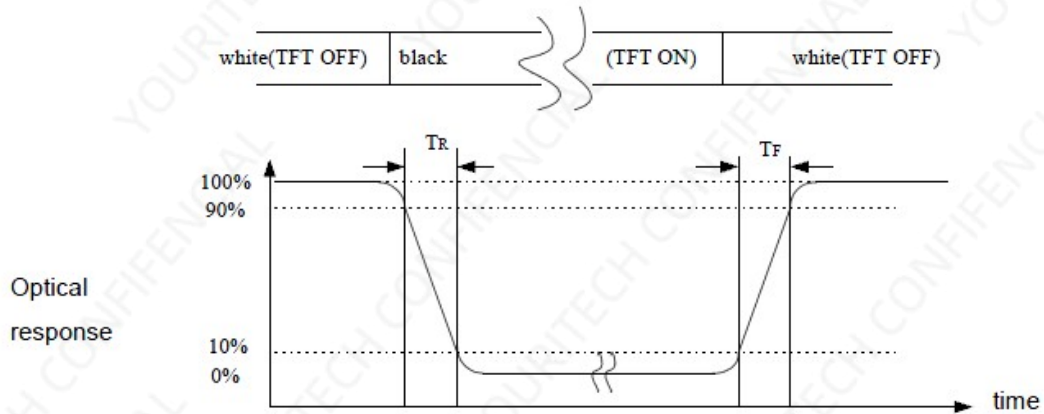
Note (1) Definition of Viewing Angle:



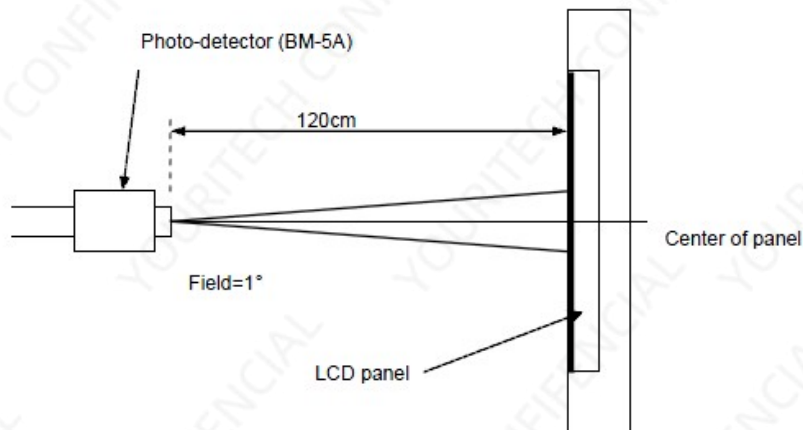
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

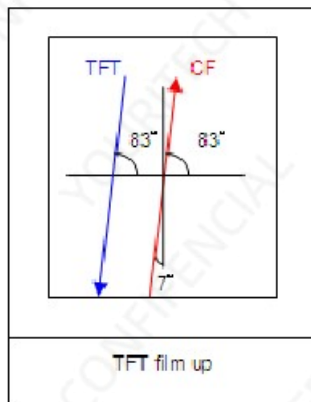
Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup

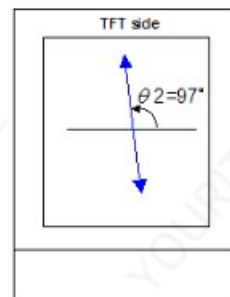
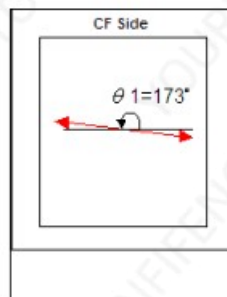


Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.)



CF side polarizing absorption angle $\theta_1=173^\circ$ (Protective film on top, glue layer face down)

TFT side polarizing absorption angle $\theta_2=97^\circ$ (Protective film on top, glue layer face down)



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test is OK. Missing Segment, short, unclear segment non-display, display abnormally and liquid crystal leakage un-allowed. 2. No low temperature bubbles, end seal loose and fall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Temp. Operating	+70°C / 96H	
4	Low Temp. Operating	-20°C / 96H	
5	High Temperature / Humidity storage	50°C x 90%RH / 96H	
6	Thermal and cold shock	Static state, -20°C (30min) ~60°C (30min), 50 cycles	

9. Packing Method----TBD

- END -