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MODEL NO : ET040WV04-TT

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2023-01-03

□Preliminary Specification

■Final Product Specification

Customer :

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 480xRGBx800.
As to basic specification of the driver IC, refer to the IC (ILI9806E) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

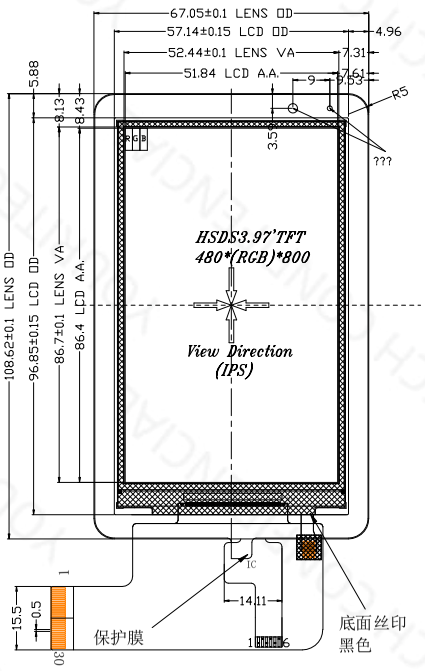
Structure: TFT PANNEL+IC +FPC+B+CTP;
IPS Type LCD
480dot-segment and 800 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
2 Lane MIPI interface;

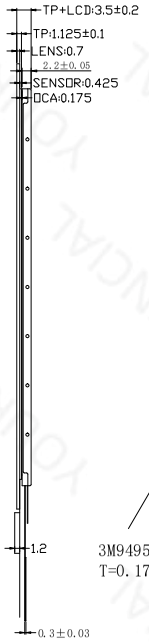
1.3 Applications:

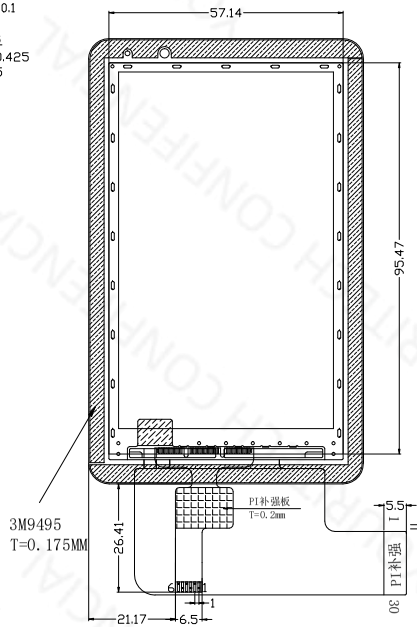
2. LCM General specification

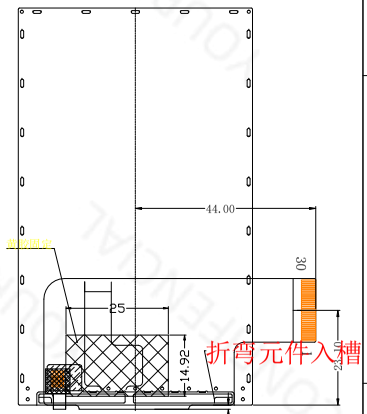
ITEM	Sandard value	Unit
LCD Type	Normally black	--
Drive element	TFT active matrix	--
Number of pixels	480*3RGB(H)X800(V)	Dots
Pixel arrangement	RGB stripe	--
Pixel Pitch (W*H)	0.108(W) × 0.108(H)	mm
Active area	51.84(W) × 86.4(H)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	ILI9806E	--
TFT interface	MIPI Interface	--
LCM Size(W*H*T)	57.14(W) ×96.85(H) ×3.5 (D)	mm
LCM+CTP Size(W*H*T)	57.14(W) ×96.85(H) ×3.5 (D)	mm
Approx. Weight	TBD	g
Touch structure	G+F+F	--
Touch Driver IC	FT5436	--
Touch Interface	I2C	--

1	GND
2	D0-
3	D0+
4	GND
5	D1-
6	D1+
7	GND
8	CLK-
9	CLK+
10	GND
11	/RST
12	TE
13	GND
14	VCI
15	VCI
16	GND
17	IO VCC
18	IO VCC
19	GND
20	CTP_VDD
21	CTP_SDA
22	CTP_SCL
23	CTP_INT
24	CTP_RST
25	GND
26	LED+
27	LED+
28	LED-
29	LED-
30	GND









FPC弯折示意图
模组展开出货
总成折弯出货

NOTES:
1. DISPLAY TYPE: 3.97", 480*800 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION:ALL view direction
4. DRIVER IC:ILI9806E
5. LCM (White 9 AVG 1/9) :
   Brightness: 300cd/㎡
   Uniformity:80%(MIN)
6. BACK LIGHT: 8 chip white LEDs If=40mA,Vf=11.6V~12.8V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS

Note :
1. G+F+F
   COVER Glass :Asahi Dragon Trail 0.7mm
   ITO FILM:0.425mm
   FPC:(PINCH=0.5mm)
   Thickness: 1.125±0.1mm
   Drive IC:FT5436

2. Operating Voltage: 2.8V-3.3 V
3. Transmittance: ≥86%
4. Hardness: 6H
5. Operating TEMP: -20℃~+70℃, ≤90%RH
6. Storage TEMP: -30℃~+80℃, ≤90%RH
7. General Tolerance:±0.2mm

TP PIN DESCRIPTION

PIN	定义
1	GND
2	VCC
3	SDA(1.8)
4	SCL(1.8)
5	INT
6	RESET

TITLE:	深圳市优瑞泰克科技有限公司				
PART NO.:	ET040WV04-TT			MODULE NO.:	00
DRAWN BY:	MR.Y	DATE:		PROJECTION:	
CHECKED BY:		DATE:		SCALE:N.T.S	UNIT: mm
APPROVED BY:		DATE:		SHEET: 1 OF 1	

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
TP Operating Temperature & Humidity(20% ~ 90%RH)	T_{OPR}	-20	+70	°C
TP SStorage Temperature & Humidity(20% ~ 90%RH)	T_{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.5	2.8	3.6	V
Current Consumption	I_{DD}	--	TBD	--	mA
	$I_{DD-SLEEP}$	--	TBD	--	uA

4.2 Back-Light Unit Characeristics

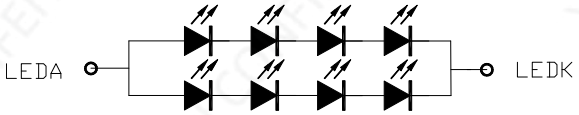
The back-light system is an edge-lighting type with 8 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	11.6	--	12.8	V	--
Forward current	I_F	--	40	--	mA	--
Luminance(With LCD+CTP)	Lv	--	300	--	cd/m^2	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



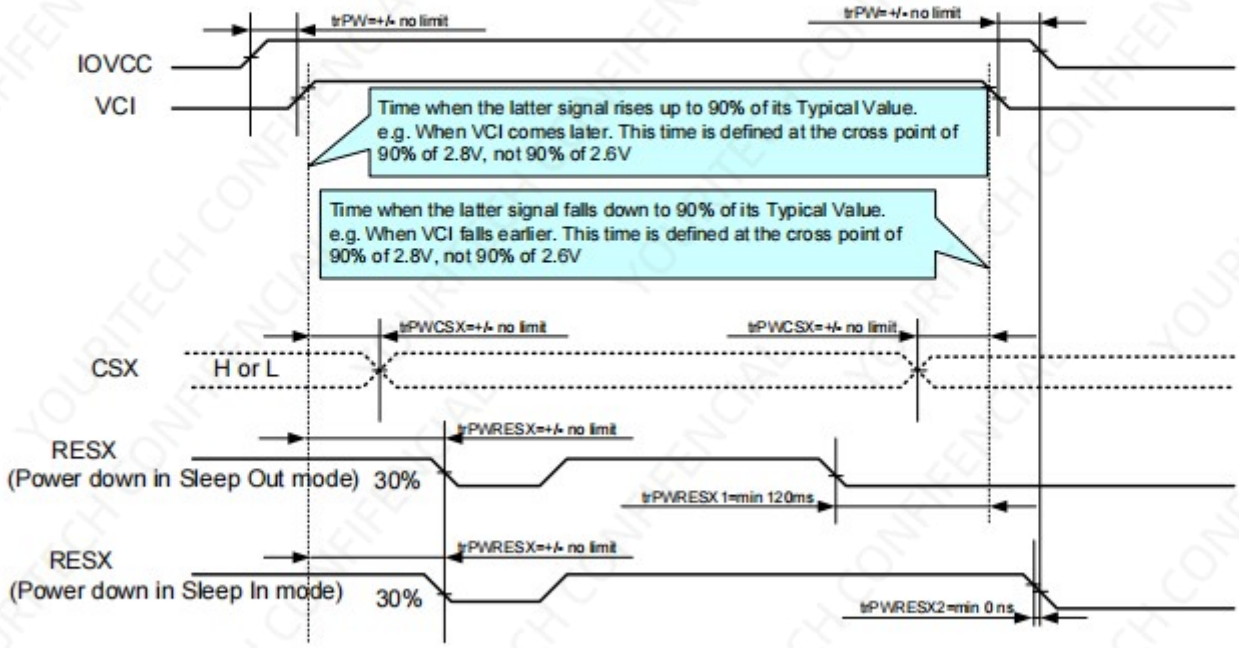
5. Module Function Description

Pin No.	Symbol	Description
1	GND	Ground.
2	DO-	MIPI DSI differential data pair
3	DO+	MIPI DSI differential data pair
4	GND	Ground.
5	D1-	MIPI DSI differential data pair
6	D1+	MIPI DSI differential data pair
7	GND	Ground.
8	CLK-	MIPI DSI differential clock pair
9	CLK+	MIPI DSI differential clock pair
10	GND	Ground.
11	RESET	Reset signal.
12	TE	Tearing effect signal is used to synchronize MCU to frame memory
13	GND	Ground.
14	VCC(2.8V)	Analog supply voltage range for VCI to GND= 2.5V ~ 3.6V
15	VCC(2.8V)	Analog supply voltage range for VCI to GND= 2.5V ~ 3.6V
16	GND	Ground.
17	IOVCC(1.8V)	I/O supply voltage range for IOVCC to DGND = 1.65V ~ 3.6V
18	IOVCC(1.8V)	I/O supply voltage range for IOVCC to DGND = 1.65V ~ 3.6V
19	GND	Ground.
20	CTP_VDD	Touch panel I/O PWR supply
21	CTP_SDA	Touch panel I2C data
22	CTP_SCL	Touch panel I2C clock
23	CTP_INT	Touch panel interrupt output
24	CTP_RST	Touch panel reset
25	GND	Ground.
26	LEDA	POWER SUPPLY+ FOR BACKLIGHT ANODE.
27	LEDA	POWER SUPPLY+ FOR BACKLIGHT ANODE.
28	LEDK	POWER SUPPLY- FOR BACKLIGHT cathode.
29	LEDK	POWER SUPPLY- FOR BACKLIGHT cathode.
30	GND	Ground.

6.Timing Characteristics

Case 1 –RESX line is held High or Unstable by Host at Power ON

If the RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode

trPWRESX2 is applied to RESX falling in the Sleep In Mode

High Speed Mode – Clock Channel Timing

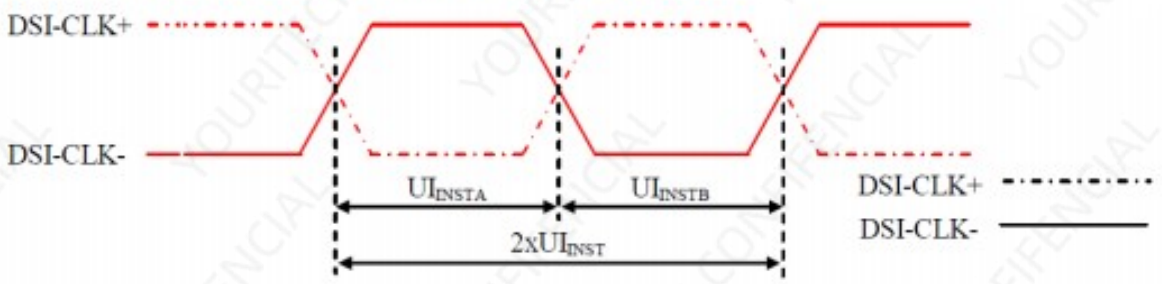


Figure 114 DSI Clock Channel Timing

Table 45 DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
DSI-CLK+/-	UI_{INSTA},UI_{INSTB}	UI instantaneous Half	2	12.5	ns

Note: $UI = UI_{INSTA} = UI_{INSTB}$

High Speed Mode – Data Clock Channel Timing

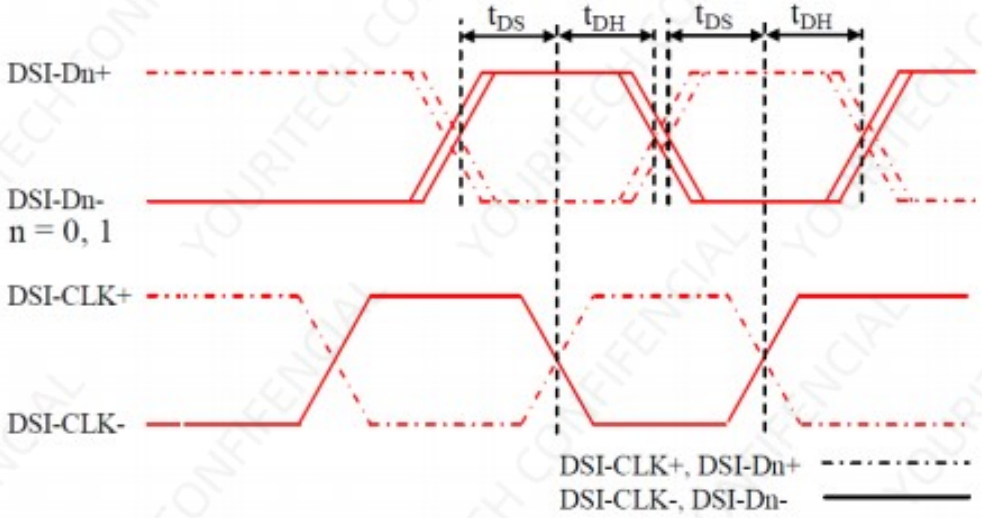


Figure 115 DSI Data to Clock Channel Timings

Table 46 DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DSI-Dn+/- , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MPU to the Display Module (ILI9806E) sequence below.

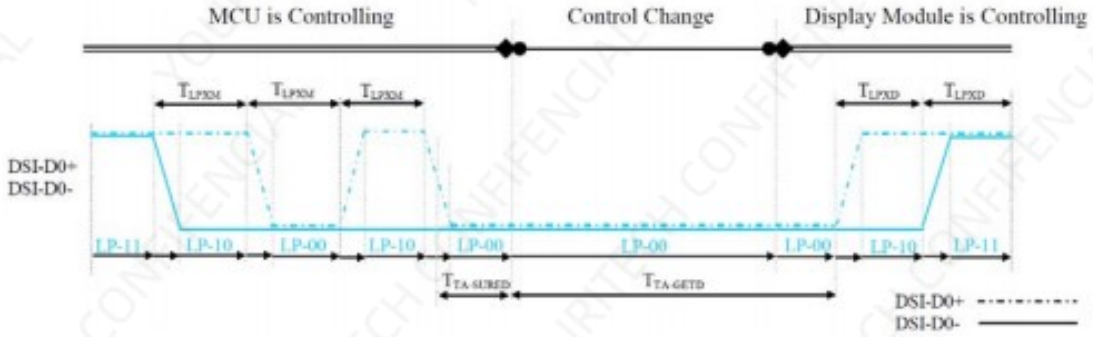


Figure 117 BTA from the MPU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module (ILI9806E) to the MPU sequence below.

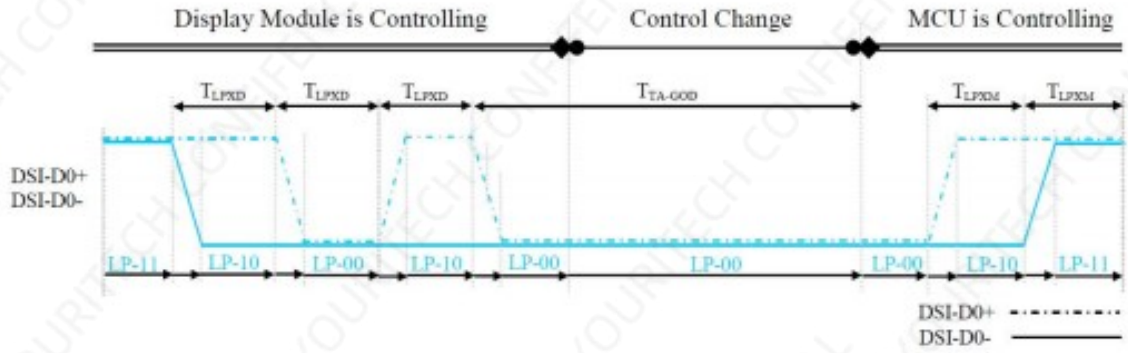


Figure 118 BTA from the Display Module to the MPU

Table 48 Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module (ILI9806E)	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9806E) → MPU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module (ILI9806E) starts driving	T_{LPXD}	$2\times T_{LPXD}$	ns

Table 49 Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9806E)	$5\times T_{LPXD}$	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MPU	$4\times T_{LPXD}$	ns

Data Lanes from Low Power Mode to High Speed Mode

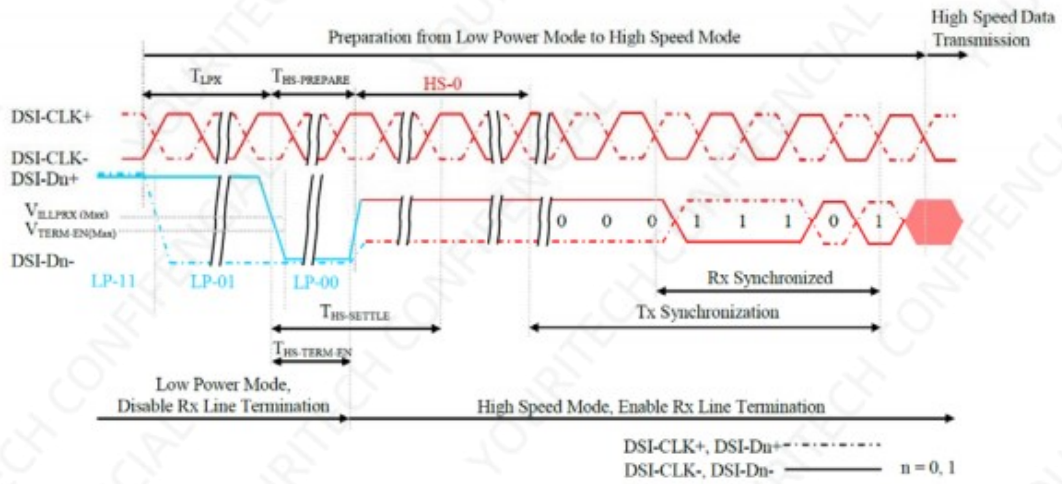
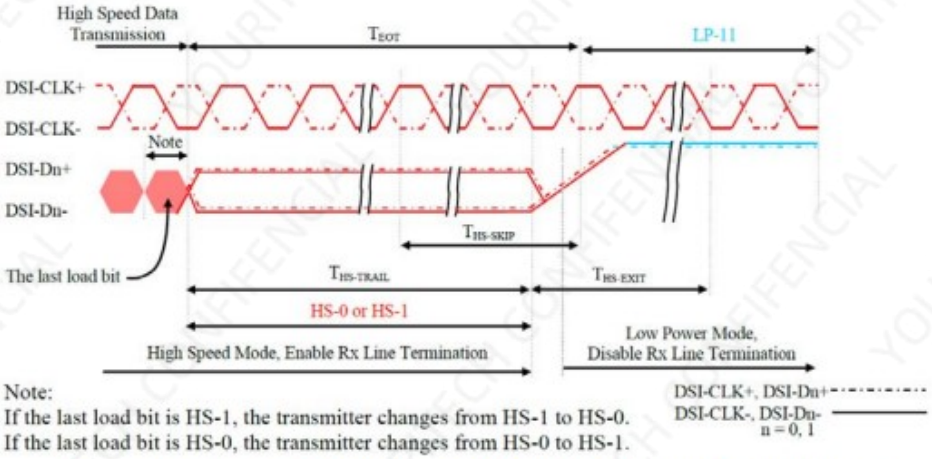


Figure 119 Data Lanes – Low Power Mode to High Speed Mode Timings

Table 50 Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Figure 120 Data Lanes – High Speed Mode to Low Power Mode Timings

Table 51 Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9806E) to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

DSI Clock Burst – High Speed Mode to/from Low Power Mode

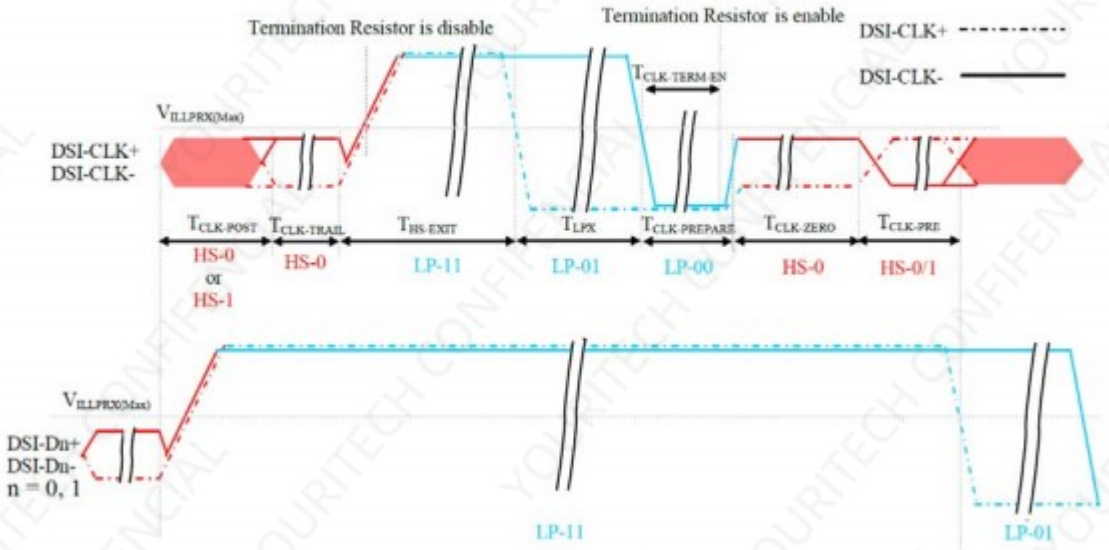


Figure 121 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Table 52 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

Reset Timing

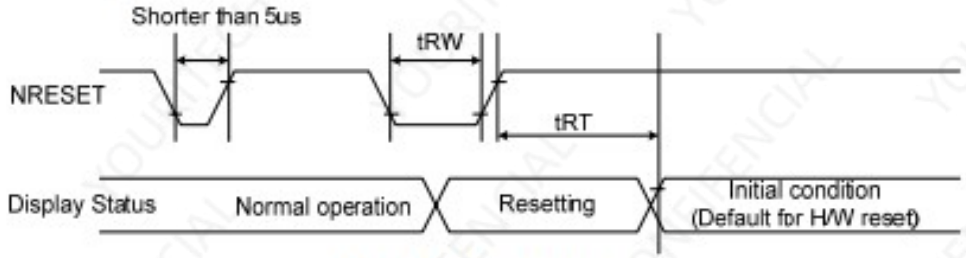


Figure 102 Reset Timing

Table 41 Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5(note 1,5)	ms
				120 (note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 43.

Table 42 Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

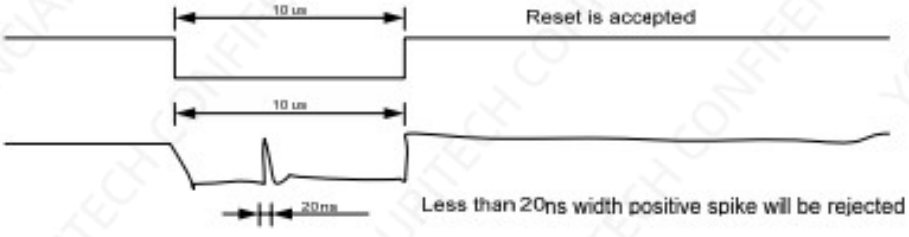


Figure 103 Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

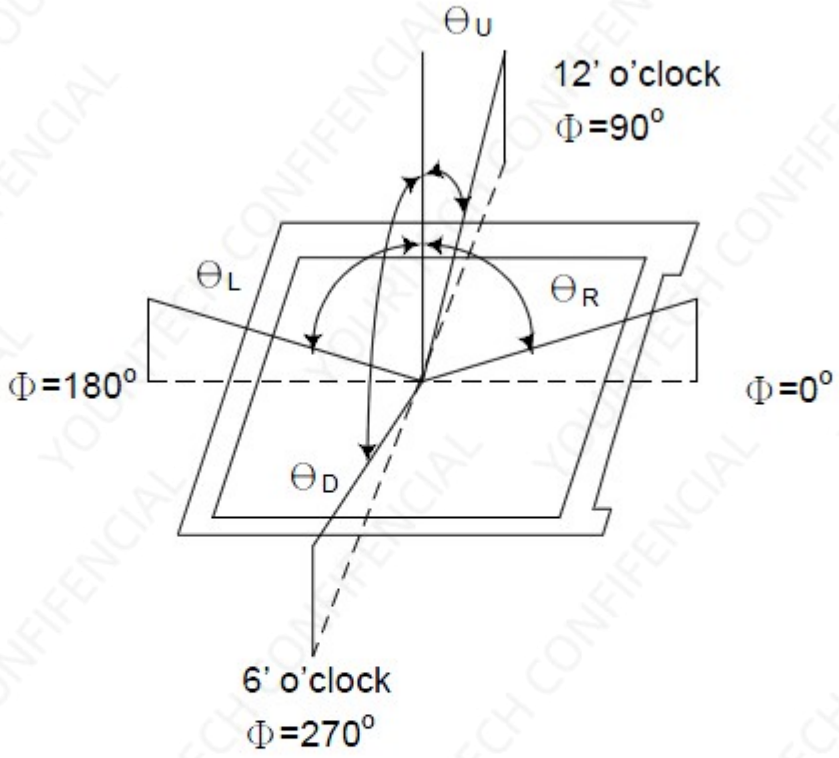
Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T (%)	Θ=0 Normal viewing angle	–	4.14	–	%	Measuring with Polarizer，Reference Only
Transmittance (without Polarizer)		T (%)		–	13.13	–	%	
Contrast		CR		720	900	–	–	(1)(2)
Response time	Rising	T_R		–	16	21	msec	(1)(3)
	Falling	T_F		–	19	24		
Color gamut	(%)			–	70	–	%	C-light
Color chromaticity (CIE1931)	White	W_x		-0.02	0.310	+0.02	–	(1)(4) CF glass
		W_y			0.336			
	Red	R_x			0.647		–	
		R_Y			0.317		–	
	Green	G_x			0.275		–	
		G_Y			0.582			
	Blue	B_x			0.140		–	
		B_Y			0.088			
Viewing angle	Hor.	$Θ_L$	CR>10	–	80	–	–	(1)(4) Measuring with Polarizer，Reference Only
		$Θ_R$		–	80	–		
	Ver.	$Θ_U$		–	80	–		
		$Θ_D$		–	80	–		
Optima View Direction		Free						(5)

Measuring Condition

- Measuring surrounding：dark room
- Ambient temperature：25±2°C
- 15min. warm-up time.

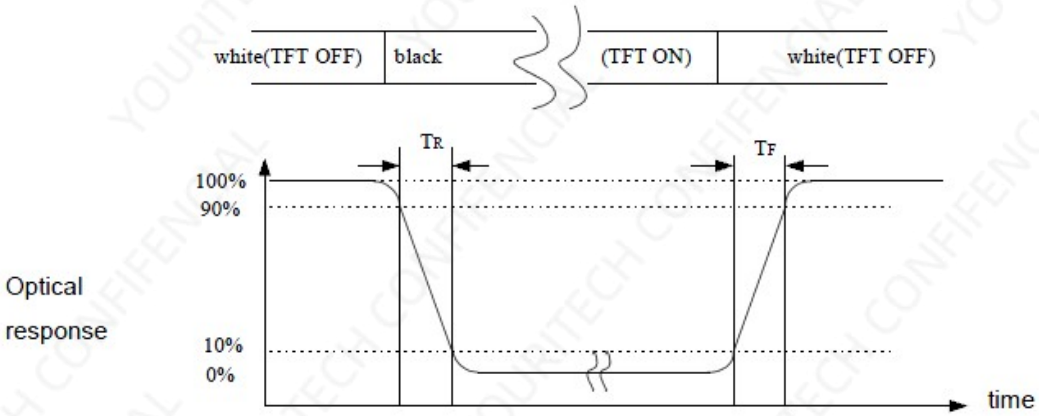
Note (1) Definition of Viewing Angle:



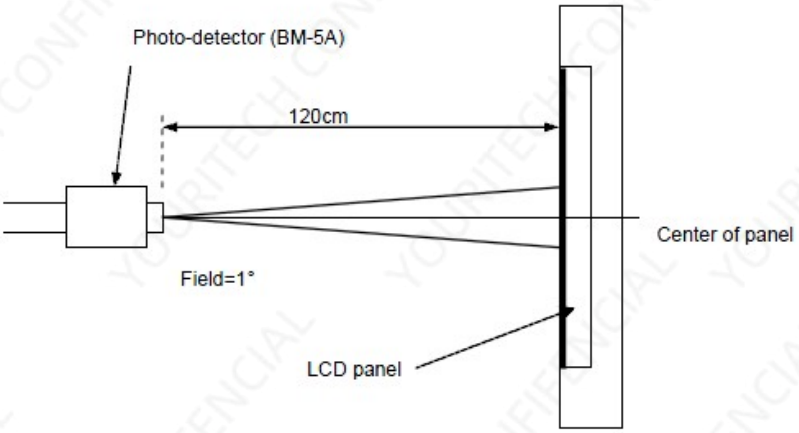
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

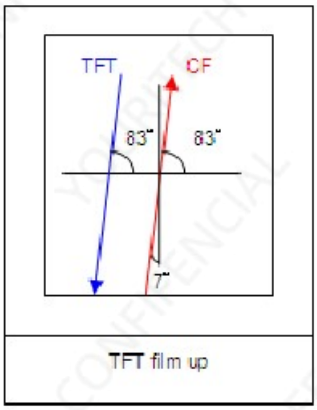
Note (3) Definition of Response Time : Sum of T_R and T_F



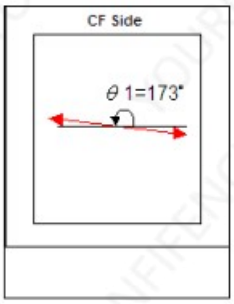
Note (4) Definition of optical measurement setup

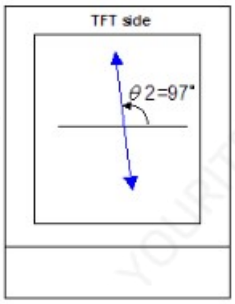


Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.)



CF side polarizing absorption angle θ 1=173° (Protective film on top, glue layer face down)
TFT side polarizing absorption angle θ 2=97° (Protective film on top, glue layer face down)





8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~60℃（30min），50 cycles	

9. Packing Method----TBD

- END -