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Project No. 项目编号	ET041HD01-TT
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	**Standard LCD Module** **TFT：720*RGBx1280Dots** **4.1”TFT LCD+CTP**

客户确认Customer Approval	
项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	

PREPARED BY	CHECKED BY	APPROVED BY

1. Introduction

1.1 Scope of application

This specification applies to the LCD module that is supplied by YOURITECH TECHNOLOGY.
LCD specification: Dots 720xRGBx1280.
As to basic specification of the driver IC, refer to the IC (ST7703I) specification and data book.
All material & processing of the LCD module should be Lead Free.

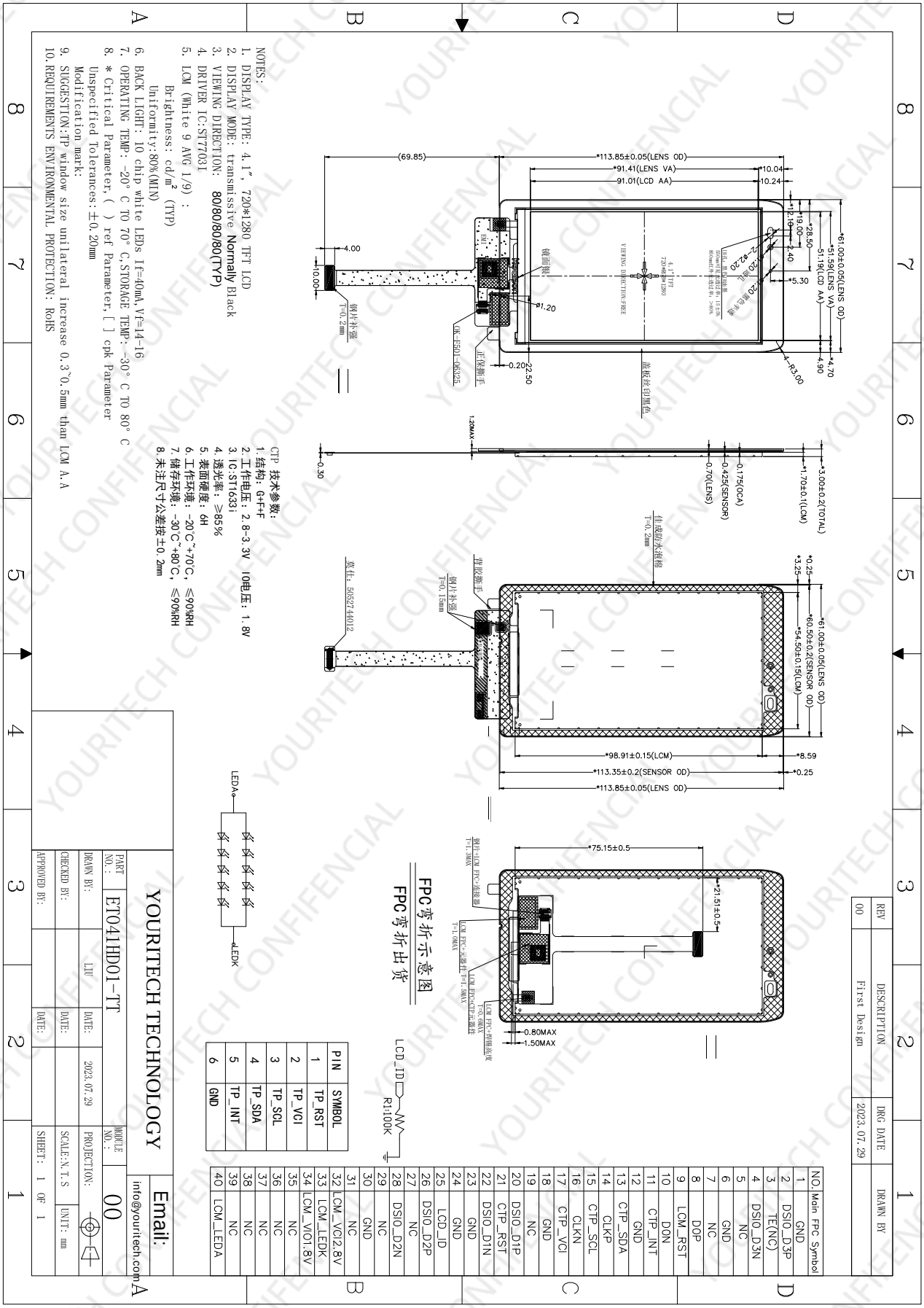
1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL+CTP;
IPS Type LCD
720 dot-segment and 1280 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
4lane MIPI interface

1.3 Applications:

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally black	--
Drive element	TFT active matrix	--
Number of pixels	720*3RGB(H)X1280(V)	Dots
Pixel arrangement	RGB Vertical stripe	--
Pixel Pitch (W*H)	0.08625(H) x0.08625 (V)	mm
Active area	51.19(H) x 91.01(V)	mm
Viewing direction	ALL O'CLOCK	mm
TFT Driver IC	ST7703I	--
TFT interface	4lane MIPI interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	54.50(W)x 98.91(H) x 1.70(T)	mm
LCM+CTP Size(W*H*T)	61.00(W)x 113.85(H) x 3.00(T)	mm
Touch structure	G+F+F	--
Touch Driver IC	ST1633i	--
Touch Interface	I2C	--


NOTES:
1. DISPLAY TYPE: 4.1", 720*1280 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: 80/80/80/80(TYP)
4. DRIVER IC:ST77031
5. LCM (White 9 AVG 1/9) :
Brightness: cd/m² (TYP)
Uniformity:80%(MIN)
6. BACK LIGHT: 10 chip white LEDs If=40mA, Vf=14~16
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter, ( ) ref Parameter, [ ] cpk Parameter
Unspecified Tolerances:±0.20mm
Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS
CTP 技术参数:
1.结构: G+F+F
2.工作电压: 2.8-3.3V IO电压: 1.8V
3.IC:ST1633i
4.透光率: ≥85%
5.表面硬度: 6H
6.工作环境: -20℃~+70℃, ≤90%RH
7.储存环境: -30℃~+80℃, ≤90%RH
8.未注尺寸公差按±0.2mm
FPC弯折示意图
FPC弯折出货
LCD_ID
R1:100K
LEDA
LEDK
PIN SYMBOL
1 TP_RST
2 TP_VCI
3 TP_SCL
4 TP_SDA
5 TP_INT
6 GND
NO. Main FPC Symbol
1 GND
2 DSI0_D3P
3 TE(NC)
4 DSI0_D3N
5 NC
6 GND
7 NC
8 DOP
9 LCM_RST
10 DON
11 CTP_INT
12 GND
13 CTP_SDA
14 CLKP
15 CTP_SCL
16 CLKN
17 CTP_VCI
18 GND
19 NC
20 DSI0_D1P
21 CTP_RST
22 DSI0_D1N
23 GND
24 GND
25 LCD_ID
26 DSI0_D2P
27 NC
28 DSI0_D2N
29 NC
30 GND
31 NC
32 LCM_VCI2.8V
33 LCM_LEDK
34 LCM_VIO1.8V
35 NC
36 NC
37 NC
38 NC
39 NC
40 LCM_LEDA
REV
00
DESCRIPTION
First Design
DRG DATE
2023.07.29
DRAWN BY
YOURITECH TECHNOLOGY
Email:
info@youritech.com
PART NO.: ET041HD01-TT
MODULE NO.: 00
DRAWN BY: LIU
DATE: 2023.07.29
PROJECTION:
CHECKED BY:
DATE:
SCALE:N.T.S
UNIT: mm
APPROVED BY:
DATE:
SHEET: 1 OF 1

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
TP Operating Temperature & Humidity (20% ~ 90%RH)	T_{OPR}	-20	+70	°C
TP SStorage Temperature & Humidity (20% ~ 90%RH)	T_{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.5	2.8	3.3	V

4.2 Back-Light Unit Characeristics

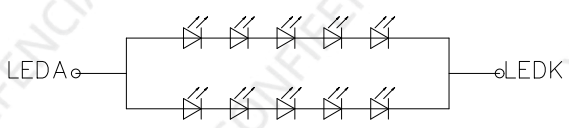
The back-light system is an edge-lighting type with 10 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	14	--	16	V	--
Forward current	I_F	--	40	--	mA	--
Luminance(With LCD+CTP)	Lv	--	TBD	--	cd/m^2	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	LCM Functional	Notes
1	GND	Power Ground	
2	MIPI_D3P	High speed interface data differential signal input/output pins	
3	TE(NC)	No Connection.	
4	MIPI_D3N	High speed interface data differential signal input/output pins	
5	NC	No Connection.	
6	GND	Power Ground	
7	NC	No Connection.	
8	MIPI_D0P	High speed interface data differential signal input/output pins	
9	RESET	The external reset input initializes the chip with a low input.	
10	MIPI_D0N	High speed interface data differential signal input/output pins	
11	CTP_INT	Interrupt signal	
12	GND	Power Ground	
13	CTP_SDA	Touch panel I2C data	
14	MIPI_CKP	High speed interface clock differential signal input/output pins	
15	CTP_SCL	Touch panel I2C clock	
16	MIPI_CKN	High speed interface clock differential signal input/output pins	
17	CTP_VCC	Touch panel Power supply 2.8~3.3V	
18	GND	Power Ground	
19	NC	No Connection.	
20	MIPI_D1P	High speed interface data differential signal input/output pins	
21	CTP_RST	Touch panel reset	
22	MIPI_D1N	High speed interface data differential signal input/output pins	
23	GND	Power Ground	
24	GND	Power Ground	
25	LCD-ID	ID read PIN for ID circuit.	
26	MIPI_D2P	High speed interface data differential signal input/output pins	
27	NC	No Connection.	
28	MIPI_D2N	High speed interface data differential signal input/output pins	
29	NC	No Connection.	
30	GND	Power Ground	
31	NC	No Connection.	
32	VCC 2.8V	power supply for DC/DC circuit(2.5~3.3V)	
33	LEDK	Power supply for backlight cathode input terminal.	
34	IOVCC 1.8V	power supply for the I/O circuit(1.65~2.0V)	
35	NC	No Connection.	
36	NC	No Connection.	
37	NC	No Connection.	
38	NC	No Connection.	
39	NC	No Connection.	
40	LEDA	Power supply for backlight anode input terminal.	

6. Timing Characteristics

Case 1: RESX line is held high or unstable by host at power on

If RESX line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied- otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

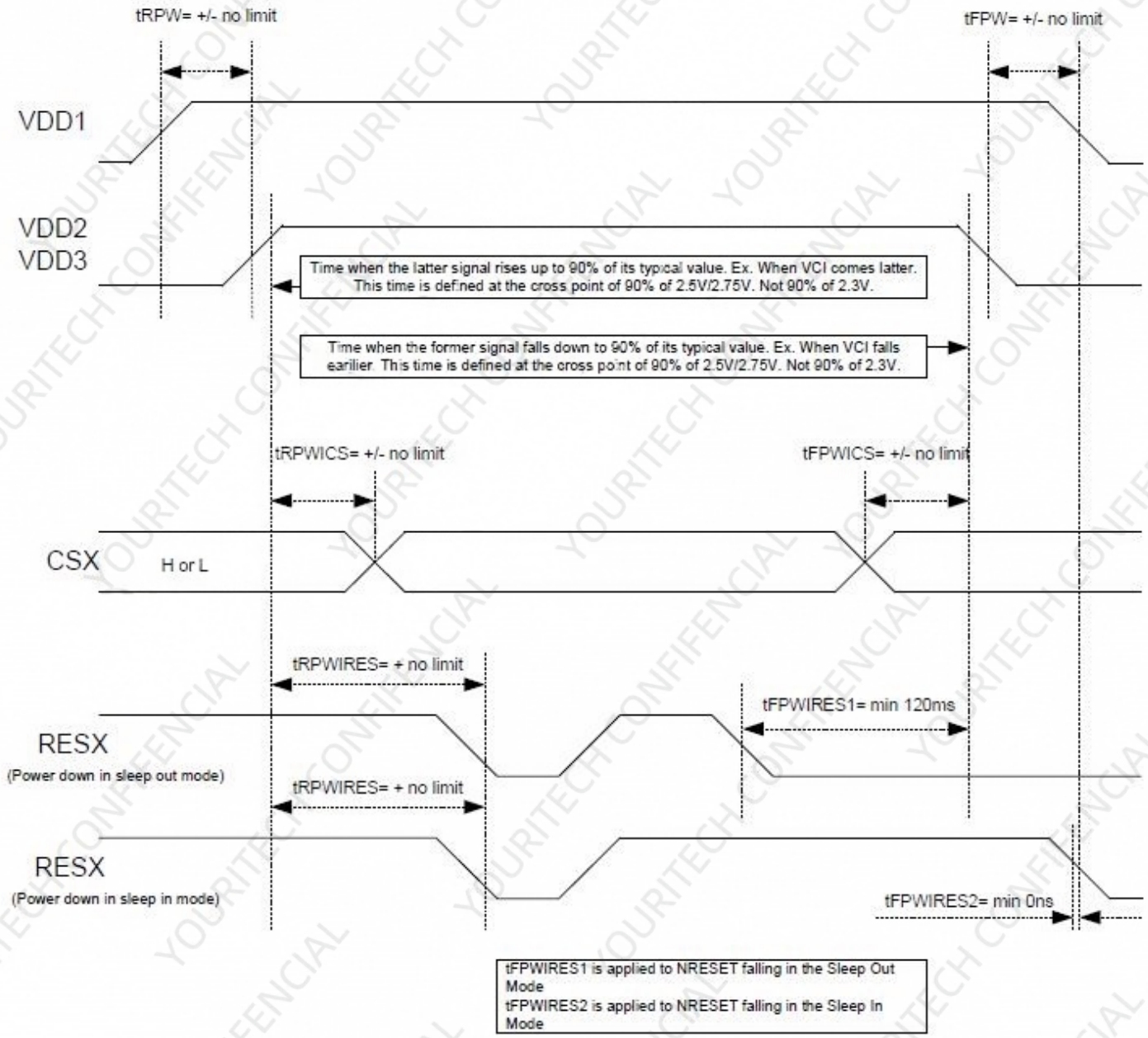


Figure 5.33: Case 1: RESX line is held high or unstable by host at power on

DSI Interface Timing Characteristics:

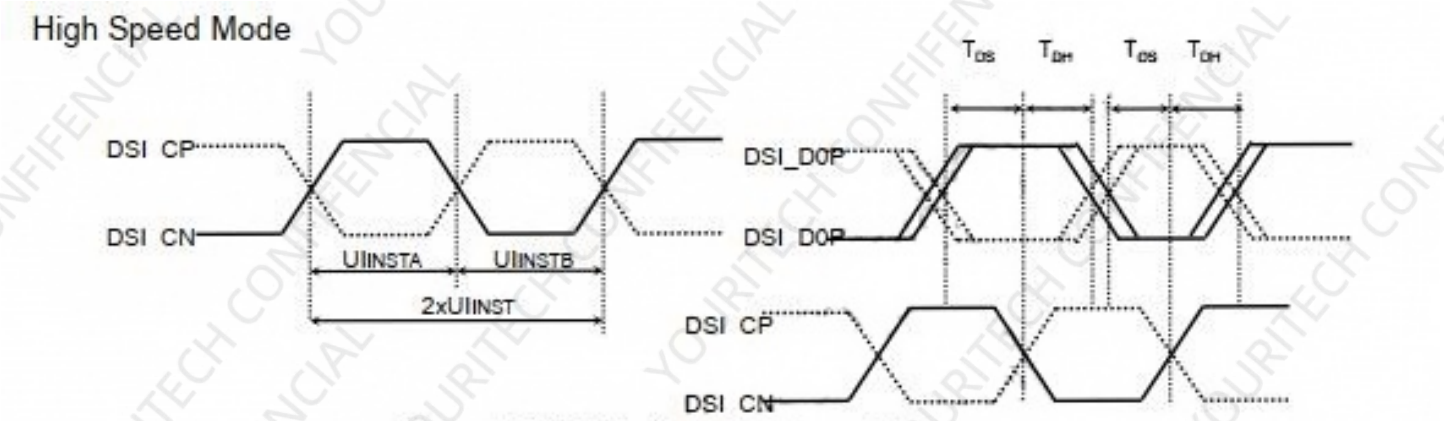


Figure 7.4: DSI clock timing Characteristics

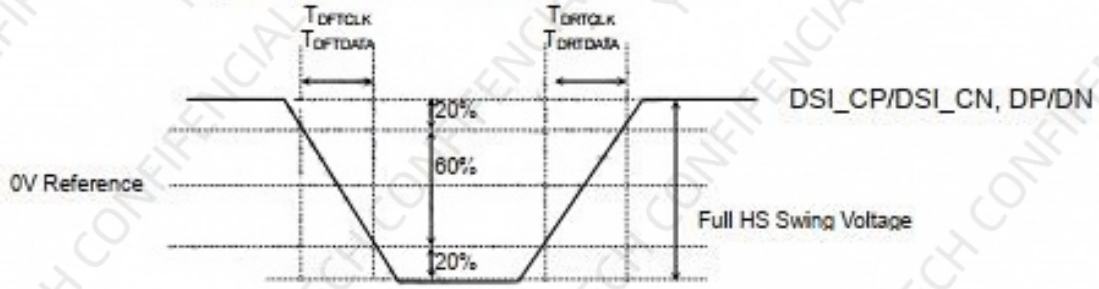


Figure 7.5: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xUINST	TBD	-	25	ns
	UI instantaneous	UINSTA UINSTB	TBD	-	12.5	ns
DP/DN	Data to clock setup time	TDS	0.15xUI	-	-	ps
	Data to clock hold time	TDH	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	TDRTCLK	150	-	0.3UI	ps
	Differential fall time for clock	TDFTCLK	150	-	0.3UI	ps
DP/DN	Differential rise time for data	TDRTDATA	150	-	0.3UI	ps
	Differential fall time for data	TDFTDATA	150	-	0.3UI	ps

Table 7.3: DSI High Speed Mode Characteristics

Low Power Mode

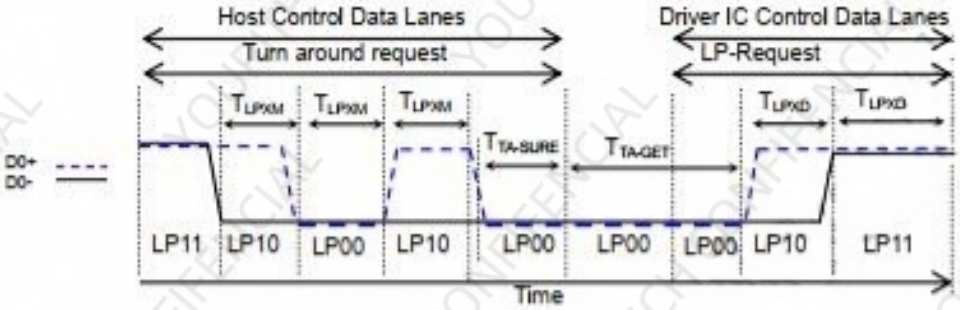


Figure 7.6: BTA from HOST to Display Module Timing

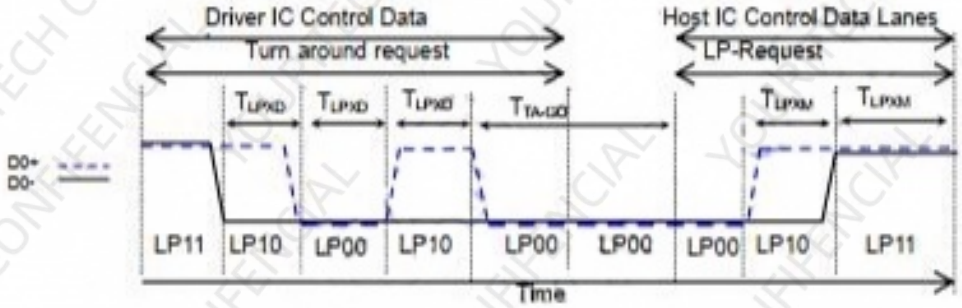


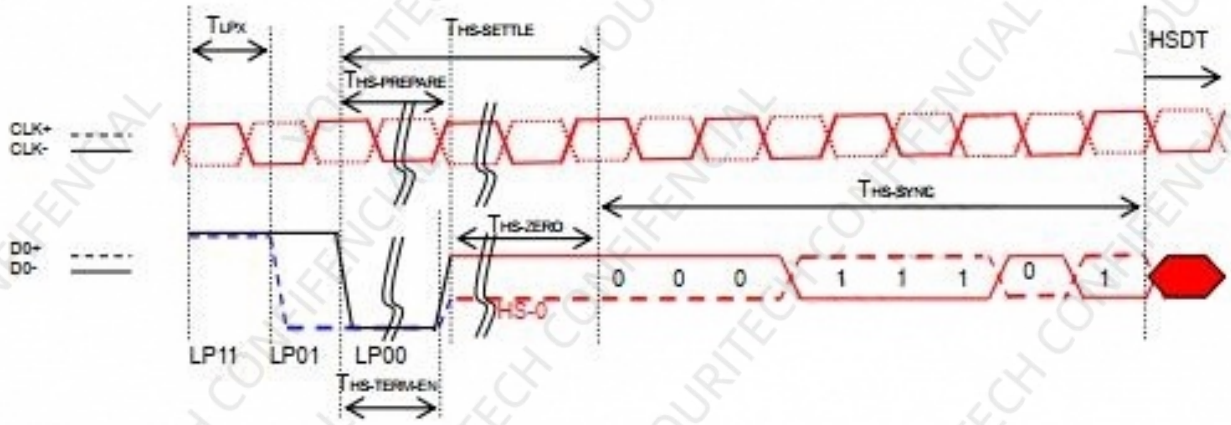
Figure 7.7: BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	2xT_{LPXD}	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

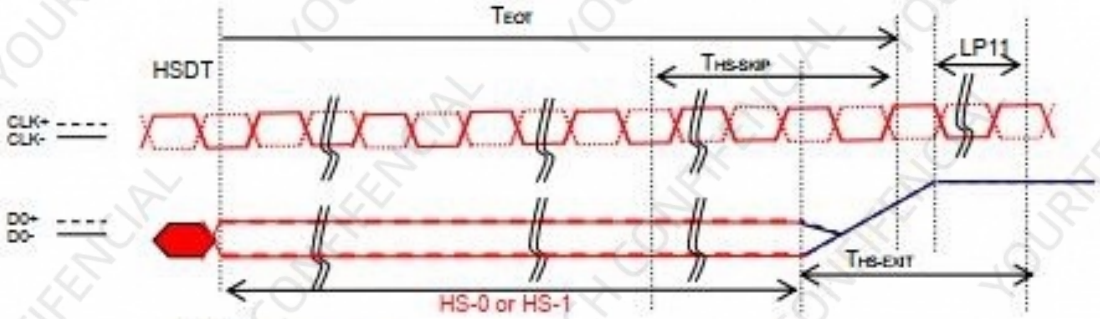
Table 7.4: DSI Low Power Mode Characteristics

DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TA-GO}	4xT_{LPXD}	-	-	ns

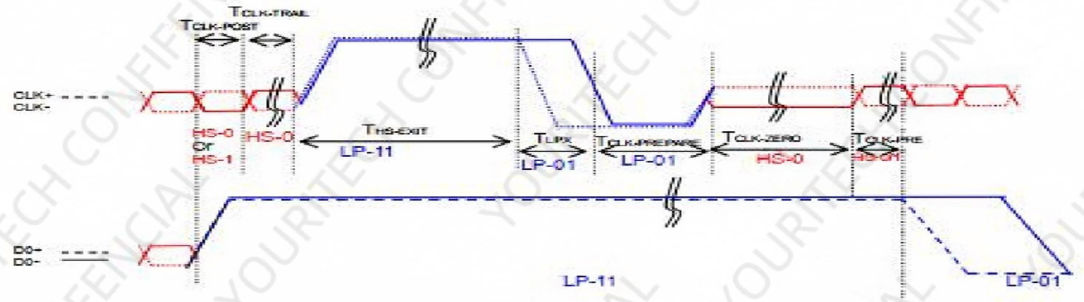
Table 7.5: DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

Table 7.6: DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	TCLK-POST	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	TCLK TRAIL	60	-	-	ns
	Time to drive LP-11 after HS burst	THS-EXIT	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	TCLK-PREPARE	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	TCLK-TERM-EN	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	TCLK-PREPARE + TCLK-ZERO	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	TCLK-PRE	8xUI			

Table 7.7: Clock Lanes High Speed Mode to/from Low Power Mode Timing

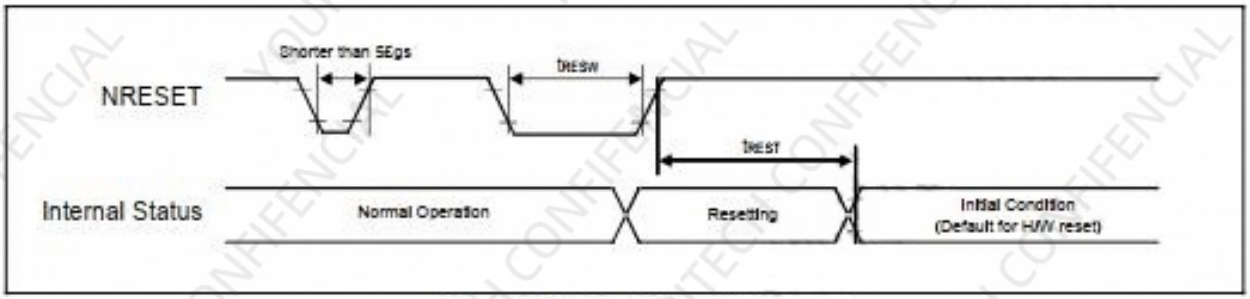


Figure 7.8: Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 7.8: Reset Input Timing

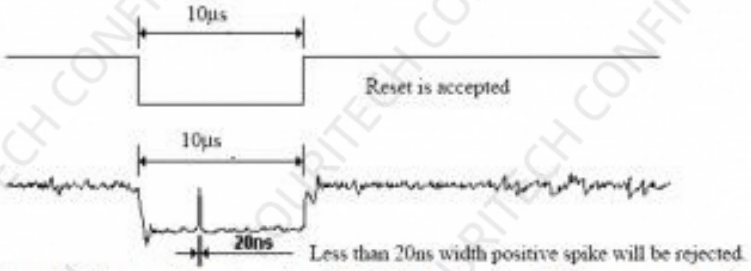
Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 us	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 15ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T (%)	Θ=0 Normal viewing angle	—	3.1	—	%	Measuring with Polarizer，Reference Only
Transmittance (without Polarizer)		T (%)		—	10.53	—	%	
Contrast Ratio		CR		640	800	—	—	(1)(2)
Response Time	Rising	T_R		—	10	15	msec	(1)(3)
	Falling	T_F		—	20	25		
Color Gamut	(%)			—	70	—	%	C-light
Color Chromaticity (CIE1931)	White	W_x		0.283	0.303	0.323	—	(1)(4) CF glass
		W_y		0.303	0.323	0.343		
	Red	R_x					—	
		R_Y						
	Green	G_x					—	
		G_Y						
	Blue	B_x					—	
		B_Y						
Viewing Angle	Hor.	Θ_L	CR>10	—	80	—	—	(1)(4) Measuring with Polarizer，Reference Only
		Θ_R		—	80	—		
	Ver.	Θ_U		—	80	—		
		Θ_D		—	80	—		
Optima View Direction		Free						(5)

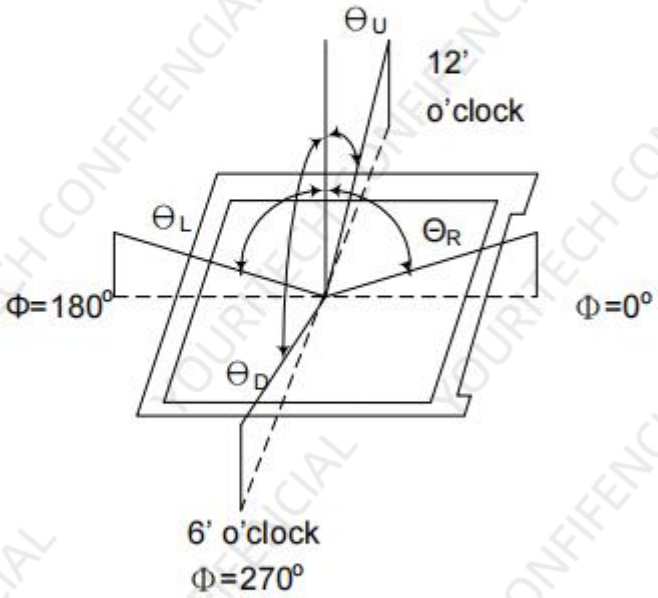
Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : 25±2°C
- 15min. warm-up time.

Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

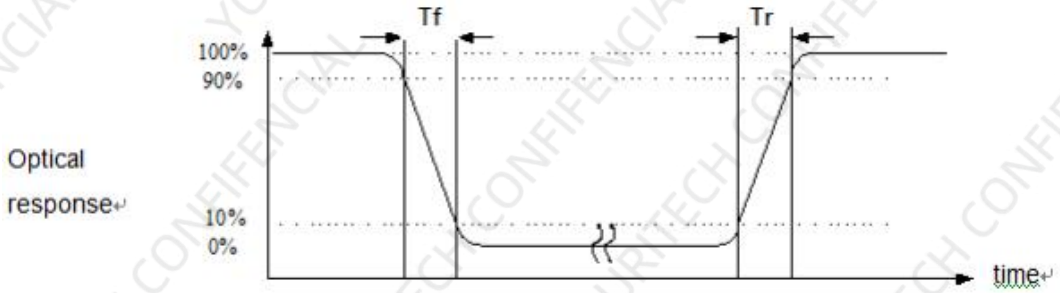
Note (1) Definition of Viewing Angle:



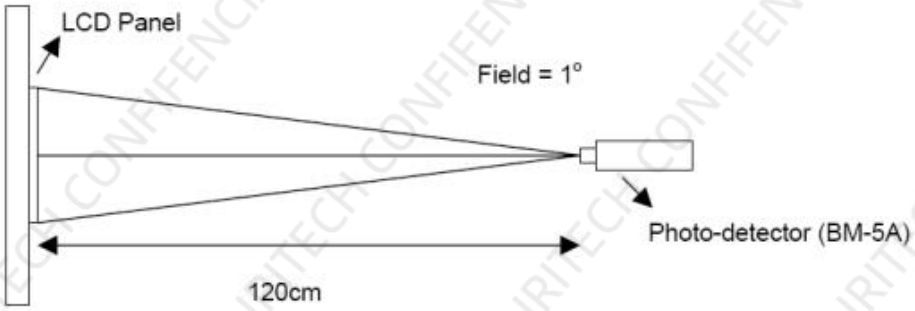
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3) Definition of Response Time: Sum of T_R and T_F



Note (4) Definition of optical measurement setup



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~70℃（30min），10 cycles	

9. Packing Method----TBD