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info@youritech.com

Project No. 项目编号	ET045FW02-T
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	**Standard LCD Module** **TFT：480*RGBx854Dots** **4.5”TFT LCD**

客户确认Customer Approval	
项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	

1. Introduction

1.1 Scope of application

This specification applies to the LCD module that is supplied by YOURITECH TECHNOLOGY

LCD specification: Dots 480xRGBx854.

As to basic specification of the driver IC, refer to the IC (GC9503V) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;

ALL O'CLOCK Type LCD

480dot-segment and 854 dot-common outputs;

16.7M Color can be selected by software;

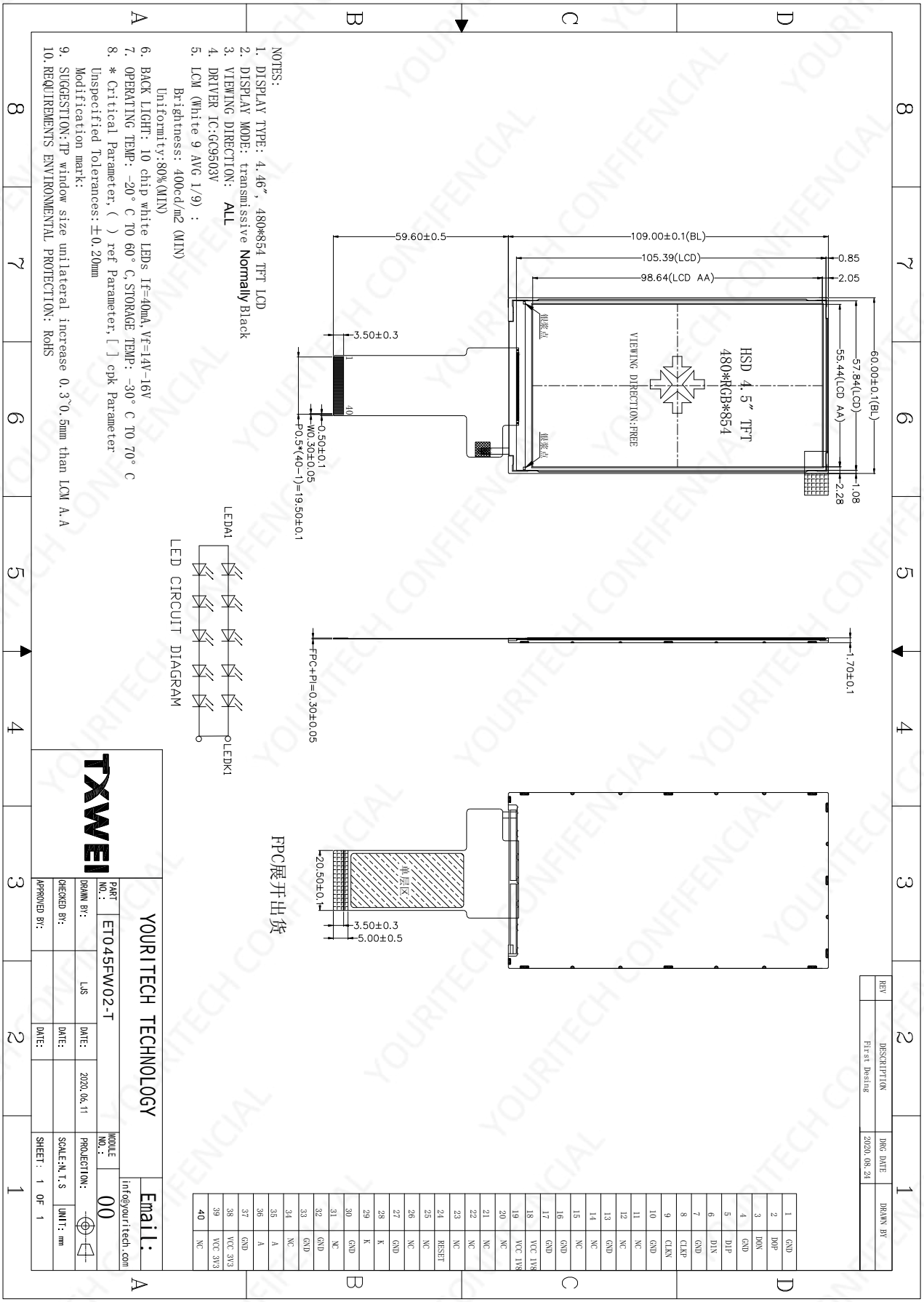
White LED back light;

2Lane MIPI interface

1.3 Applications:

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally black	--
Drive element	TFT active matrix	--
Number of pixels	480*3RGB(H)X854(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.1155 (H) x 0.1155 (V)	mm
Active area	55.44 (H) x 98.637 (V)	mm
Viewing direction	ALL O'CLOCK	-
TFT Driver IC	GC9503V	
TFT interface	2Lane MIPI Interface	-
Module Size(W*H*T)	60.00(W) ×109.00(H) ×1.70(T)	mm
Approx. Weight	TBD	g
Touch structure		
Touch Driver IC		-
Touch Interface		


NOTES:
1. DISPLAY TYPE: 4.46", 480*854 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL
4. DRIVER IC:GC9503V
5. LCM (White 9 AVG 1/9) :
Brightness: 400cd/m2 (MIN)
Uniformity:80%(MIN)
6. BACK LIGHT: 10 chip white LEDs If=40mA, Vf=14V-16V
7. OPERATING TEMP: -20° C TO 60° C,STORAGE TEMP: -30° C TO 70° C
8. * Critical Parameter, ( ) ref Parameter, [ ] cpk Parameter
Unspecified Tolerances:±0.20mm
Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS
HSD 4.5" TFT
480*RGB*854
VIEWING DIRECTION:FREE
LED CIRCUIT DIAGRAM
FPC展开出货
YOURITECH TECHNOLOGY
TXWEI
PART NO.: ET045FW02-T
MODULE NO.: 00
DRAWN BY: LJS
DATE: 2020.06.11
PROJECTION:
CHECKED BY:
APPROVED BY:
SCALE:N.T.S
UNIT: mm
SHEET: 1 OF 1
Email: info@youritech.com
DESCRIPTION: First Desing
DRG DATE: 2020.08.24
DRAWN BY

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+60	°C
LCM Storage Temperature	T_{STG}	-30	+70	°C
Humidity	RH	-	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage for(DC/DC)	VDD	2.5	2.8	3.3	V	
Supply Voltage for(IOVCC)	IOVCC	1.65	1.8	3.3	V	
TFT Gate ON Voltage	VGH	9.0	--	12.5	V	*1,*2
TFT Gate OFF Voltage	VGL	-8	--	-11.5	V	*1,*2
AVDD Voltage	AVDD	6.01	--	7.4	V	

Note:

*1. VGH is TFT Gate operating Voltage.

*2. VGL is TFT Gate operating Voltage.

The storage structure of this model is CST(Storage on Common)

*3. Vcom must be adjusted to optimize display quality _Cross talk, Contrast Ratio and etc.

4.2 Back-Light Unit Characeristics

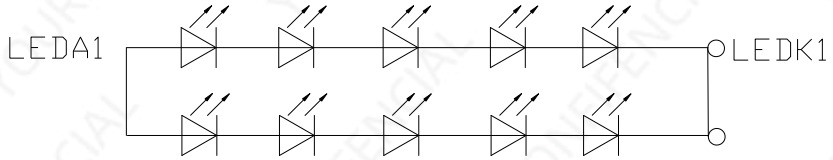
The back-light system is an edge-lighting type with 10 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	14	--	16	V	-
Forward current	I_F	--	40	-	mA	-
Luminance(With LCD)	Lv		400	--	cd/m^2	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	Description
1	GND	Power Ground
2	DSI_ D0_P	MIPI-DSI Data differential signal input pins
3	DSI_ D0_N	MIPI-DSI Data differential signal input pins
4	GND	Power Ground
5	DSI_ D1_P	MIPI-DSI Data differential signal input pins
6	DSI_ D1_N	MIPI-DSI Data differential signal input pins
7	GND	Power Ground
8	DSI_CLKP	MIPI-DSI CLOCK differential signal input pins
9	DSI_CLKN	MIPI-DSI CLOCK differential signal input pins
10	GND	Power Ground
11	NC	NC
12	NC	NC
13	GND	Power Ground
14	NC	NC
15	NC	NC
16~17	GND	Power Ground
18~19	VDD_1V8	I/O Voltage (VDDI to DGND): 1.65~3.3V
20~23	NC	NC
24	RESET	Reset signal input terminal. Active at 'L'.
25~26	NC	NC
27	GND	Power Ground
28~29	LEDK	Power supply for backlight cathode input terminal.
30	GND	Power Ground
31	NC	NC
32~33	GND	Power Ground
34	NC	NC
35~36	LEDA	Power supply for backlight anode input terminal.
37	GND	Power Ground
38~39	VDD_3V3	Power supply 2.5~3.3V
40	NC	NC

6. Timing Characteristics

RGB Interface Characteristics :

High Speed Mode – Clock Channel Timing

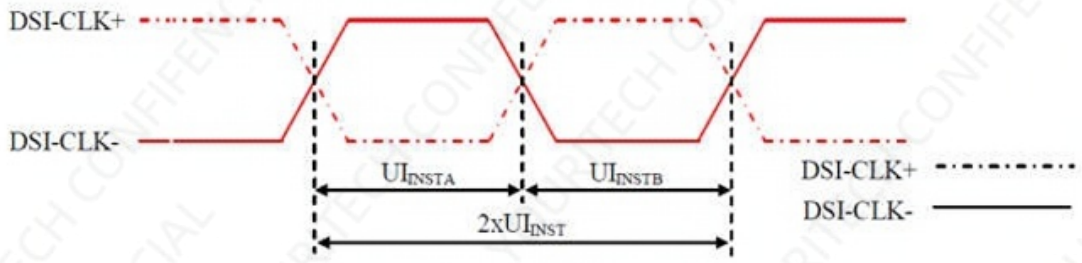


Figure 114 DSI Clock Channel Timing

Table 45 DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
DSI-CLK+/-	UI_{INSTA}, UI_{INSTB}	UI instantaneous Half	2	12.5	ns

Note: $UI = UI_{INSTA} = UI_{INSTB}$

High Speed Mode – Data Clock Channel Timing

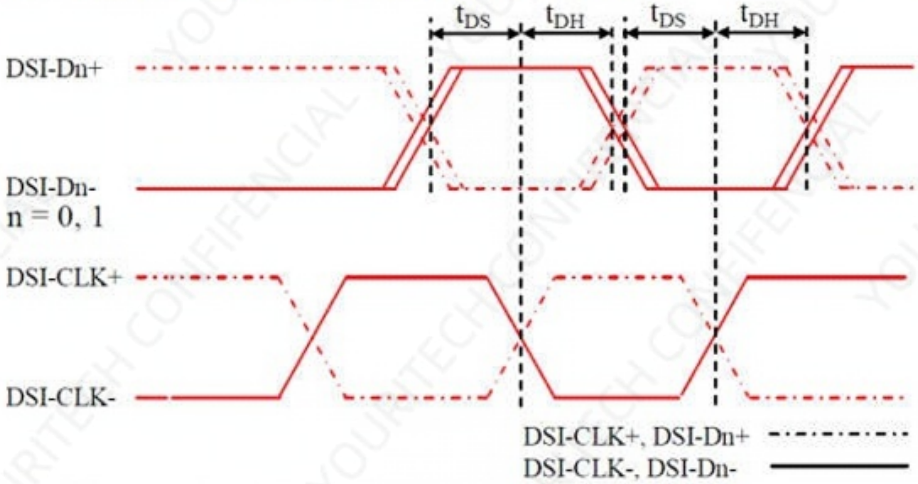


Figure 115 DSI Data to Clock Channel Timings

Table 46 DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DSI-Dn+/- , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

High Speed Mode – Rise and Fall Timings

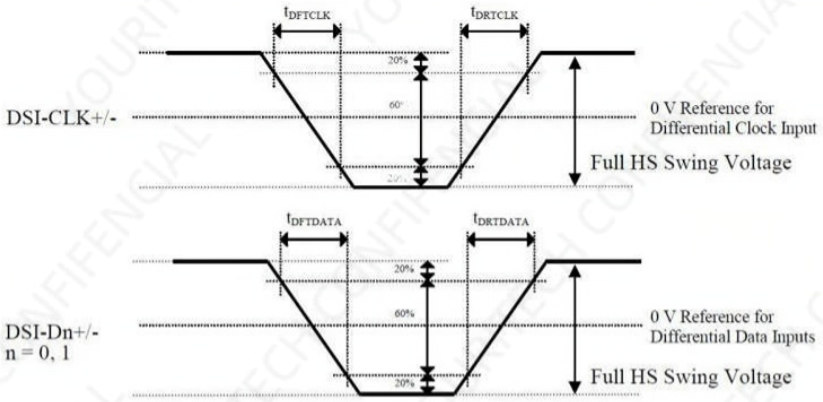


Figure 116 Rise and Fall Timings on Clock and Data Channels

Table 47 Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification			Unit
			Min	Typ	Max	
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-	-	-	150 (Note)	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note)	ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-	-	-	150 (Note)	ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note)	ps

Note:The display module has to meet timing requirements, what are defined for the transmitter (MPU) on MIPI D-Phy standard

Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MPU to the Display Module (GC9503V) sequence below.

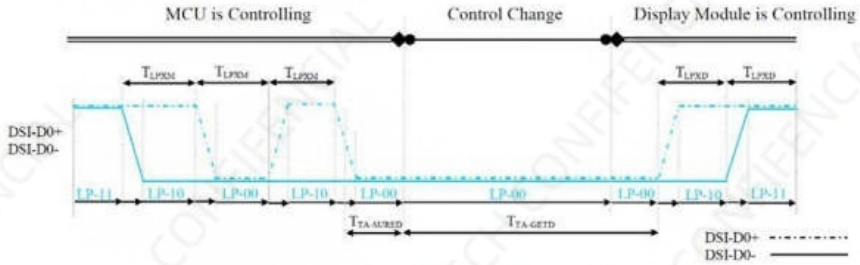


Figure 117 BTA from the MPU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module (GC9503V) to the MPU sequence below.

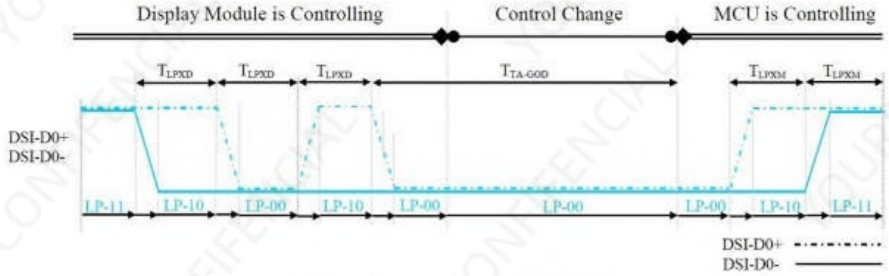


Figure 118 BTA from the Display Module to the MPU

Table 48 Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module (GC9503V)	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (GC9503V) → MPU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module (GC9503V) starts driving	T_{LPXD}	$2\times T_{LPXD}$	ns

Table 49 Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (GC9503V)	$5\times T_{LPXD}$	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MPU	$4\times T_{LPXD}$	ns

Data Lanes from Low Power Mode to High Speed Mode

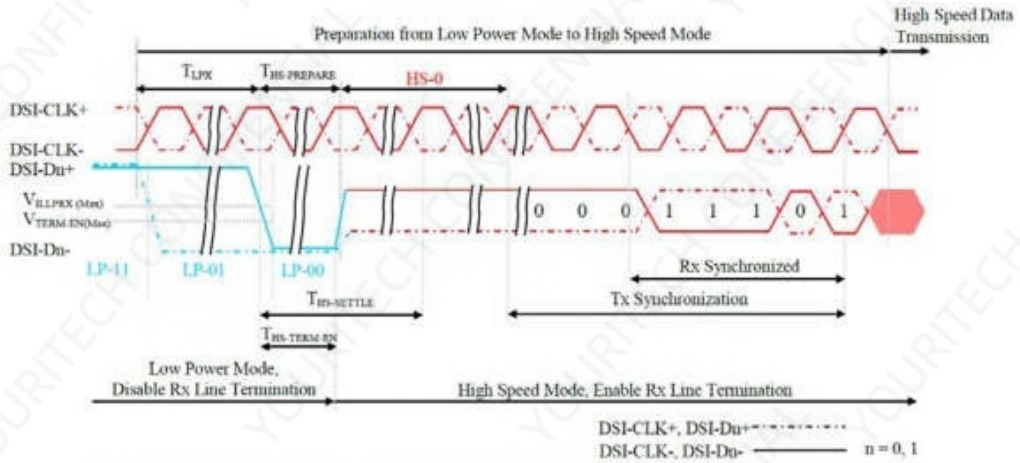


Figure 119 Data Lanes – Low Power Mode to High Speed Mode Timings

Table 50 Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-TERMEN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

Data Lanes from High Speed Mode to Low Power Mode

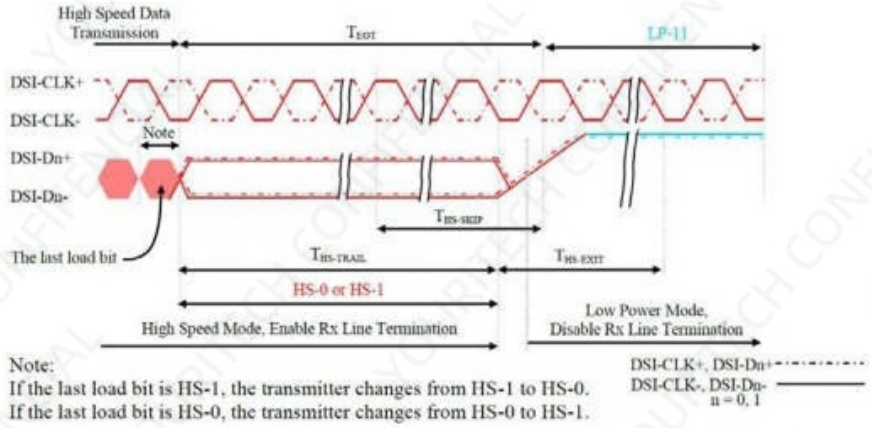


Figure 120 Data Lanes – High Speed Mode to Low Power Mode Timings

Table 51 Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (GC9503V) to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

DSI Clock Burst – High Speed Mode to/from Low Power Mode

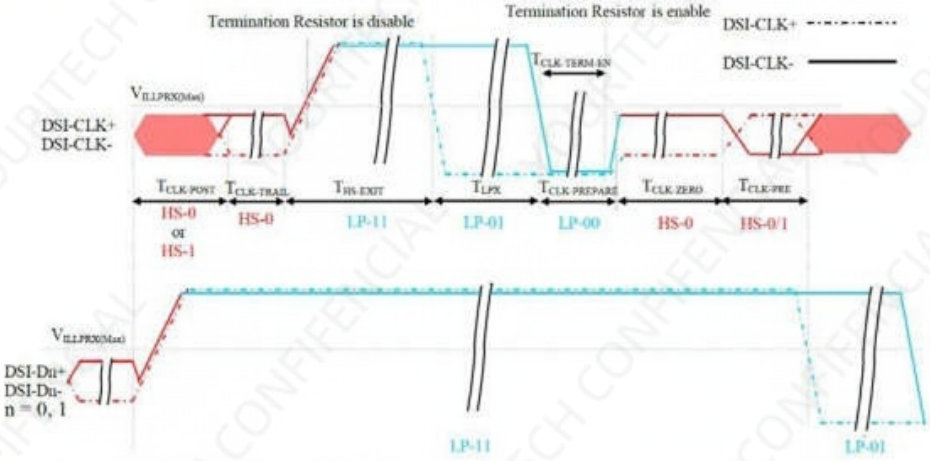


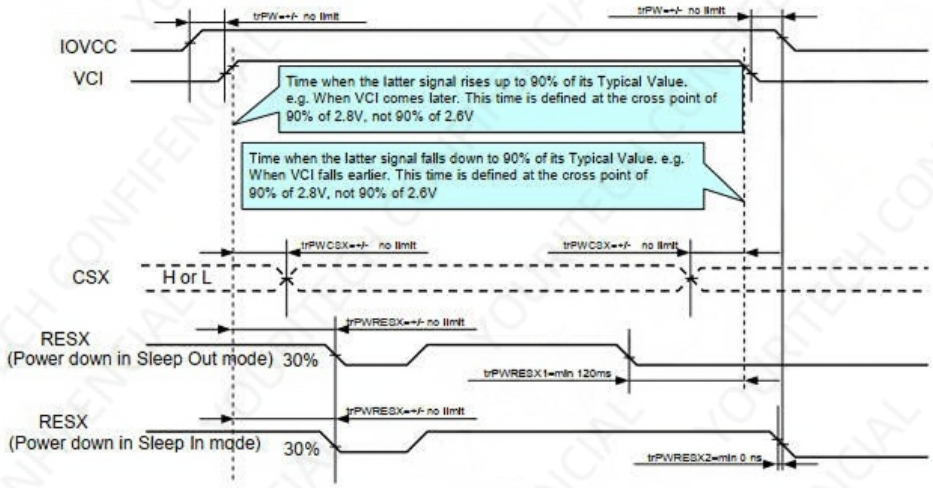
Figure 121 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Table 52 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

Reset Timing:

If the RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode

trPWRESX2 is applied to RESX falling in the Sleep In Mode

7.Optical Characteristics

7.1 Optical Specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T (%)	Θ=0 Normal viewing angle	—	3.82	—	%	using Normal Polarizer，Reference Only
Transmittance (without Polarizer)		T (%)		—	12.15	—	%	—
Contrast Ratio		CR		800	1000	—		(1)(2)
Response Time	Rising	T_R		—	16	21	msec	
	Falling	T_F		—	19	24		
Color Gamut	S(%)			—	70	—	%	C-Light
Color Chromaticity (CIE1931)	White	W_x		0.290	0.310	0.330		
		W_y		0.316	0.336	0.356		
	Red	R_x		0.631	0.651	0.671		
		R_Y		0.297	0.317	0.337		
	Green	G_x		0.255	0.275	0.295		
		G_Y		0.566	0.586	0.606		
	Blue	B_x		0.120	0.140	0.160		
		B_Y		0.068	0.088	0.108		
Viewing Angle	Hor.	$Θ_L$	CR>10	—	80	—		
		$Θ_R$		—	80	—		
	Ver.	$Θ_U$		—	80	—		
		$Θ_D$		—	80	—		
Optima View Direction		Free						(5)

7.2 Measuring Condition

■ Measuring surrounding： dark room

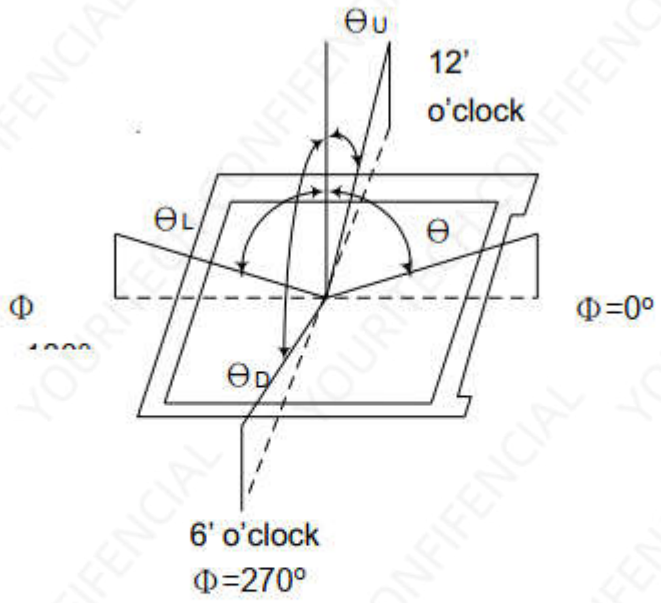
■ Ambient temperature： 25±2oC

■ 15min. warm-up time.

7.3 Measuring Equipment

■ FPM520 , which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

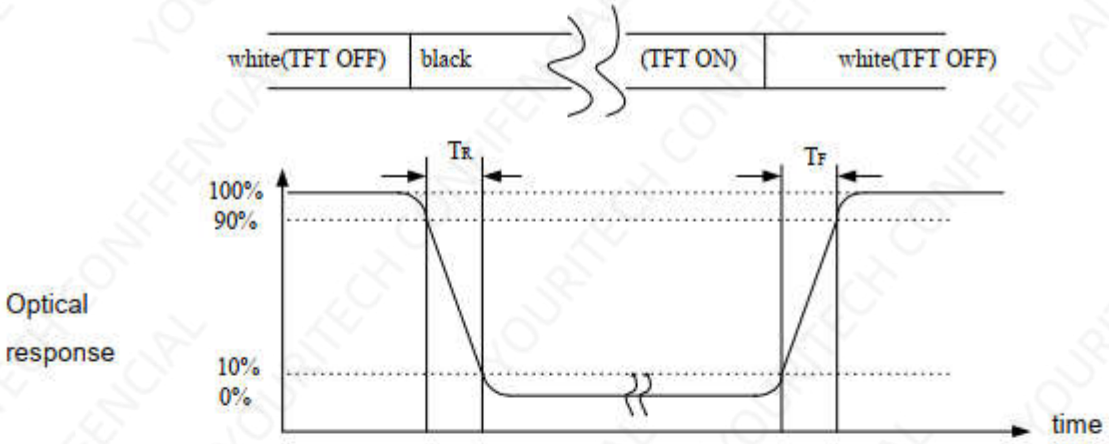
Note (1) Definition of Viewing Angle:



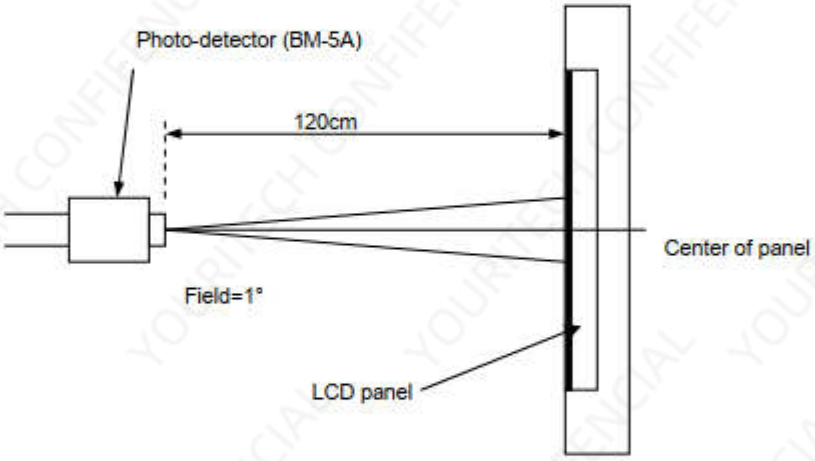
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

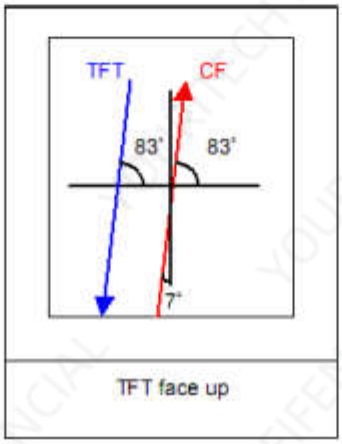
Note (3) Definition of Response Time: Sum of T_R and T_F



Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+70°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+60°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH / 96H	
6	Thermal and cold shock	Static state， -20℃（30min） ~70℃（30min），50 cycles	