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**MODEL NO : ET047HD01-T**

**MODEL VERSION: 01**

**SPEC VERSION : 1.0**

**ISSUED DATE: 2022-07-07**

□**Preliminary Specification**

■**Final Product Specification**

**Customer :**_____

| Approved by | Notes |
|---|---|
| | |

**Youri Confirmation**

| Prepared by | Reviewed by | Approved by |
|---|---|---|
| John | Johnny | Wang |

# 1. Introduction

## 1.1 Scope of application

LCD specification: Dots 720xRGBx1280.
As to basic specification of the driver IC, refer to the IC (JD936DA-H3) specification and data book.
All material & processing of the LCD module should be Lead Free.

## 1.2 TFT features:

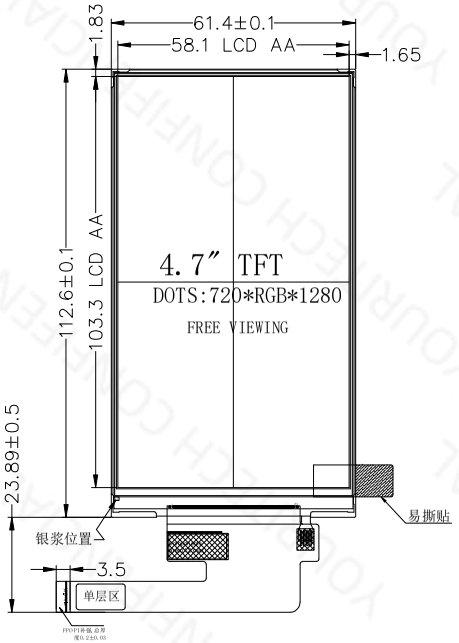
Structure: TFT PANNEL+IC +FPC1+BL;
IPS Type LCD
720dot-segment and 1280 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
4 Lane MIPI Interface can be selected by software;

## 1.3 Applications:

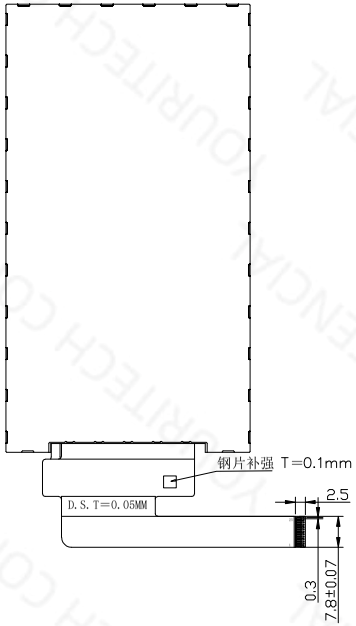
## 2. LCM General specification

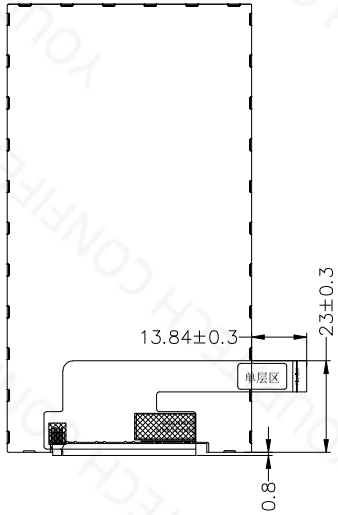
| ITEM | Sandard value | Unit |
|---|---|---|
| LCD Type | Normally Black | -- |
| Drive element | TFT active matrix | -- |
| Number of pixels | 720*3RGB(H)X1280(V) | Dots |
| Pixel arrangement | RGB stripe | -- |
| Pixel Pitch (W*H) | 0.0807(W) × 0.0807(H) | mm |
| Active area | 58.10(W) × 103.30(H) | mm |
| Viewing direction | ALL O'CLOCK | -- |
| TFT Driver IC | JD936DA-H3 | -- |
| TFT interface | 4 lane Interface | -- |
| Module Size(W*H*T) | 61.40(W) ×112.60(H) ×1.6(T) | mm |
| Approx. Weight | TBD | g |
| Touch structure | -- | -- |
| Touch Driver IC | -- | -- |
| Touch Interface | -- | -- |

| REV | DESCRIPTION | DRG DATE | DRAWN BY |
|---|---|---|---|
| | First Desing | 2022.07.07 | |








折弯示意图
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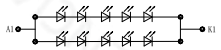
| PIN: | SYMBLE |
|---|---|
| 1 | GND |
| 2 | LED+ |
| 3 | LED- |
| 4 | GND |
| 5 | VCC_2.8 |
| 6 | GND |
| 7 | VDDIO_1.8V |
| 8 | RST |
| 9 | LPTE |
| 10 | NC(ID) |
| 11 | GND |
| 12 | MIPI_TCN |
| 13 | MIPI_TCP |
| 14 | GND |
| 15 | MIPI_TDN0 |
| 16 | MIPI_TDP0 |
| 17 | GND |
| 18 | MIPI_TDN1 |
| 19 | MIPI_TDP1 |
| 20 | GND |
| 21 | MIPI_TDN2 |
| 22 | MIPI_TDP2 |
| 23 | GND |
| 24 | MIPI_TDN3 |
| 25 | MIPI_TDP3 |

MIPI-4lane




背光电路图 (CIRCUIT DIAGRAM)

NOTES:
1. DISPLAY TYPE: 4.7″, 720*1280 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: Free
4. DRIVER IC:JD936DA-H3
5. LCM (White 9 AVG 1/9) :
   Brightness: 280cd/$m^2$ (TYP)
   Uniformity:80%(MIN)
6. BACK LIGHT: 10 chip white LEDs If=40mA,Vf=14.5V-16V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS

深圳市优瑞泰克科技有限公司

| | | | | | |
|---|---|---|---|---|---|
| PART NO.: | ET047HD01-T | | | MODULE NO.: | 00 |
| DRAWN BY: | LIU | DATE: | | PROJECTION: | |
| CHECKED BY: | | DATE: | | SCALE:N.T.S | UNIT: mm |
| APPROVED BY: | | DATE: | | SHEET: 1 OF 1 | |

# 3.Absolute Maximum Rating

| Characteristics | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| LCM Operating Temperature | $T_{OPR}$ | -20 | +70 | °C |
| LCM Storage Temperature | $T_{STG}$ | -30 | +80 | °C |
| Humidity | RH | -- | 90 | % |

# 4.Electrical Characteristics

## 4.1 TFT DC Characteristics

| Characteristics | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply Voltage for I/O | VDDIO | 1.65 | 1.8 | 3.3 | V |
| Supply Voltage for(DC/DC) | VDD | 2.5 | 2.8 | 3.6 | V |
| Supply Voltage for(DC/DC) | AVDD | -- | -- | -- | V |
| Supply Voltage for(DC/DC) | AVEE | -- | -- | -- | V |

## 4.2 Back-Light Unit Characeristics

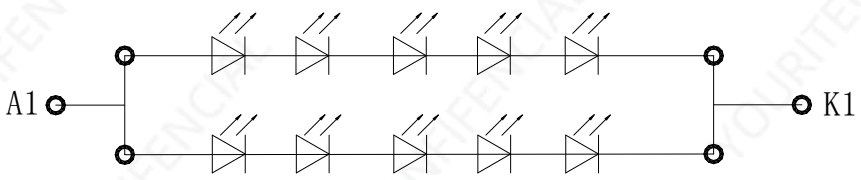
The back-light system is an edge-lighting type with 10 white LEDs. The characteristics of the back-light are shown in the following tables.

| Characteristics | Symbol | Min. | Type | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Forward Voltage | $V_F$ | 14.5 | -- | 16 | V | -- |
| Forward current | $I_F$ | -- | 40 | -- | mA | -- |
| Luminance(With LCD) | Lv | -- | 280 | -- | $cd/m^2$ | -- |
| LED life time | N/A | -- | 30,000 | -- | Hr | Note 1 |

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at $I_L$=20mA/LED. The LED life time could be decreased if operating $I_L$ is larger than 25mA/LED.

Backlight circuit diagram shown in below:



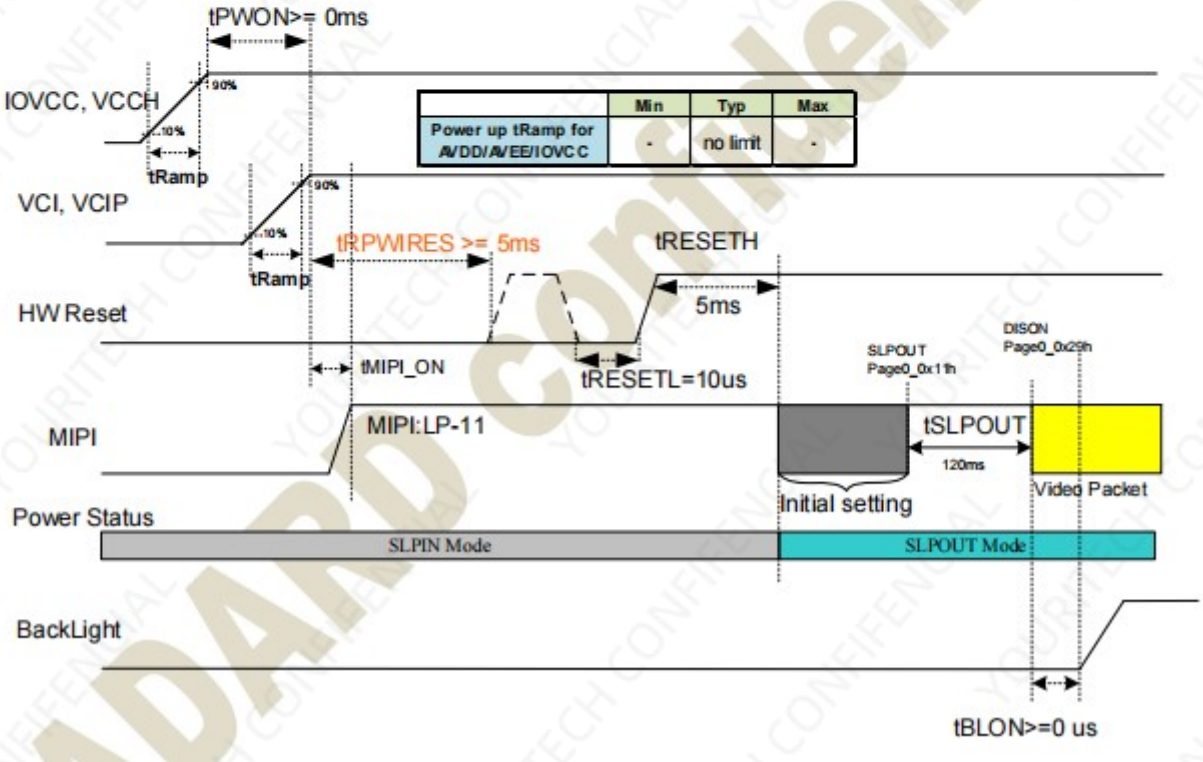
# 5. Module Function Description

| Pin No. | Symbol | Functional | Notes |
|---|---|---|---|
| 1 | GND | Power Ground | |
| 2 | LEDA | Power supply for backlight anode input terminal. | |
| 3 | LEDK | Power supply for backlight cathode input terminal. | |
| 4 | GND | Power Ground | |
| 5 | VCC 2.8V | Power supply 2.5-3.6V | |
| 6 | GND | Power Ground | |
| 7 | VDDIO 1.8V | Power supply 1.65-3.3V | |
| 8 | RST | Reset signal input terminal. Active at 'L'. | |
| 9 | LPTE | Tearing effect signal is used to synchronize MCU to frame memory | |
| 10 | NC(ID) | NC | |
| 11 | GND | Power Ground | |
| 12 | TCN | MIPI-DSI CLOCK differential signal input pins | |
| 13 | TCP | MIPI-DSI CLOCK differential signal input pins | |
| 14 | GND | Power Ground | |
| 15 | TDN0 | MIPI-DSI Data differential signal input pins | |
| 16 | TDP0 | MIPI-DSI Data differential signal input pins | |
| 17 | GND | Power Ground | |
| 18 | TDN1 | MIPI-DSI Data differential signal input pins | |
| 19 | TDP1 | MIPI-DSI Data differential signal input pins | |
| 20 | GND | Power Ground | |
| 21 | TDN2 | MIPI-DSI Data differential signal input pins | |
| 22 | TDP2 | MIPI-DSI Data differential signal input pins | |
| 23 | GND | Power Ground | |
| 24 | TDN3 | MIPI-DSI Data differential signal input pins | |
| 25 | TDP3 | MIPI-DSI Data differential signal input pins | |

## 6. Timing Characteristics

| Symbol | Min | Typ | Max | Unit | Remark |
|---|---|---|---|---|---|
| tRamp | - | no limit | - | us | |
| tPWON | 0 | - | - | ms | |
| tON1 | 0 | - | - | ms | |
| tMIPI-ON | 0 | - | tRPWIRES | ms | |
| tRPWIRES | 5 | - | - | ms | |
| tRESETL | 10 | - | - | us | |
| tRESETH | 5 | - | - | ms | |
| tSLPOUT | 120 | - | - | ms | |
| tBLON | 0 | - | - | ms | |

BOOSTM[1:0]=10 (Internal DC/DC power mode : Charge Pump, FP7721)
VCCD=IOVCC=VCCH=1.65V ~ 3.6V, VCI=VCIP=2.5V ~ 4.8V.
Power on:




| | Min | Typ | Max |
|---|---|---|---|
| Power up tRamp for AVDD/AVEE/IOVCC | - | no limit | - |

### High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 13.5.

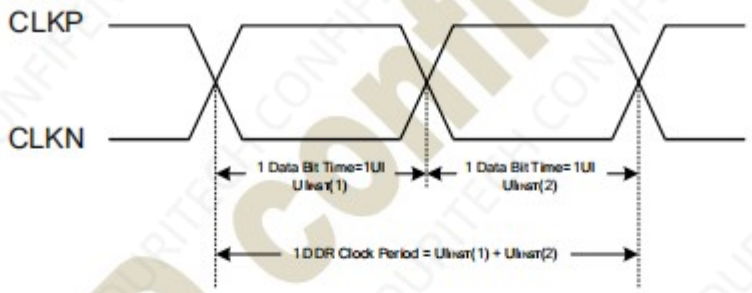



**Figure 11.5: DDR Clock Definition**

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in following Table.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| UI instantaneous | $UI_{INST}$ | - | - | 12.5 | ns | (1), (2), (3), (4), (5), (6) |

**Note:** (1) This value corresponds to a minimum 80 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Maximum total bit rate is 850bps of 1 data lane 24-bit data format/ 630Mbps of 1 data lane 18-bit data format/ 560Mbps of 1 data lane 16-bit data format.
(4) Maximum total bit rate is 1.7Gbps of 2 data lanes 24-bit data format/ 1.27Gbps of 2 data lane 18-bit data format/ 1.13Gbps of 2 data lane 16-bit data format.
(5) Maximum total bit rate is 2Gbps of 3 data lanes 24-bit data format/ 1.5Gbps of 3 data lane 18-bit data format/ 1.33Gbps of 3 data lane 16-bit data format.
(6) Maximum total bit rate is 2Gbps of 4 data lanes 24-bit data format/ 1.5Gbps of 4 data lane 18-bit data format/ 1.33Gbps of 4 data lane 16-bit data format.

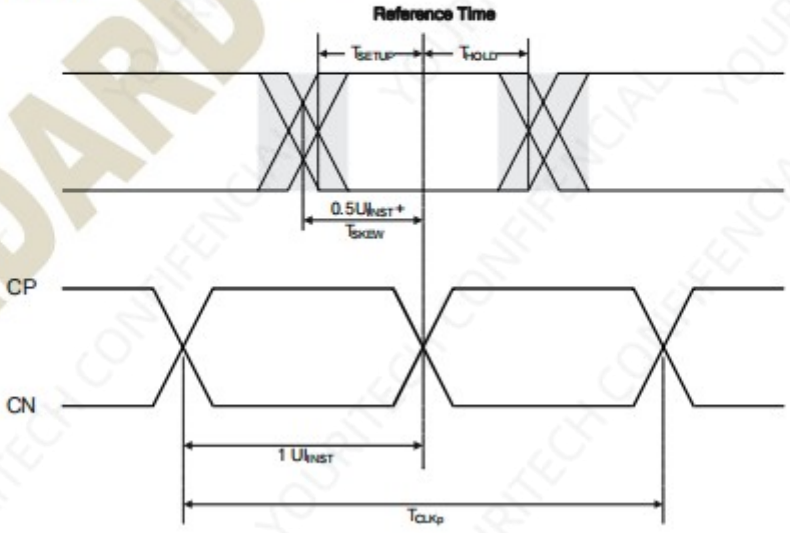
**Table 11.11: Reverse HS Data Transmission Timing Parameters**

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.13. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.



### Low-Power Receiver (RX)

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The Figure 13.4 shows Input Glitch Rejection of Low-Power RX. In addition, under tables list DC and AC characteristic for LP-RX.

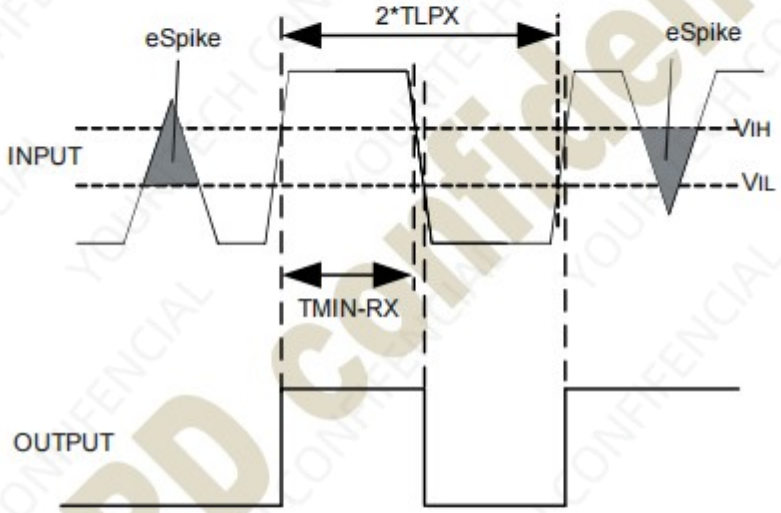



**Figure 11.4: Input Glitch Rejections of Low-Power Receivers**

| Parameter | Description | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Logic 1 input threshold | 880 | - | - | mV | - |
| $V_{IL}$ | Logic 0 input threshold, not in ULP state | - | - | 550 | mV | - |

**Table 11.6: LP-RX DC Specifications**

| Parameter | Description | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| $e_{SPIKE}$ | Input pulse rejection | - | - | 300 | V.ps | 1, 2, 3 |
| $T_{MIN}$ | Minimum pulse width response | 20 | - | - | ns | 4 |
| $V_{INT}$ | Peak-to-peak interference voltage | - | - | 200 | mV | - |
| $f_{INT}$ | Interference frequency | 450 | - | - | MHz | - |

**Note:** (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state
(2) An impulse less than this will not change the receiver state.
(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
(4) An input pulse greater than this shall toggle the output.

## Burst Mode Data Transmission

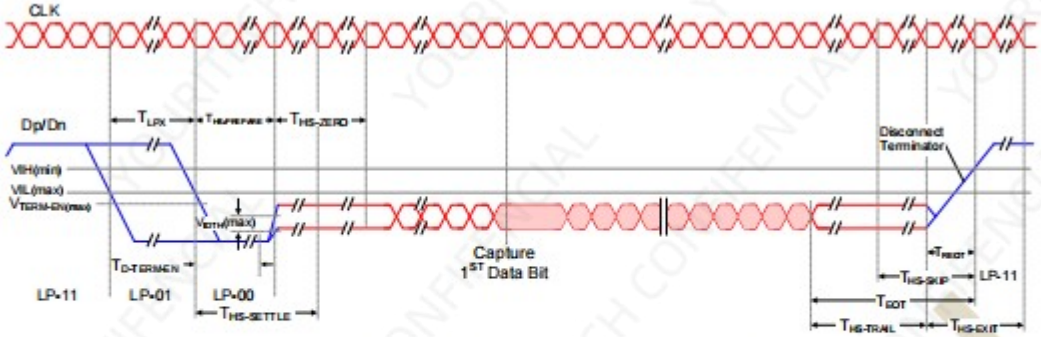



**Figure 11.7: High-Speed Data Transmission in Bursts**

| Parameter | Description | Min | Typ | Max | UNIT |
|---|---|---|---|---|---|
| $T_{LPX}$ | Transmitted length of any Low-Power state period | 50 | - | - | ns |
| $T_{HS-PREPARE}$ | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission | 40 + 4*UI | - | 85 + 6*UI | ns |
| $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ | $T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. | 145 + 10*UI | - | - | ns |
| $T_{D-TERM-EN}$ | Time for the Data Lane receiver to enable the HS line termination. | - | - | 35 + 4*UI | ns |
| $T_{HS-SETTLE}$ | Time interval during which the HS receiver shall ignore any Data Lane HS transitions. | 85 + 6*UI | - | 145 + 10*UI | ns |
| $T_{HS-TRAIL}$ | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst | max( n*8*UI, 60 + n*4*UI ) | - | - | ns |
| $T_{HS-EXIT}$ | Time that the transmitter drives LP-11 following a HS burst. | 100 | - | - | ns |

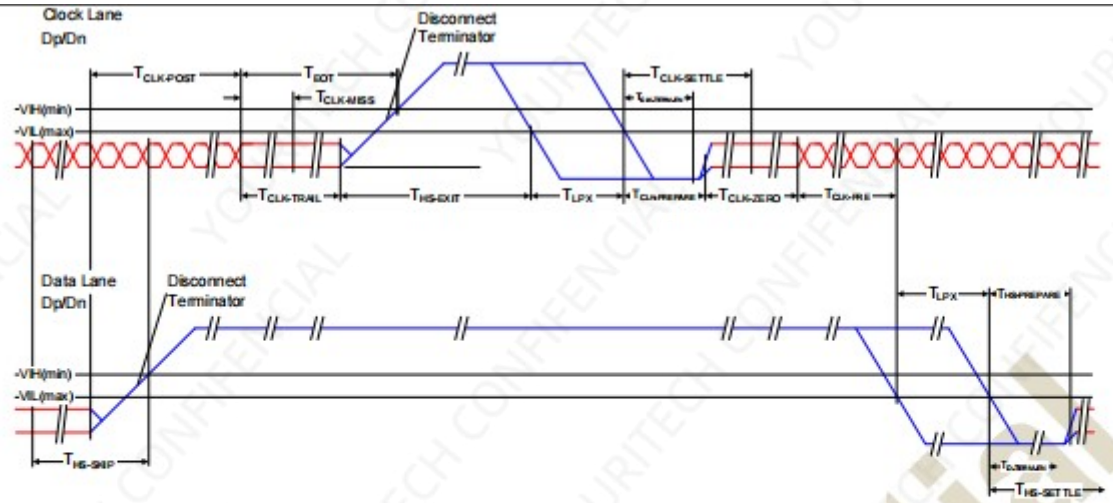



**Figure 11.8: Switching the Clock Lane between Clock Transmission and Low-Power Mode**

| Parameter | Description | Min | Typ | Max | UNIT |
|---|---|---|---|---|---|
| $T_{CLK-POST}$ | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. | 60 + 52*UI | - | - | ns |
| $T_{CLK-PRE}$ | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8*UI | - | - | ns |
| $T_{CLK-PREPARE}$ | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | 38 | - | 95 | ns |
| $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | $T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock. | 300 | - | - | ns |
| $T_{CLK-TERM-EN}$ | Time for the Clock Lane receiver to enable the HS line termination. | - | - | 38 | ns |
| $T_{CLK-TRAIL}$ | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst. | 60 | - | - | ns |
| $T_{HS-EXIT}$ | Time that the transmitter drives LP-11 following a HS burst. | 100 | - | - | ns |

## Reset input timings

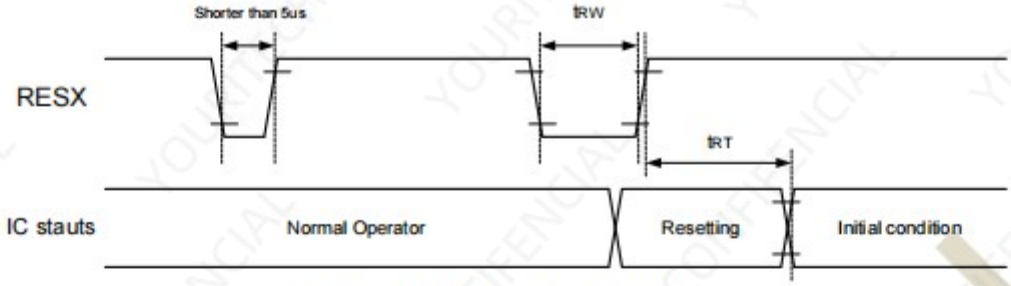



**Figure 11.1: Reset input timings**

| Symbol | Parameter | Related pins | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{RW}$ | Reset pulse width(2) | RESX | 10 | - | µs |
| $t_{RT}$ | Reset complete time(3) | - | - | 5 (Note 5) | ms |
| | | - | - | 120 (Note 6, 7) | ms |

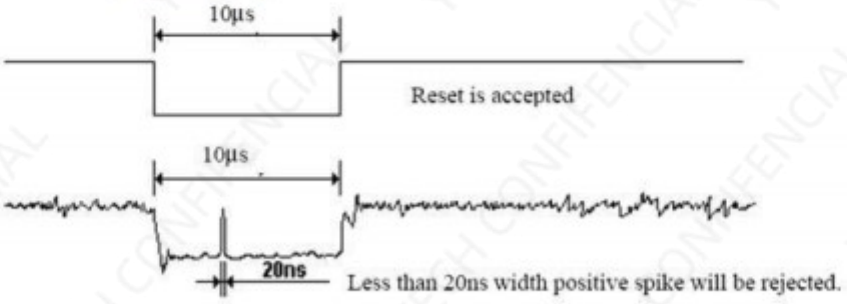
**Note:** (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

| RESX Pulse | Action |
|---|---|
| Shorter than 5 µs | Reset Rejected |
| Longer than 10 µs | Reset |
| Between 5 µs and 10 µs | Reset Start |

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:




(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

## 7.Optical Characteristics

| Parameter | | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|---|
| Viewing Angle range | Horizontal | $\Theta_3$ | CR > 10 | - | 80 | - | Deg. | Note 1 |
| | | $\Theta_9$ | | - | 80 | - | Deg. | |
| | Vertical | $\Theta_{12}$ | | - | 80 | - | Deg. | |
| | | $\Theta_6$ | | - | 80 | - | Deg. | |
| Luminance Contrast ratio | | CR | Θ = 0° | 1200 | 1500 | - | | Note 2 |
| Transmittance | | T(%) | Θ = 0° | 3.87 | 4.3 | - | % | Base on C light Note 3 With APF |
| White Chromaticity | | $x_w$ | Θ = 0° | 0.263 | 0.293 | 0.323 | | Color Filter ( with ITO ) Based On C light Note 4 |
| | | $y_w$ | | 0.299 | 0.329 | 0.359 | | |
| Reproduction of color | Red | $x_R$ | Θ = 0° | 0.635 | 0.665 | 0.695 | | |
| | | $y_R$ | | 0.289 | 0.319 | 0.349 | | |
| | Green | $x_G$ | | 0.227 | 0.257 | 0.287 | | |
| | | $y_G$ | | 0.547 | 0.577 | 0.607 | | |
| | Blue | $x_B$ | | 0.107 | 0.137 | 0.167 | | |
| | | $y_B$ | | 0.065 | 0.095 | 0.125 | | |
| Threshold Voltage | | Vsat | | 3.7 | 3.9 | 4.1 | V | Figure 3 |
| | | Vth | | 1.8 | 2.0 | 2.2 | V | |
| Response Time (Rising + Falling) | | $T_{RT}$ | Ta= 25° C Θ = 0° | - | 25 | 30 | ms | Note 5 |

Notes : 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 4 shown in Appendix).

2. Contrast measurements shall be made at viewing angle of Θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (see Figure 4) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with Polarizer

4. The color chromaticity coordinates specified in Table 4 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel. Measurement condition is C- light Source & Halogen Lampe

5. The electro-optical response time measurements shall be made as Figure 5 by switching the "data" input signal ON and OFF. The times needed for the transmittance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

## 8. Reliability Test Item

| No. | Test Item | Test Condition | Notes |
|---|---|---|---|
| 1 | High Temp. Storage | +80°C / 240H | 1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed.<br>2. No low temperature bubbles,end seal loose andfall, frame rainbow. |
| 2 | Low Temp. Storage | -30°C / 240H | |
| 3 | High Tempe. Operating | +70°C / 240H | |
| 4 | Low Tempe. Operating | -20°C / 240H | |
| 5 | High Temperature /Humidity storage | 50+5°C x 90%RH / 48H | |
| 6 | Thermal and cold shock | Static state，-30℃（1 hour）~60℃（1 hour） ~ -30℃（1 hour），packaging， 10 cycles | |

## 9. Packing Method----TBD

- END -