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PRODUCT SPECIFICATION

PRODUCT 产品规格: 4.7″ TFT

MODEL NO. 模组型号: ET047HD03-V

CUSTOMER 客户:

SPECIFICATION

FOR

ET047HD03-V 产品规格书

版本: V 1.0

Customer Confirmation column 客户确认栏 Approved by 核准: _____ Dept. 部门: _____ Data 日期: _____ Please return one of the copies of the specification with your signature to us 请贵司在收到规格书的两周内，将签好字的规格书原件或者复印件寄回.如果没有返回， within two weeks after you receive this document. If it is not returned, we will 我司将会认为贵司已经默认接受产品规格书中的全部资料和规范. assume that you agree to the entire contents of this specification document.

● Preliminary Specification 样品规格书 ☼ Final Specification 量产规格书 Design 制作: _____ Check 检查: _____ Approval 审核: _____

Revision History

PRODUCT SPECIFICATION

Version NO.	DATE	Description	Remark
V1.0	2018.3.26	Original	

PRODUCT SPECIFICATION

CONTENTS 内容

1. GENERAL INFORMATION

1.1 features

1) Display Format: 4.7” HD Vertical Stripe (720*1280)
2) Interface : MIPI 4 lane
3) Operation Temperature : -20~70℃
4) Storage Temperature : -30~80℃
5) Backlight Type: White LED
6) Display mode: Normally Black

1.2 mechanical specification

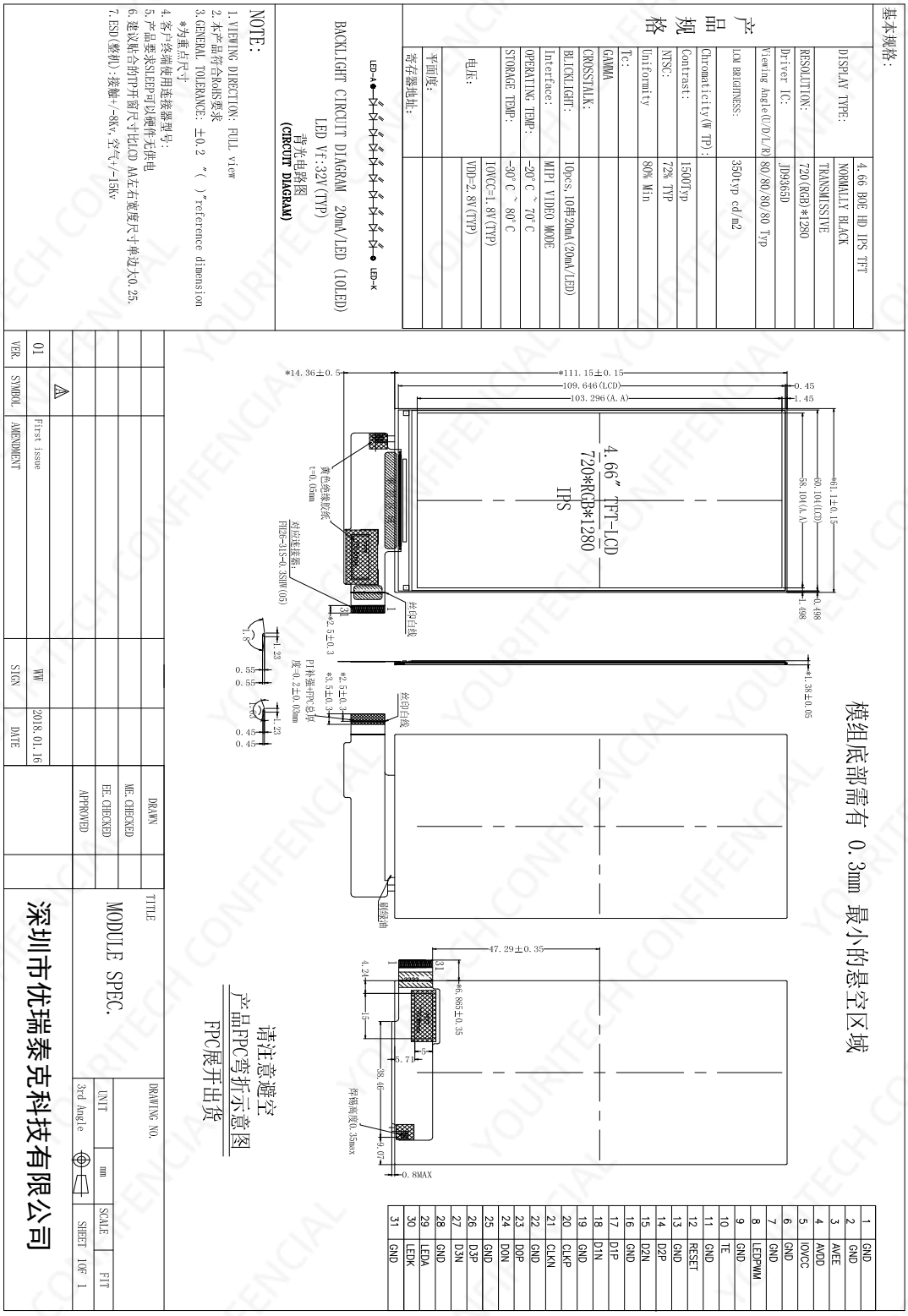
Item of	Contents	Unit
LCD Type	IGZO TFT/TRANSMISSIVE	/
Panel Size	4.7	inch
Pixel arrangement	720*3(RGB)*1280	Dots
Active Area	58.104 (H)*103.296(V)	mm
Pixel pitch (W*H)	0.0269(H)*0.0807(V)	mm
Module area (W*H*T)	61.1(H)*111.15(V)*1.38(D)	mm
Recommended Viewing Direction	All	0’ clock

2. ABSOLUTE MAXIMUM RATINGS

(GND=AGND=0V)

Parameter of absolute maximum ratings 参数	Symbol 符号	Min 最小值	Max 最大值	Unit 单位
Power voltage supply1	IOVCC	-0.3	+4.6	V
Power voltage supply2	AVDD	-0.3	+6.6	V
Power voltage supply3	AVEE	-6.6	0	V
Backlight forward current	I_{LED}	-0.001	30	mA(For each led)
Reverse Voltage	V_R	-	+5	V
Operating temperature	Top	-20	+70	°C
Storage temperature	Tst	-30	+80	°C

3. DIAGRAM FOR LCM



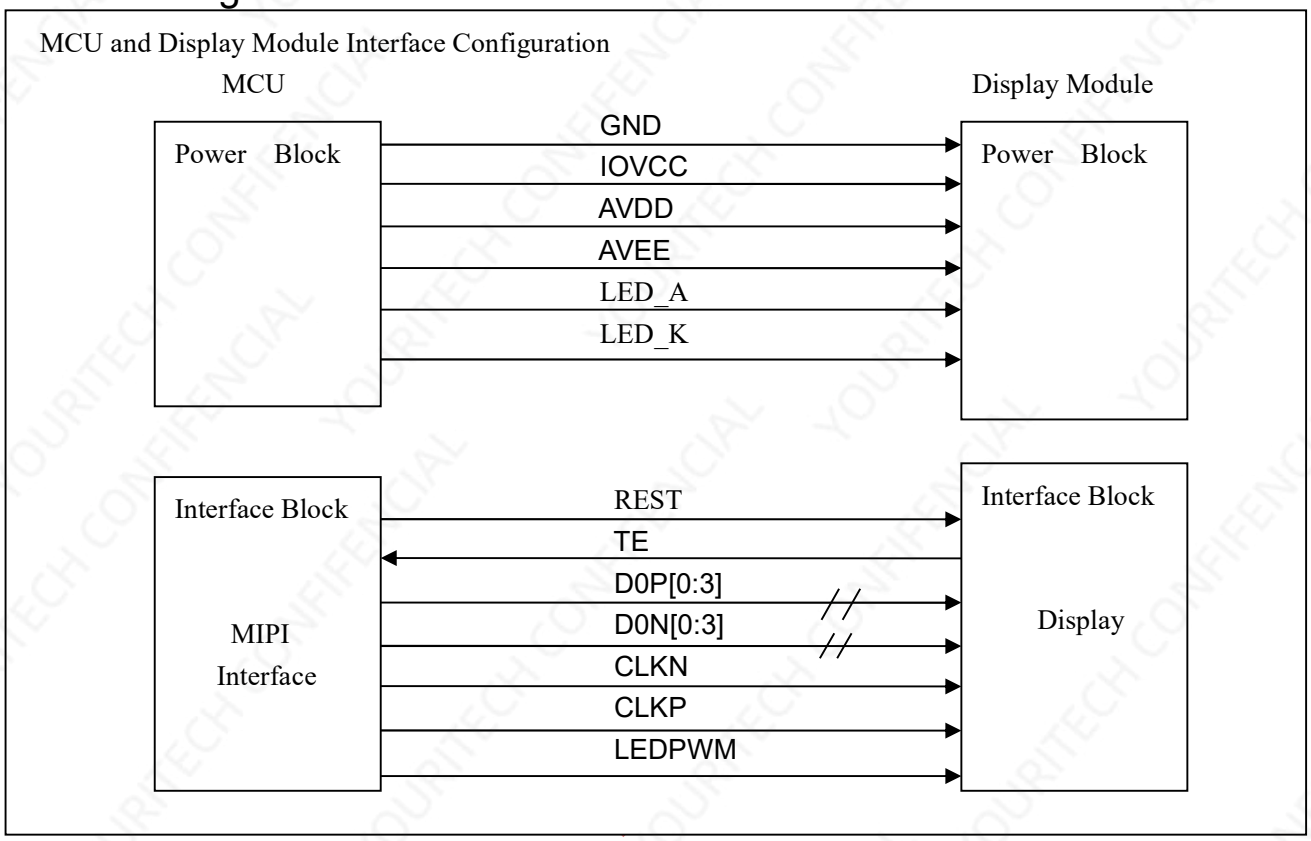
4. I/O CONNECTION & BLOCK DIAGRAM

4.1 I/O connection

LCM Pin NO.	Symbol	I/O	Description
1-2	GND	P	Power Ground
3	AVDD	P	Input voltage from the set-up circuit. it is generated from VCIP
4	AVEE	P	Input voltage from the set-up circuit. it is generated from AVEE
5	IOVCC	P	A power supply for digital circuit and IO pads(1.8V)
6-7	GND	P	Power Ground
8	LEDPWM	O	Backlight on/off control pin. If use CABC function, the pin can connect to external
9	GND	P	Power Ground
10	TE	O	Tearing effect output pin to synchronize MCU to frame writing
11	GND	P	Power Ground
12	REST	I	The signal will reset the LCM, Signal is active low.
13	GND	P	Power Ground
14	D2P	I	Differential data signals for MIPI interface
15	D2N	I	Differential data signals for MIPI interface
16	GND	P	Power Ground
17	D1P	I	Differential data signals for MIPI interface
18	D1N	I	Differential data signals for MIPI interface
19	GND	P	Power Ground
20	CLKP	I	Differential clock signals for MIPI interface
21	CLKN	I	Differential clock signals for MIPI interface
22	GND	P	Power Ground
23	D0P	I/O	Differential data signals for MIPI interface
24	D0N	I/O	Differential data signals for MIPI interface
25	GND	P	Power Ground
26	D3P	I	Differential data signals for MIPI interface
27	D3N	I	Differential data signals for MIPI interface
28	GND	P	Power Ground
29	LEDA	P	Power supply for LED+
30	LEDK	P	Power supply for LED-
31	GND	P	Power Ground

I：Input；O：Output；P：Power

4.2 block diagram

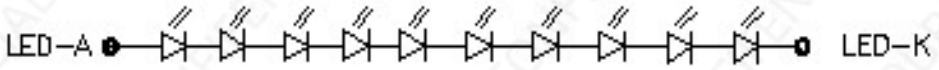


5. ELECTRICAL CHARACTERISTICS

5.1 Typical Operation Conditions

Item	Symbol	Values			Unit	Remarks
		Min.	Typ.	Max.		
Power Voltage Supply1	IOVCC	1.65	1.8	3.3	V	
Power Voltage Supply2	AVDD	3.3	5	6.6	V	
Power Voltage Supply3	AVEE	-6.6	-5	0	V	
Luminance for LCM	Lv	-	400	-	cd/m2	
Backlight Forward Voltage	Vf	-	32	-	V	
LED Forward Current	If	-	40	-	MA	Note

Note:The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20Ma(for each led). The LED life time could be decreased if operating $I_L$is larger than 20mA



BACKLIGHT CIRCUIT DIAGRAM 20mA/LED (10LED)
LED Vf:32V(TYP)

5. 2 Reset Timing

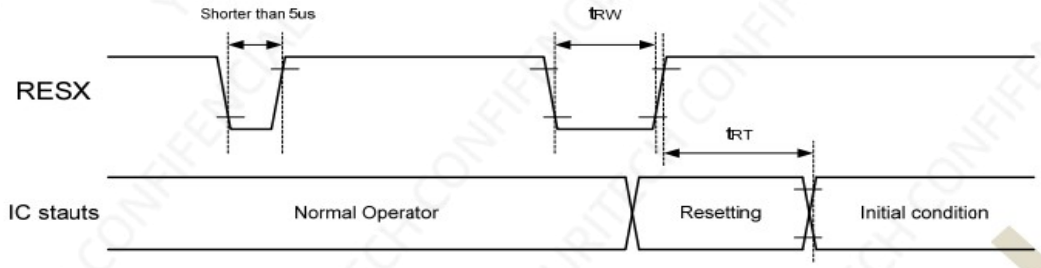


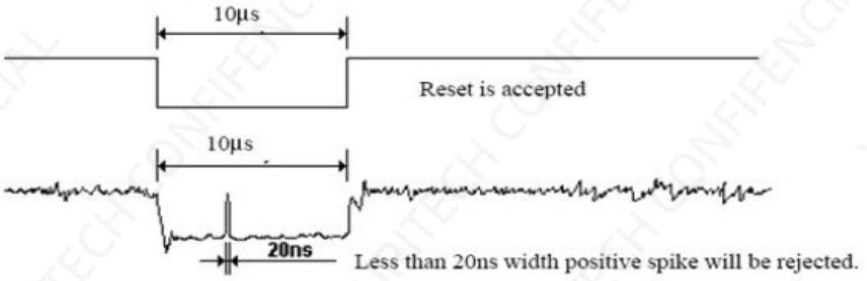
Figure 11.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width(2)	RESX	10	-	μs
t_{RT}	Reset complete time(3)	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

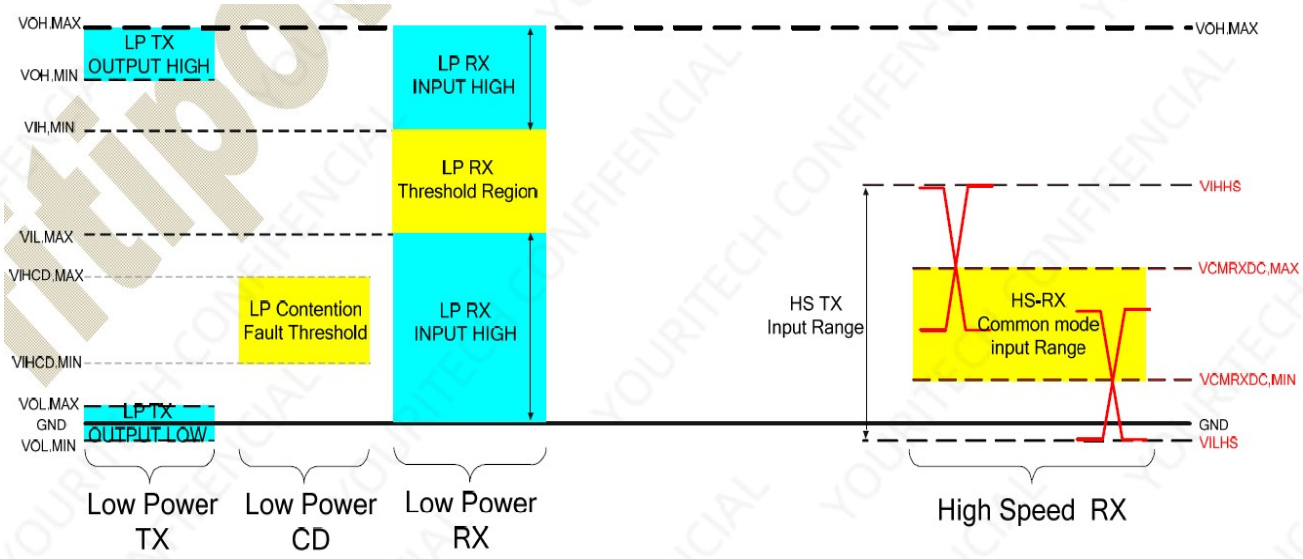
5.3 DC Characteristics for LCD

5.3.1 DC Characteristics for LCM

Item		Symbol	Min.	Typ	Max.	Unit	Note
Supply power1		IOVCC	1.65	1.8	3.3	V	-
Supply power2		AVDD	2.8	5	6.6	V	
Supply power3		AVEE	-6.6	-5	0		
Logic High level input voltage		V_{IH}	0.7* IOVCC	-	IOVCC	V	Note1
Logic Low level input voltage		V_{IL}	-0.3	-	0.3* IOVCC	V	Note1
Logic High level output voltage		V_{OH}	0.8* IOVCC	-	IOVCC	V	Note1
Logic Low level output voltage		V_{OL}	0	-	0.2* IOVCC	V	Note1
LP_RX	Logic 1 input threshold	V_{IH}	880	-	1350	V	Note3
	Logic0 input threshold,not in ULP State	V_{IL}	0.0		550	mV	
LP_TX	Output impedance of LP transmitter	Z_{OLP}	0.0	-	300	Ω	
	Thevenin output high level	V_{OH}	1.1	1.2	1.3	V	
	Thevenin output low level	V_{OL}	-50	-	50	mV	
LP_CD	Logic 1 contention threshold	V_{ILCD}	450	-	1350	mV	
	Logic 0 contention threshold	V_{ILCD}	0.0	-	200	mV	
HS_RX	Common-mode voltage HS receive mode	V_{CMRXDC}	70		330	mV	
	Differential input high threshold	V_{IDTH}	-	-	70	mV	
	Differential input low threshold	VIDTL	-70	-	-	mV	
	Single-ended input high voltage	V_{IHHS}	-	-	460	mV	
	Single-ended input low voltage	V_{ILHS}	-40	-	-	mV	
	Differential input impedance	Z_{ID}	80	100	125	Ω	

Note:

1. Ta = -20 to 60 °C, IOVCC(1.8V) =1.65V to 3.3V, AVDD=3.3V to 6.6V.



5.32 AC characteristics

Burst Mode Data Transmission

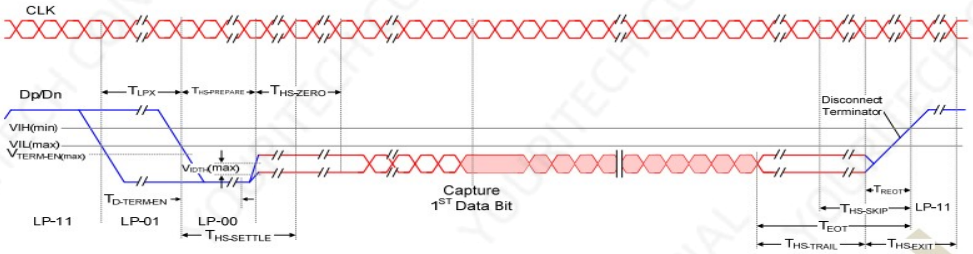


Figure 11.7: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 + n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

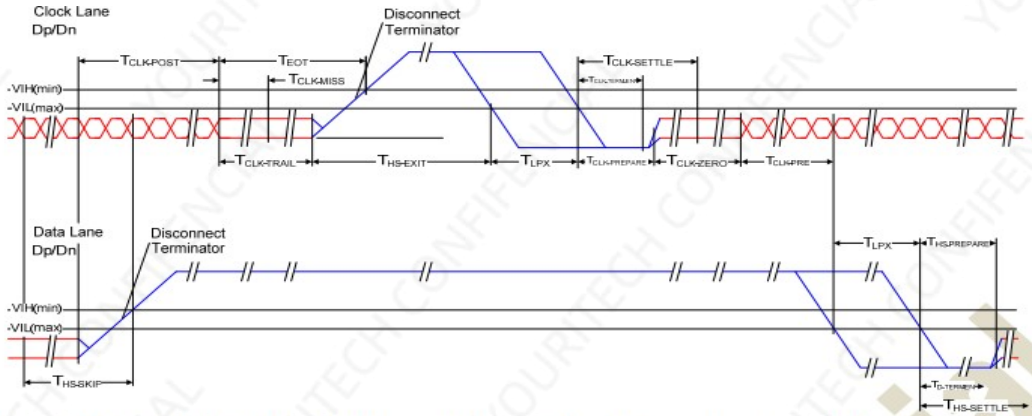


Figure 11.8: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

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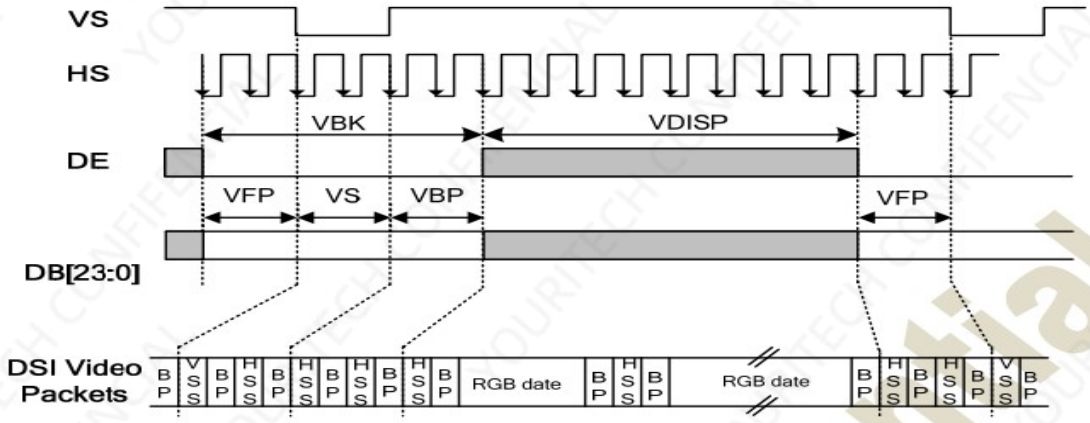
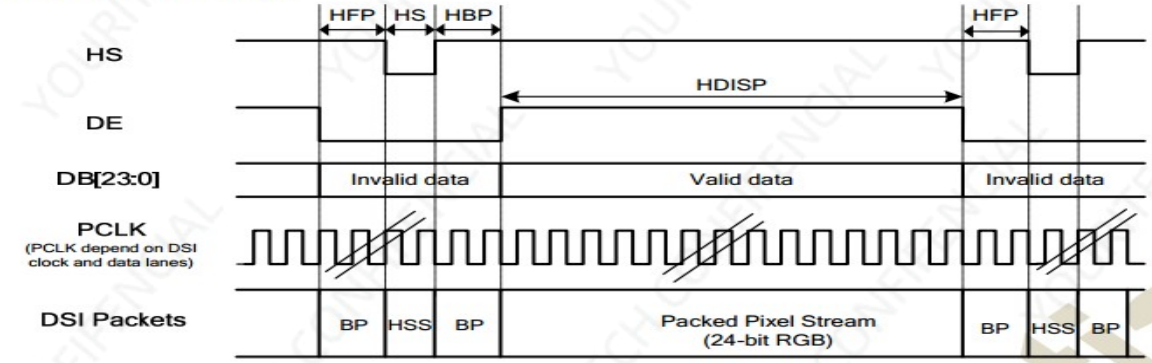
Vertical Timings



Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	-	200 Note(1)	Line
Vertical front porch	VFP	-	4	-	200	Line
Vertical back porch	VBP	-	2	-	200 Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	8	-	250	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at corresponding position for LCD normal display.

Horizontal Timings



Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	6	18	78	DCK
Horizontal back porch	HBP	-	5	18	78	DCK
Horizontal front porch	HFP	-	5	18	78	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	16	54 (Note1)	88	DCK
Horizontal active area	HDISP	-	-	720	-	DCK
			56.88 (Note2)	61.02 (Note2)	74.17 (Note2)	MHz

Note 1: HS+HBP > 0.5us.
Note 2: Pixel Clock = (HBLK+HDISP) * (VBK+VDISP) * Frame rate, Frame rate=60Hz.

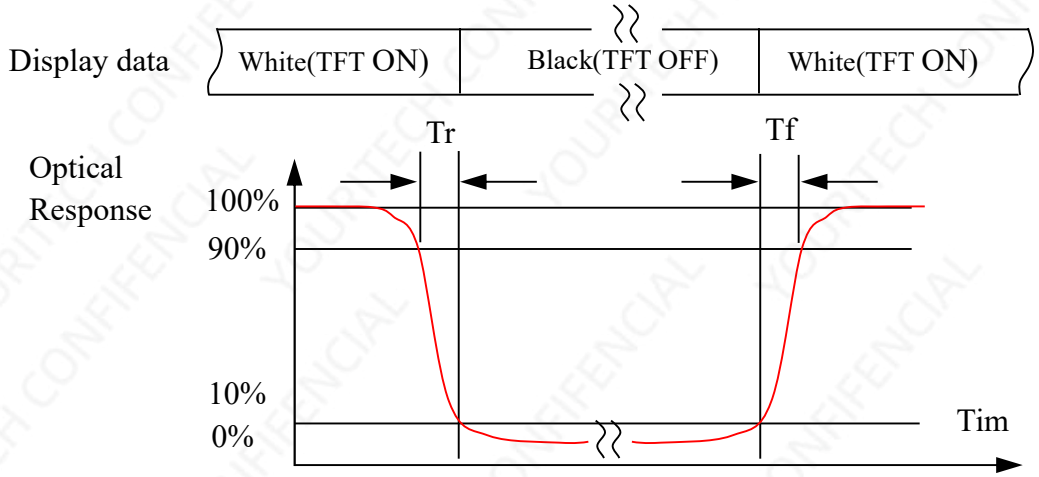
6. ELECTRO-OPTICAL CHARACTERISTICS

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio (Center point)		C/R	-	1200	1500	-	-	Note(1)
Luminance uniformity		U_W	θ = 0. Normal viewing angle B/L On Note(1)	75	80		%	Note(3)
Response Time		Tr + Tf		-	25	30	ms	Note(2)
Color Chromaticity (CIE 1931)	White	W_X		-0.02	0.2803	+0.02	-	Note(5)
		W_X			0.3234			
	Red	R_X			0.6461			
		R_Y			0.3323			
	Green	G_X			0.2960			
		G_y			0.6081			
	Blue	B_X			0.1446			
		B_Y			0.0530			
Viewing Angle	Hor.	¢3	C/R≥10		80	-	Deg	Note(4)
		¢9			80	-		
	Ver.	¢12			80	-		
		¢6		-	80	-		

Note1 Definition of Contrast Ratio (CR):

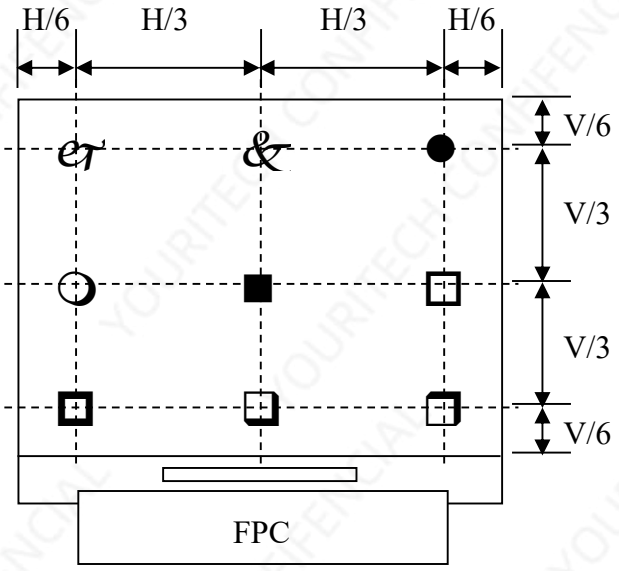
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note2: Definition of Response time: Sum of Tr and Tf



Note 3: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas (Shown in below), every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity} = \frac{\text{Min Luminance of white among 9-points}}{\text{Max Luminance of white among 9-points}} \text{x100\%}$$



The spot locations for luminance measurement

Note 5: Definition of Color Chromaticity (CIE 1931)

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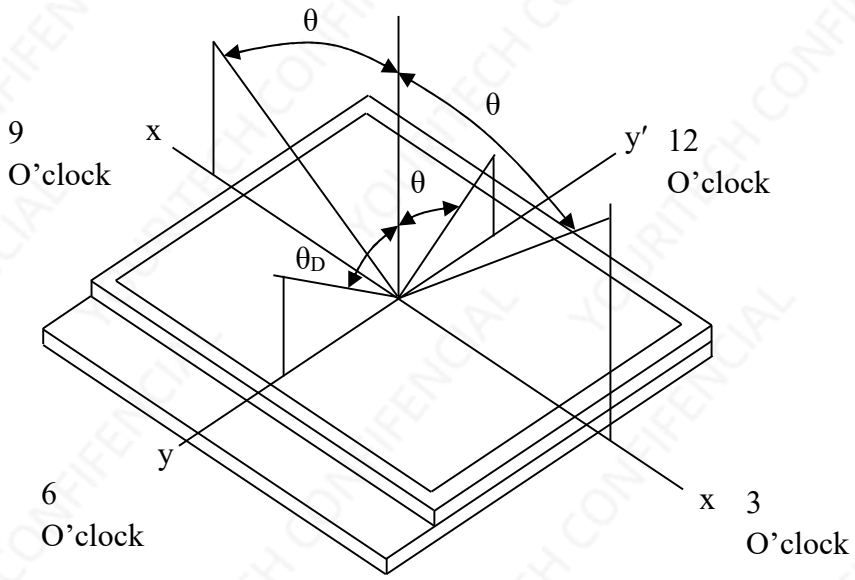
Color coordinate of white & red, green, blue at center point.

Note4.Definition of Viewing Angle: The viewing angle range that the CR≥10



7. RELIABILITY TEST CONDITIONS

No 序号	Test Item	Test Condition
1	High Temperature Storage	+80°C / 24Hours
2	Low Temperature Storage	-30°C / 24Hours
3	High Temperature Operating	+70°C / 24Hours
4	Low Temperature Operating	-20°C / 24Hours
5	Temperature Cycle	-20°C ~ 0°C~+ 60°C x 10cycles (30min) (5min) (30min)
6	Damp Proof Test	60°C x 90%RH / 24H
7	Vibration Test	Frequency: 10Hz~55Hz~10Hz Amplitude:1.5mm, 2 hours for each direction of X, Y, Z
8	Dropping test	Drop to the ground from 1m height, 1 corner, 3 edges, 6 surfaces.
9	ESD test	Contact: ±8KV Air: ±15KV 150PF/330Ω,5Points/panel,5times

Inspection after test判断标准

1. The test samples should be applied to only one test item. 每个被测试的模块只能用于其中的一个测试项目。
2. Sample size for each test item is 5~10pcs. 每个测试项目的样品数量为5～10 片.
3. For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used. 对于防潮试验，试验箱的用水必须是电阻大于10M 欧姆的纯水。
4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part. 如果由静电引起产品故障,当放置一段时间后能够恢复正常，则不视为产品缺陷。
5. EL evaluation should be excepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has. 带EL片的可靠性测试在高温高湿条件下,荧光粉会发生自然化学反应而产生黑点或瑕疵,因此不在高温高湿条件测试范围内.
6. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic. 故障判断标准:基本规格,电气特性,机械特性,光电特性

8. INSPECTION STANDARDS

8.1 AQL Sampling inspection standard

使用 GB/T 2828-2003 一般 II 水平,采用正常检查一次抽样方式；具体抽检方式参照《成品检验管理程序》、《抽样管理规范》

缺陷区分	AQL 允收水准
严重缺陷	0 收 1 退
重缺	0.4
轻缺	0.65

8.2 Inspect the condition

8.2.1 在 20—40W 日光灯的照明条件下，样品离检查者眼睛约 30cm 处进行检查。检验方向以垂直线前后左右 45°（以时钟 3 点、6 点、9 点、12 点）

8.2.2 检验者视力需达到标准视力 1.0 以上。

8.2.3 检验者需戴静电手环、两手八个手指套。

8.2.4 外观检验者以目视检查或以菲林对比卡比对。

8.2.5 电性测试使用电测测架,主板,电源线及单片机。

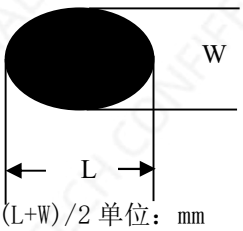
8.2.6 若标准与规格书不符时，以产品发行之规格书特殊检验规格、工程变更为准

8.2.7 辉色度检测请参照样品,检测方法依照辉色度检验标准。

8.2.8 电测检验环境:照度为 200LUX 以下,外观检验环境: 照度为 600LUX-1000LUX，检验时间：1 秒-3 秒。

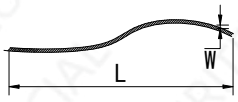
8.2.9 检验工具:电测测架,主板,电源线及单片机,菲林对比卡,游标卡尺,放大镜,实体显微镜(必要时)等等。

8.3 Judgment criterion

<table>
<tr><td>不良项目</td><td colspan="3">判定标准</td><td>缺点类别</td></tr>
<tr><td rowspan="4">点状缺陷</td><td rowspan="4"> 

D=(L+W)/2 单位： mm
点不良间距需≥10mm</td><td>尺寸</td><td>允许个数</td><td rowspan="3">轻缺</td></tr>
<tr><td>D≤0.2</td><td>忽略不计</td></tr>
<tr><td>0.2＜D≤0.3</td><td>3</td></tr>
<tr><td>D＞0.3</td><td>0</td><td></td></tr>
<tr><td>亮点</td><td rowspan="3">1.单一点：单个 DOT
2.连续点：相连 2 个 DOT
3.亮点及暗点总个数不可超过 5 个
4.点不良间距需≥10mm</td><td>单一点</td><td>2</td><td rowspan="3">轻缺</td></tr>
<tr><td rowspan="2">暗点</td><td>2 连续亮点</td><td>1</td></tr>
<tr><td>单一点</td><td>5</td></tr>
<tr><td>POL 气泡、凹凸点</td><td>参照点状缺陷定义</td><td>2 连续暗点</td><td>1</td><td></td></tr>
<tr><td></td><td></td><td>D≤0.2</td><td>忽略不计</td><td></td></tr>
</table>

PRODUCT SPECIFICATION

		0.2＜D≤0.4	3	
		D＞0.4	0	
Mura	斑点、不均	ND 5% 不可见视为 OK		轻缺
电测 线状缺陷	 L：长度 W：宽度 线不良间距需≥10.0mm	尺寸	允许个数	轻缺
		W≤0.05	忽略不计	
		L≤5.0，0.05＜W≤0.10	3	
		W＞0.10	依点状缺陷判定	
外观 线状缺陷		尺寸	允许个数	
		W≤0.05	忽略不计	
		L≤10.0，0.05＜W≤0.10	3 个	
		W＞0.10	依点状缺陷判定	

9. PACKAGE DRAWING