

# INDUSTRIAL STRENGTH... Start Your Application From YOURITECH

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|                      |                                                                                     |
|----------------------|-------------------------------------------------------------------------------------|
| Project No.<br>项目编号  | ET050FH10-T                                                                         |
| Customer<br>客户名称     |                                                                                     |
| Module No.<br>客户型号   |                                                                                     |
| Product type<br>产品内容 | <b>Standard LCD Module</b><br><b>TFT: 1080*RGBx1920Dots</b><br><b>4.97" TFT LCD</b> |

## 客户确认Customer Approval

|                          |  |
|--------------------------|--|
| 项目负责人Project Manager     |  |
| 品质主管Director of Quality  |  |
| 采购工程师Purchasing Engineer |  |

| PREPARED BY | CHECKED BY | APPROVED BY |
|-------------|------------|-------------|
|             |            |             |
|             |            |             |



## 1. Introduction

### 1.1 Scope of application

This specification applies to the LCD module that is supplied by YOURITECH E echnology CO., LTD.

LCD specification: Dots 1080xRGBx1920.

As to basic specification of the driver IC, refer to the IC (Himax:HX8399-C) specification and data book.

All material & processing of the LCD module should be Lead Free.

### 1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;

IPS Type LCD

1080 dot-segment and 1920 dot-common outputs;

16.7M Color can be selected by software;

White LED back light;

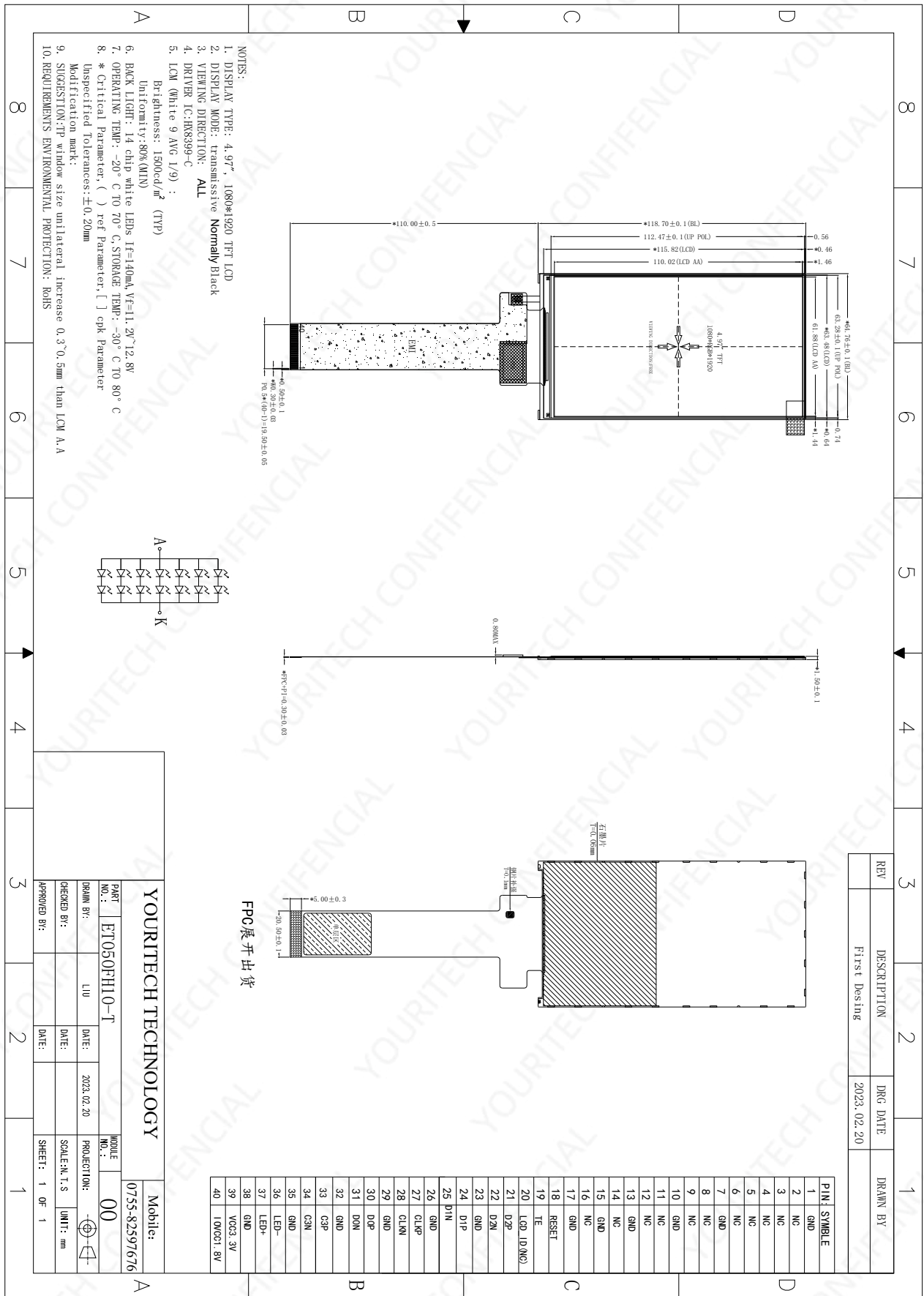
4lane MIPI interface



## 2. LCM General specification

| ITEM              | Standard value                | Unit |
|-------------------|-------------------------------|------|
| LCD Type          | Normally black                | --   |
| Drive element     | TFT active matrix             | --   |
| Number of pixels  | 1080*3RGB(H)X1920(V)          | Dots |
| Pixel arrangement | RGB stripe                    | --   |
| Pixel Pitch (H*V) | 57.3 (H) x57.3 (V)            | um   |
| Active area(H*V)  | 61.88(H) x 110.02(V)          | mm   |
| Viewing direction | ALL O'CLOCK                   | --   |
| TFT Driver IC     | HX8399-C                      | --   |
| TFT interface     | 4lane MIPI Interface          | --   |
| Approx. Weight    | TBD                           | g    |
| LCM Size(W*H*T)   | 64.76(W) x 118.70(H) x1.50(T) | mm   |
| Touch structure   | --                            | --   |
| Touch Driver IC   | --                            | --   |
| Touch Interface   | --                            | --   |





### 3.Absolute Maximum Rating

| Characteristics           | Symbol           | Min. | Max. | Unit |
|---------------------------|------------------|------|------|------|
| LCM Operating Temperature | T <sub>OPR</sub> | -20  | +70  | °C   |
| LCM Storage Temperature   | T <sub>STG</sub> | -30  | +80  | °C   |
| Humidity                  | RH               | --   | 90   | %    |

### 4.Electrical Characteristics

#### 4.1 TFT DC Characteristics

| Characteristics           | Symbol | Min. | Typ. | Max. | Unit | Note |
|---------------------------|--------|------|------|------|------|------|
| Supply Voltage for I/O    | VDDIO  | 1.65 | 1.8  | 3.3  | V    | --   |
| Supply Voltage for(DC/DC) | VDD    | 2.5  | 3.3  | 3.6  | V    | --   |

#### 4.2 Back-Light Unit Characeristics

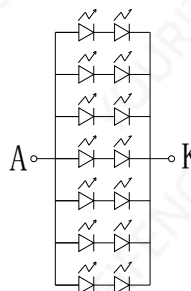
The back-light system is an edge-lighting type with 14 white LEDs. The characteristics of the back-light are shown in the following tables.

| Characteristics     | Symbol         | Min. | Type   | Max. | Unit              | Notes  |
|---------------------|----------------|------|--------|------|-------------------|--------|
| Forward Voltage     | V <sub>F</sub> | 11.2 | --     | 12.8 | V                 | --     |
| Forward current     | I <sub>F</sub> | --   | 140    | --   | mA                | --     |
| Luminance(With LCD) | L <sub>v</sub> | --   | 1500   | --   | cd/m <sup>2</sup> | --     |
| LED life time       | N/A            | --   | 20,000 | --   | Hr                | Note 1 |

Note:

- (1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I<sub>L</sub>=20mA/LED. The LED life time could be decreased if operating I<sub>L</sub> is larger than 25mA/LED.

Backlight circuit diagram shown in below:



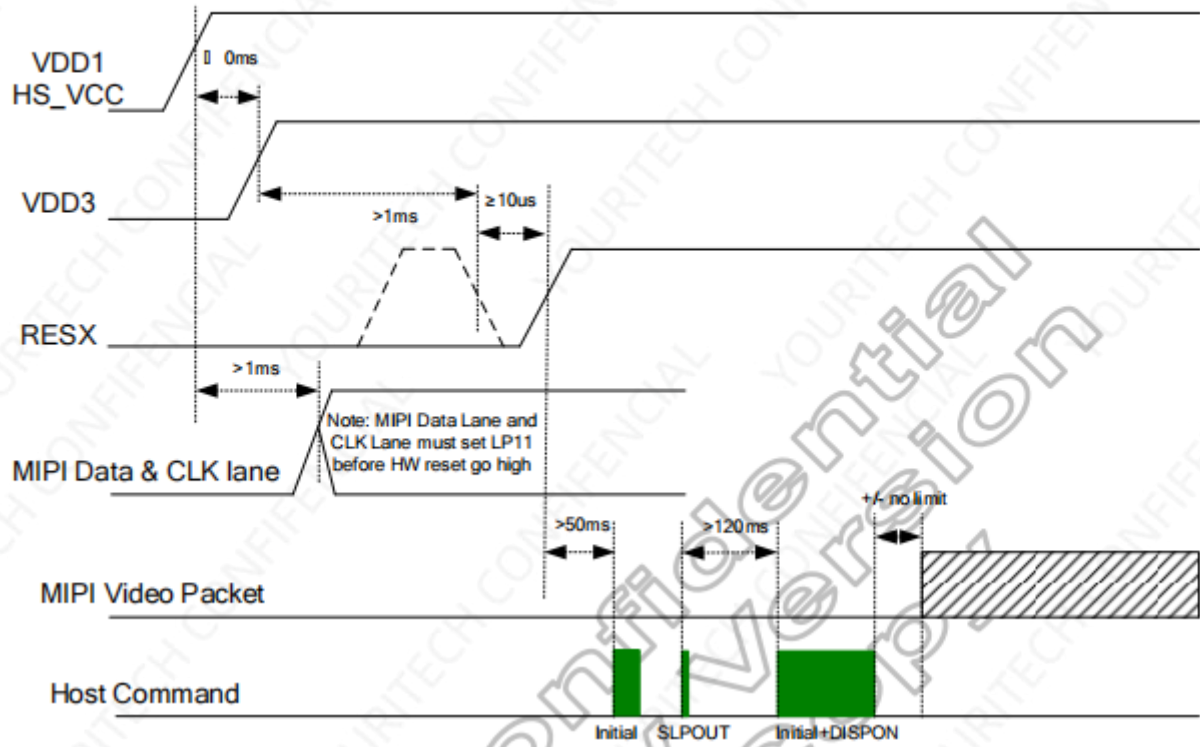
## 5. Module Function Description

| Pin No | Symbol     | Description                                                      |
|--------|------------|------------------------------------------------------------------|
| 1      | GND        | Power Ground                                                     |
| 2-6    | NC         | NC                                                               |
| 7      | GND        | Power Ground                                                     |
| 8-9    | NC         | NC                                                               |
| 10     | GND        | Power Ground                                                     |
| 11-12  | NC         | NC                                                               |
| 13     | GND        | Power Ground                                                     |
| 14     | NC         | NC                                                               |
| 15     | GND        | Power Ground                                                     |
| 16     | NC         | NC                                                               |
| 17     | GND        | Power Ground                                                     |
| 18     | RESET      | Reset signal input terminal. Active at 'L' .                     |
| 19     | TE         | Tearing effect signal is used to synchronize MCU to frame memory |
| 20     | LED-ID(NC) | NC                                                               |
| 21     | D2P        | High speed interface data differential signal input/output pins  |
| 22     | D2N        | High speed interface data differential signal input/output pins  |
| 23     | GND        | Power Ground                                                     |
| 24     | D1P        | High speed interface data differential signal input/output pins  |
| 25     | D1N        | High speed interface data differential signal input/output pins  |
| 26     | GND        | Power Ground                                                     |
| 27     | CLKP       | High speed interface clock differential signal input/output pins |
| 28     | CLKN       | High speed interface clock differential signal input/output pins |
| 29     | GND        | Power Ground                                                     |
| 30     | D0P        | High speed interface data differential signal input/output pins  |
| 31     | D0N        | High speed interface data differential signal input/output pins  |
| 32     | GND        | Power Ground                                                     |
| 33     | D3P        | High speed interface data differential signal input/output pins  |
| 34     | D3N        | High speed interface data differential signal input/output pins  |
| 35     | GND        | Power Ground                                                     |
| 36     | LEDK       | Power supply for backlight cathode input terminal.               |
| 37     | LEDA       | Power supply for backlight anode input terminal.                 |
| 38     | GND        | Power Ground                                                     |
| 39     | VCC 3.3V   | Power Supply For LCD.                                            |
| 40     | IOVCC 1.8V | Power Supply For I/O.                                            |

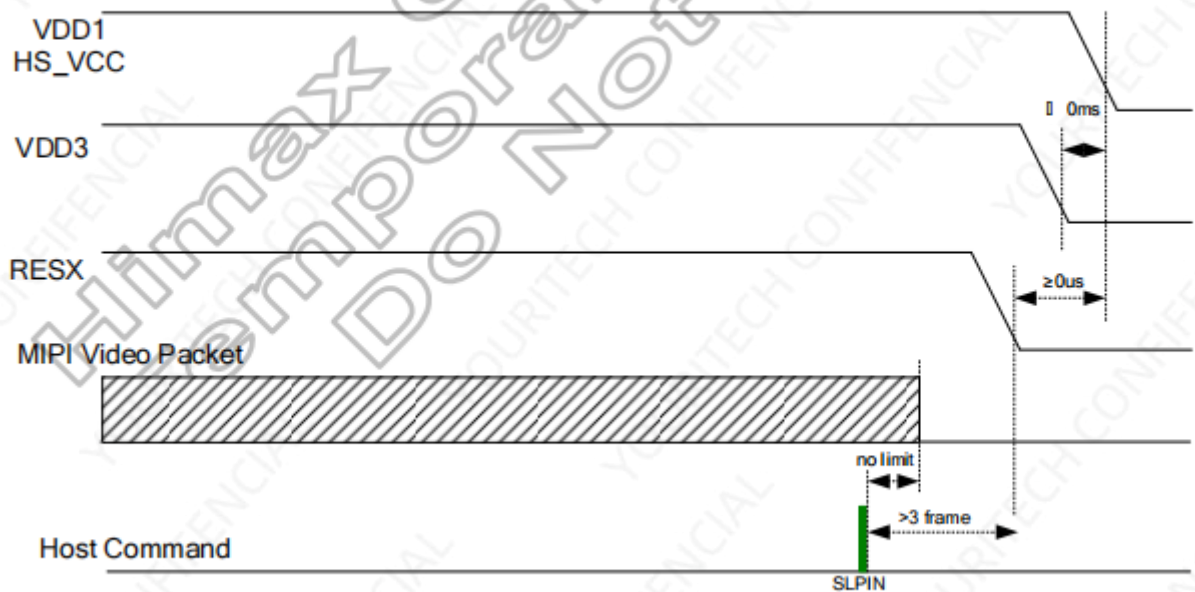


## 6. Timing Characteristics

**VDD3/VDD1 input power (PCCS[2:0]=000, 001, 101)**



**Figure 5.30: VDD3/VDD1 input power on sequence (PCCS[2:0]=000/001/101)**



**Figure 5.31: VDD3/VDD1 input power off sequence (PCCS[2:0] =000/001/101)**



## Timings for DSI video mode

### Vertical Timings

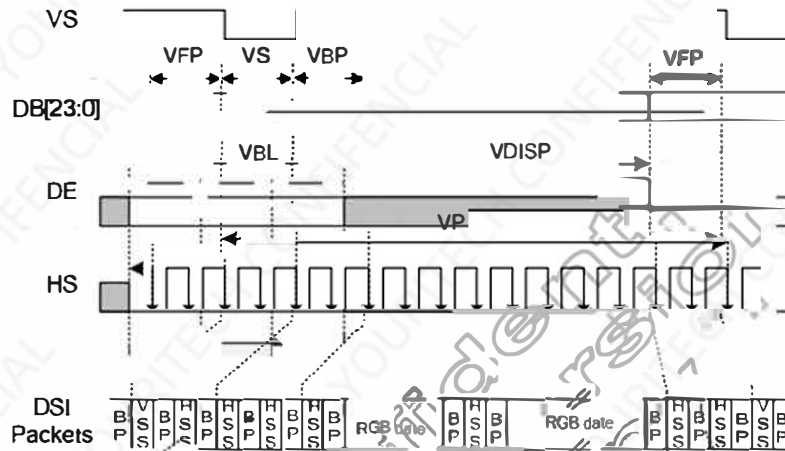


Figure 8.10: vertical timings for DSI I/F

Vertical Resolution=528+8xNL VSSA=0x, VDD1=0x, VDD2=0x, VDD3=0x

| Parameter                 | Symbol | Condition  | Spec.    |          |                     | Unit |
|---------------------------|--------|------------|----------|----------|---------------------|------|
|                           |        |            | Min.     | Typ.     | Max.                |      |
| Vertical cycle            | VR     |            | 534+8xNL |          |                     | Line |
| Vertical low pulse width  | VS     |            | 2        | 25°C     | Note <sup>(1)</sup> | Line |
| Vertical front porch      | VFP    |            | 2        |          |                     | Line |
| Vertical back porch       | VBP    |            | 2        |          | Note <sup>(1)</sup> | Line |
| Vertical data start point |        | VS+VBP     | 4        |          | Note <sup>(1)</sup> | Line |
| Vertical blanking period  | VBL    | VS+VBP+VFP | 6        |          |                     | Line |
| Vertical active area      |        | VDISP      |          | 528+8xNL |                     | Line |
| Vertical Refresh rate     | VRR    |            |          | -60      |                     | Hz   |

Note: (1) The VS and VBP pulse width are related to GSP and GCK timing. The GSP and GCK must be set at corresponding position for LCD normal display

Table 8.14: Vertical timings for DSI I/F

### Horizontal Timings

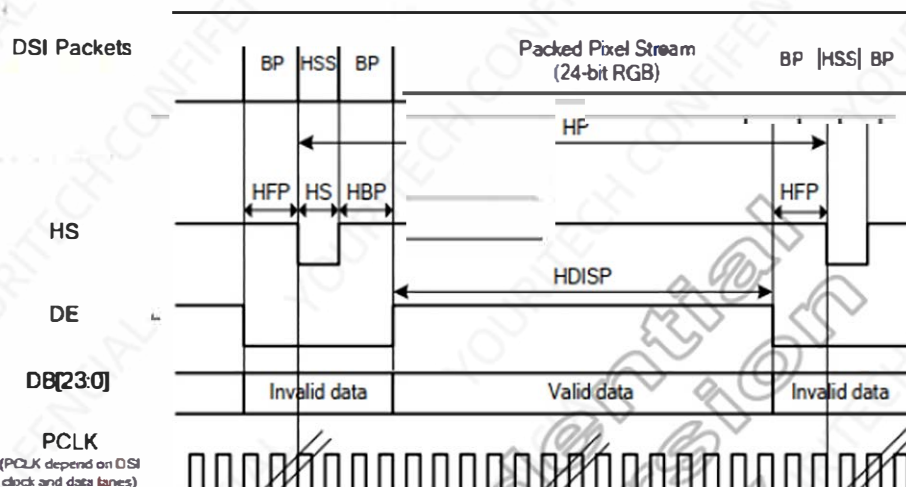


Figure 8.11: Horizontal timing for DSI video mode I/F



Horizontal Resolution=H\_RES(1200/1080/1024/960/900/800/720) (VSSA=0V, VDD1=1.8V, VDD3 = HS\_VCC =2.8V, T<sub>A</sub>=25°C)

| Parameter                   | Symbol | Condition  | Spec.    |       |      | Unit |
|-----------------------------|--------|------------|----------|-------|------|------|
|                             |        |            | Min.     | Typ.  | Max. |      |
| HS cycle                    | HP     | -          | H_RES+15 | -     | -    | DCK  |
| HS low pulse width          | HS     | -          | 5        | -     | -    | DCK  |
| Horizontal back porch       | HBP    | -          | 5        | -     | -    | DCK  |
| Horizontal front porch      | HFP    | -          | 5        | -     | -    | DCK  |
| Horizontal data start point | -      | HS+HBP     | 10       | -     | -    | DCK  |
| Horizontal blanking period  | HBLK   | HS+HBP+HFP | 15       | -     | -    | DCK  |
| Horizontal active area      | HDISP  | -          | -        | H_RES | -    | DCK  |

Table 8.15: Horizontal timings for DSI video mode I/F

### Reset input timing

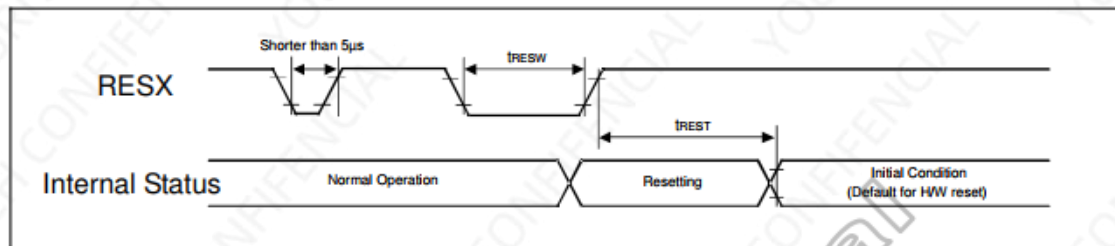


Figure 8.12: Reset input timing

| Symbol            | Parameter                            | Related pins | Spec. |      |      | Unit | Note |
|-------------------|--------------------------------------|--------------|-------|------|------|------|------|
|                   |                                      |              | Min.  | Typ. | Max. |      |      |
| t <sub>RESW</sub> | Reset low pulse width <sup>(1)</sup> | RESX         | 10    | -    | -    | µs   | -    |
| t <sub>REST</sub> | Reset complete time <sup>(2)</sup>   | -            | -     | -    | 50   | ms   | -    |

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

| RESX Pulse           | Action         |
|----------------------|----------------|
| Shorter than 5µs     | Reset Rejected |
| Longer than 10µs     | Reset          |
| Between 5µs and 10µs | Reset Start    |

(2) During Reset Complete Time, OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t<sub>REST</sub>) within 5ms after a rising edge of RESX.

(3) Spike Rejection also applies during a valid reset pulse as shown below:

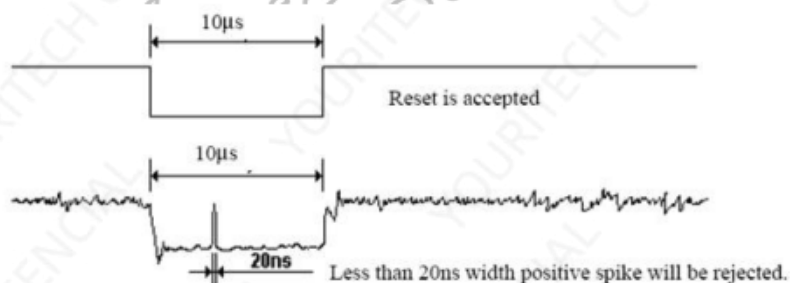


Table 8.16: Reset timing



## 7. Optical Characteristics

| Parameter           |            | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
|---------------------|------------|--------|-----------|------|------|------|------|--------|
| Viewing Angle Range | Horizontal | Θ3     | CR> 10    | 70   | 80   | -    | Deg. | Note1  |
|                     |            | Θ9     |           | 70   | 80   | -    | Deg. |        |
|                     | Vertical   | Θ12    |           | 70   | 80   | -    | Deg. |        |
|                     |            | Θ6     |           | 70   | 80   | -    | Deg. |        |
| Contrast ratio      |            | CR     | Θ = 0°    | 1000 | 1500 | -    |      | Note2  |
| Transmittance       |            | Tr     |           | 3.6  | 4.3  |      | %    | Note3  |
| Color Gamut         |            | CG     | CIE1931   | 55   | 60   |      | %    | NTSC   |

| Parameter                           | Symbol      | Condition                          | Min.  | Typ.  | Max.  | Unit | Remark |
|-------------------------------------|-------------|------------------------------------|-------|-------|-------|------|--------|
| White Chromaticity                  | Wx          | $\Theta = 0^\circ$                 | 0.270 | 0.300 | 0.330 |      | Note 4 |
|                                     | Wy          |                                    | 0.308 | 0.338 | 0.368 |      |        |
| Response Time<br>(Rising + Falling) | $T_r + T_f$ | Ta= 25°<br>C<br>$\Theta = 0^\circ$ | -     | -     | 35    | ms   | Note 5 |

**Note:**

- 1.Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o' clock direction and the vertical or 6, 12 o' clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).
- 2.Contrast measurements shall be made at viewing angle of  $\Theta= 0$  and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGUR 1)  
Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

- 3.Transmittance is the Value without CG, APF and Haze. ESR Reflector and Composite Prism backlight unit shall be used for Transmittance measurements. Transmittance value shall be tested by PR730.
- 4.The color chromaticity coordinates specified in the above table shall be calculated from the spectral data measured with bare CF Glass at C standard light source. Measurements shall be made at the center of the CF Glass.
- 5.The electro-optical response time measurements shall be made as FIGURE 2 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is  $T_r$ , and 90% to 10% is  $T_f$ .



## 8. Reliability Test Item

| No. | Test Item                              | Test Condition                                          | Notes                                                                                                                                                                                                                                   |
|-----|----------------------------------------|---------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | High Temp. Storage                     | +80°C / 96H                                             | 1. Functional test is OK.<br>Missing Segment, short,<br>unclear segment<br>non-display, display abnormally<br>and liquid crystal leakage<br>un-allowed.<br>2. No low<br>temperature bubbles, end seal<br>loose and fall, frame rainbow. |
| 2   | Low Temp. Storage                      | -30°C / 96H                                             |                                                                                                                                                                                                                                         |
| 3   | High Temp. Operating                   | +70°C / 96H                                             |                                                                                                                                                                                                                                         |
| 4   | Low Temp. Operating                    | -20°C / 96H                                             |                                                                                                                                                                                                                                         |
| 5   | High Temperature<br>/ Humidity storage | 50°C x 90%RH / 96H                                      |                                                                                                                                                                                                                                         |
| 6   | Thermal and cold shock                 | Static state, -20°C (30min) ~60°C<br>(30min), 10 cycles |                                                                                                                                                                                                                                         |

## 9. Packing Method----TBD

- END -

