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MODEL NO : ET050FW03-TT

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-03-18

□Preliminary Specification

■Final Product Specification

Customer :

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 480xRGBx854
As to basic specification of the driver IC, refer to the IC (ST7701S) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

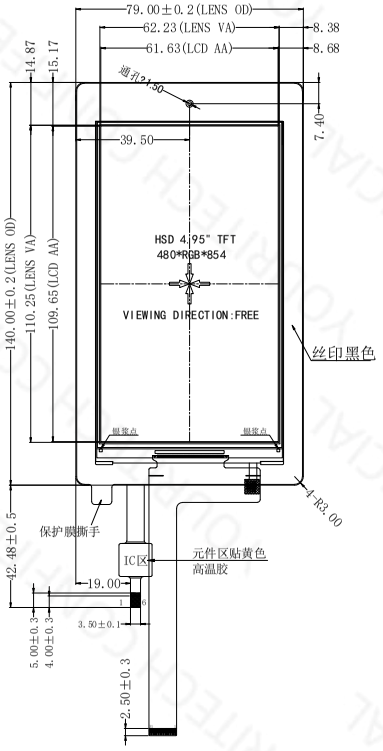
Structure: TFT PANNEL+IC +FPC1+BL+CTP;
ALL Viewing Type LCD
480 dot-segment and 854 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
2Lane MIPI interface

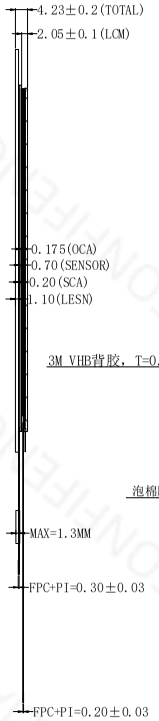
1.3 Applications:

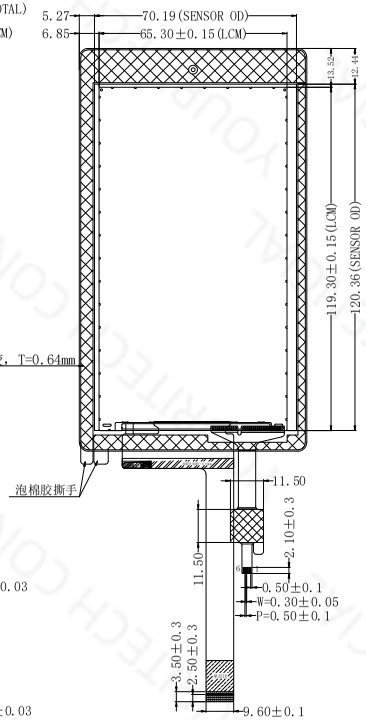
2. LCM General specification

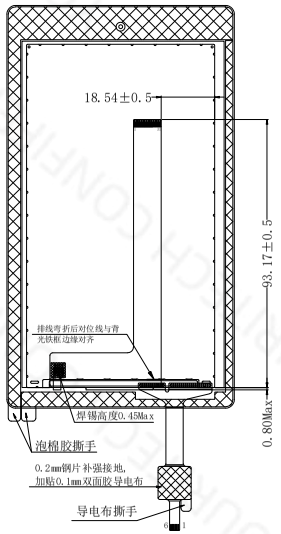
ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	480*3RGB(H)X854(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.1284 (H) x 0.1284 (V)	mm
Active area	61.63(H) x 109.65(V)	mm
Viewing direction	ALL Viewing	--
TFT Driver IC	ST7701S	--
TFT interface	2lane MIPI Interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	65.30(W) ×119.30(H) ×2.05(T)	mm
LCM+CTP Size(W*H*T)	79.00(W) ×140.00(H) ×4.23(T)	mm
Approx. Weight	TBD	g
Touch structure	G+G	--
Touch Driver IC	GT911	--
Touch Interface	I2C	--

REV	DESCRIPTION	DRG DATE	DRAWN BY
	First Desing	2022.03.18	







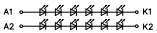


FPC弯折示意图
LCM FPC弯折出货
TP FPC 展开出货

1	LEDA
2	NC
3	LEDK
4	TP_2.8V(NC)
5	TP_SCL(NC)
6	TP_SDA(NC)
7	TP_INT(NC)
8	TP_RST(NC)
9	GND
10	NC
11	VCI2.8V
12	IOVCC1.8V
13	RESET
14	FMARK
15	LCM_ID
16	TDP3
17	TDN3
18	GND
19	TDP2
20	TDN2
21	GND
22	TDP1
23	TDN1
24	GND
25	TDP0
26	TDN0
27	GND
28	TCP
29	TCN
30	GND
31	NC

技术参数：
1. 结构：G+G
IC型号：GT911
2. 工作电压：3.3V
3. 透光率：≥85%
4. 表面硬度：6H
5. 工作环境：-10℃~+60℃，湿度20%~90%
6. 储存环境：-20℃~+70℃，湿度20%~90%
7. 未注尺寸公差按±0.2mm

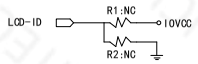
NOTES:
1. DISPLAY TYPE: 4.95", 480*854 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL
4. DRIVER IC:ST7701
5. LCM (White 9 AVG 1/9) :
   Brightness: 350cd/m² (TYP)
   Uniformity:80%(MIN)
6. BACK LIGHT: 12 chip white LEDs If=40mA,Vf=18V-19.2V
7. OPERATING TEMP: -10° C TO 60° C,STORAGE TEMP: -20° C TO 70° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS



12颗LED灯 Vled=19.2V ILed=20*2mA

LED CIRCUIT: B/L CIRCUIT DIAGRAM

PIN	NAME
1	VDD 3.3V
2	SCL 3.3V
3	SDA 3.3V
4	GND
5	RST
6	INT



深圳市优瑞泰克科技有限公司

PART NO.:	ET050FW03-TT			MODULE NO.:	00
DRAWN BY:	LYH	DATE:		PROJECTION:	
CHECKED BY:		DATE:		SCALE:N.T.S	UNIT: mm
APPROVED BY:		DATE:		SHEET: 1 OF 1	

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+60	°C
LCM Storage Temperature	T_{STG}	-30	+70	°C
TP Operating Temperature & Humidity(20%～90%RH)	T_{OPR}	-20	+60	°C
TP SStorage Temperature & Humidity(20%～90%RH)	T_{STG}	-30	+70	°C
Humidity	RH	-	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.5	2.8	3.6	V
Supply Voltage for(DC/DC)	AVDD				V
Supply Voltage for(DC/DC)	AVEE				V

4.2 Back-Light Unit Characeristics

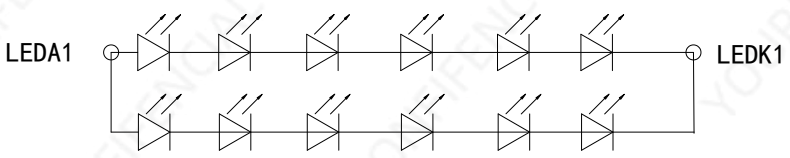
The back-light system is an edge-lighting type with 12 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	18		19.2	V	-
Forward current	I_F	--	40	-	mA	-
Luminance(With LCD)	Lv		350	--	cd/m^2	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

(2) Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	LCM Functional	Notes
1	LEDA	Power supply for backlight anode input terminal.	
2	NC	NC	
3	LEDK	Power supply for backlight cathode input terminal.	
4	TP_2.8V(NC)	NC	
5	TP_SCL(NC)	NC	
6	TP_SDA(NC)	NC	
7	TP_INT(NC)	NC	
8	TP_RST(NC)	NC	
9	GND	Power Ground	
10	NC	NC	
11	VCI2.8V	Power supply : 2.5V ~ 3.3V	
12	IOVCC1.8V	I/O Voltage (VDDI to DGND): 1.65V ~ 3.3V	
13	RESET	Reset signal input terminal. Active at 'L'.	
14	TE	Tearing effect output pin to synchronies MCU to frame rate.	
15	LCM_ID	LCM_ID: R1=IOVCC(NC)、R0=GND(NC)	
16	MIPI_3P	NC	
17	MIPI_3N	NC	
18	GND	Power Ground	
19	MIPI_2P	NC	
20	MIPI_2N	NC	
21	GND	Power Ground	
22	MIPI_1P	MIPI-DSI clock data Lane 1 pegative-end input/output pin.	
23	MIPI_1N	MIPI-DSI clock data Lane 1 nositive-end input/output pin.	
24	GND	Power Ground	
25	MIPI_0P	MIPI-DSI clock data Lane 0 pegative-end input/output pin.	
26	MIPI_0N	MIPI-DSI clock data Lane 0 nositive-end input/output pin.	

27	GND	Power Ground	
28	MIPI_CKP	MIPI-DSI clock data Lane pegative-end input pin.	
29	MIPI_CKN	MIPI-DSI clock data Lane nositive-end input pin.	
30	GND	Power Ground	
31	NC	NC	

Pin No.	Symbol	CTP Functional	Notes
1	CTP_VDD 3.3V	Touch panel Power supply 2.8~3.3V	
2	CTP_SCL 3.3V	Touch panel I2C clock	
3	CTP_SDA 3.3V	Touch panel I2C data	
4	GND	Power Ground	
5	CTP_RST 3.3V	Touch panel reset	
6	CTP_INT 3.3V	Touch panel interrupt output	

6. Timing Characteristics

POWER ON/OFF SEQUENCE

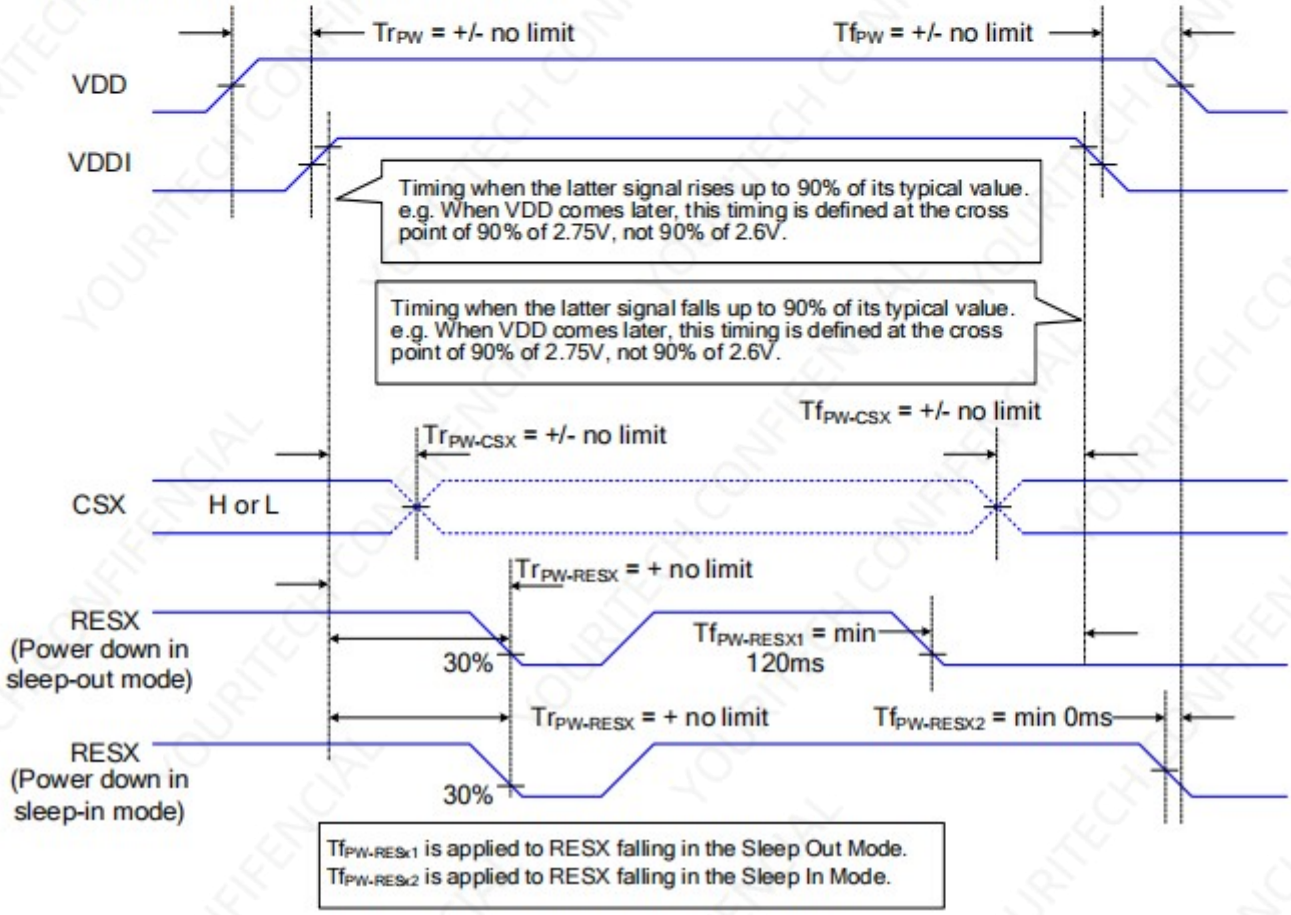
VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released.

CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

Notes:

1. There will be no damage to the ST7701S if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

The power on/off sequence is illustrated below



DSI-MIPI Interface Timing Characteristics of IC

Normal Write Mode (VCC = IOVCC=2.5~3.3V)

High Speed Mode

DSI clock channel timing

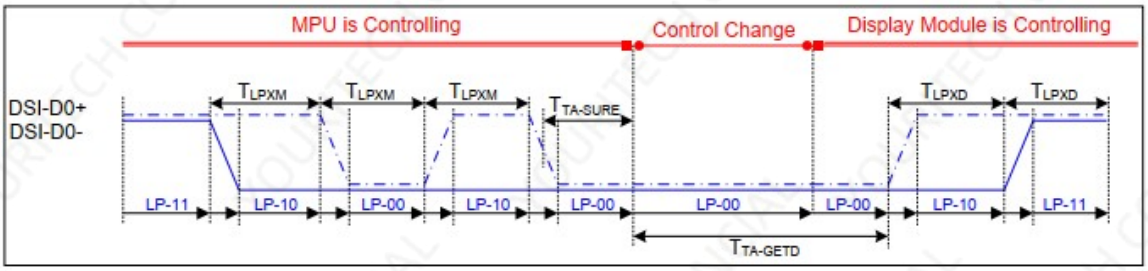
Rising and falling time on clock and data channel

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

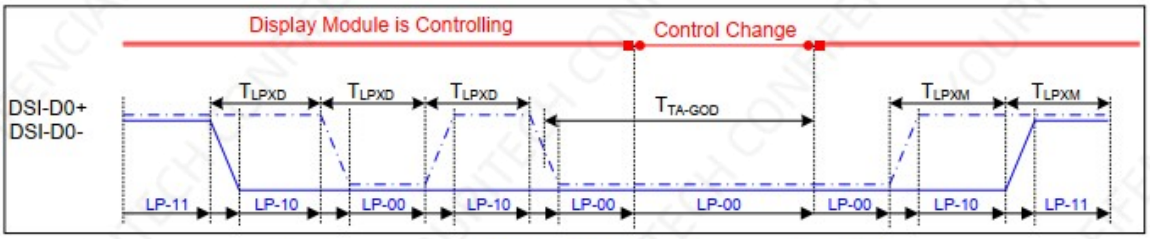
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Mipi Interface- High Speed Mode Timing Characteristics

Lowe Power Mode



Bus Turnaround (BTA) from display module to MPU Timing



Bus Turnaround (BTA) from MPU to display module Timing

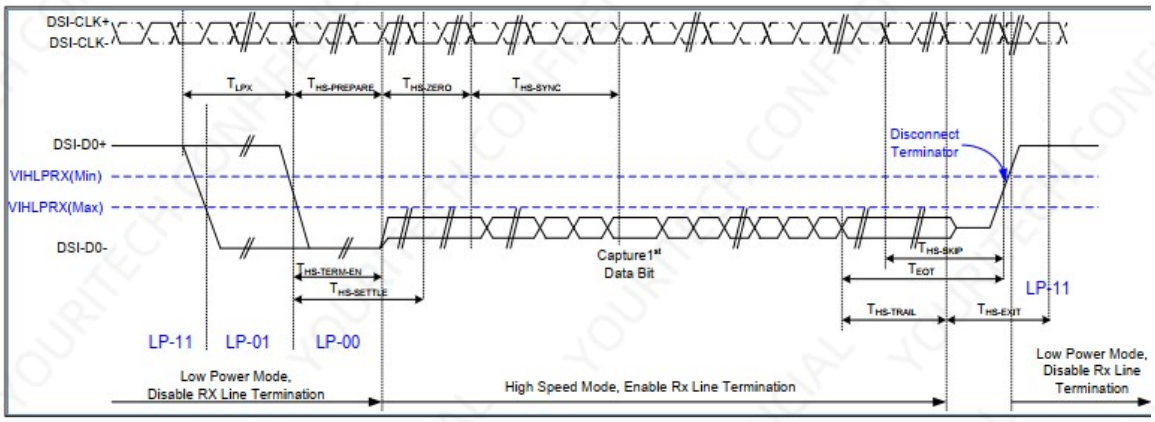
VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

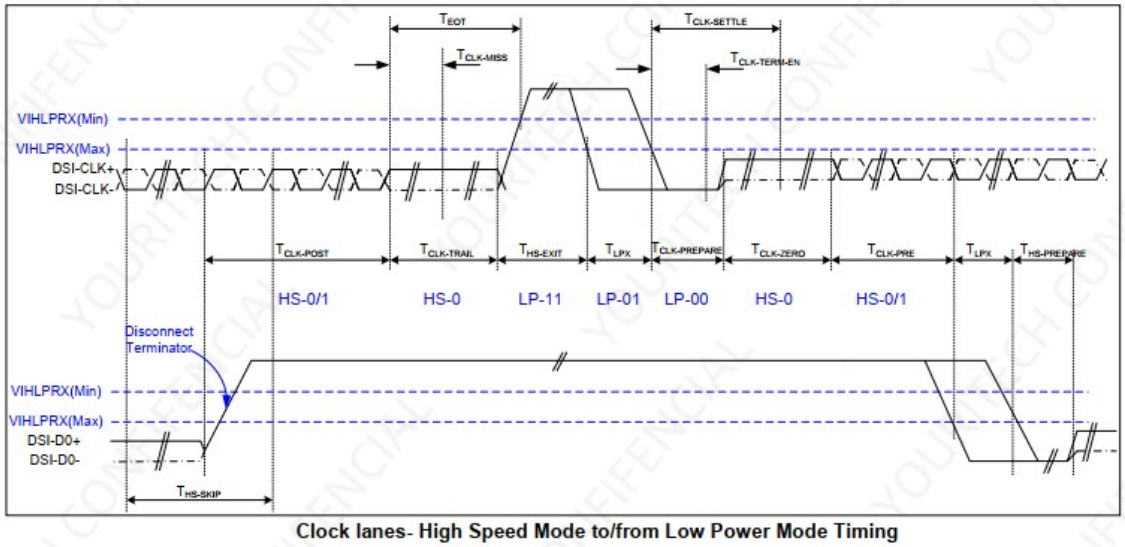
Mipi Interface Low Power Mode Timing Characteristics

DSI Bursts Mode

DSI Bursts Mode



Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

Reset Description:

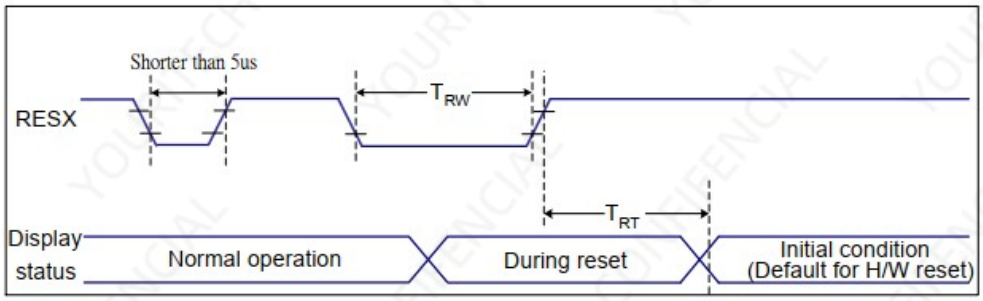


Figure 9 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

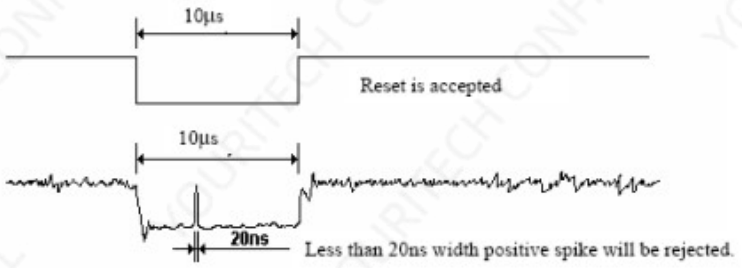
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Optical Specification

908OI908		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T (%)	Θ=0 Normal viewing angle	—	4.47	—	%	Measuring with Polarizer, Reference Only
Transmittance (without Polarizer)		T (%)		—	14.2	—	%	
Contrast		CR		640	800	—	—	(1)(2)
Response time	Rising	T_R		—	16	21	msec	(1)(3)
	Falling	T_F		—	19	24		
Color gamut	(%)			—	70	—	%	C-light
Color chromaticity (CIE1931)	White	W_x		-0.02	0.305	+0.02	—	(1)(4) CF glass
		W_y			0.340			
	Red	R_x			0.665		—	
		R_Y			0.327		—	
	Green	G_x			0.276		—	
		G_Y			0.594			
	Blue	B_x			0.134		—	
		B_Y			0.118			
Viewing angle	Hor.	Θ_L	CR>10	—	80	—	—	(1)(4) Measuring with Polarizer, Reference Only
		Θ_R		—	80	—		
	Ver.	Θ_U		—	80	—		
		Θ_D		—	80	—		
Optima View Direction		Free						(5)

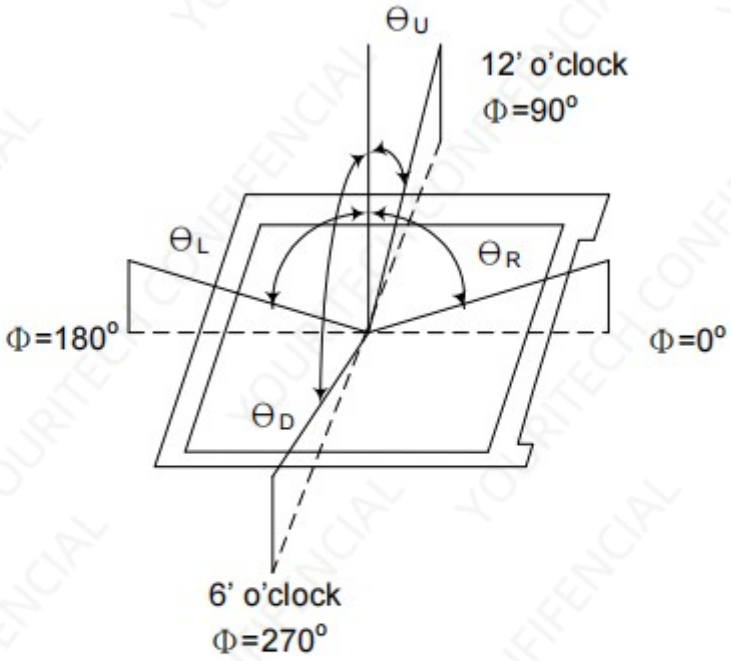
Measuring Condition

- Measuring surrounding：dark room
- Ambient temperature：25±2°C
- 15min. warm-up time.

Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

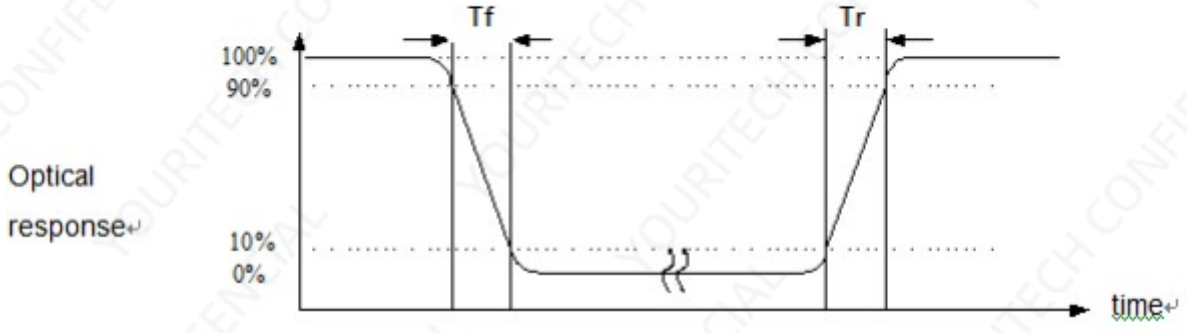
Note (1) Definition of Viewing Angle:



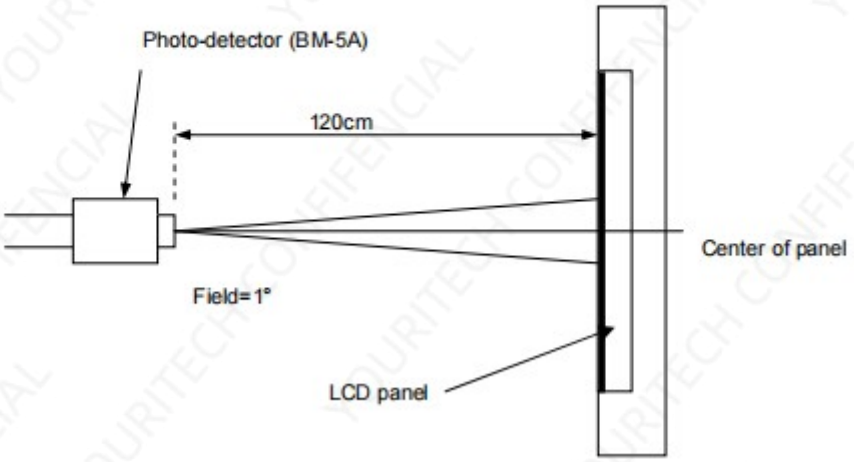
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

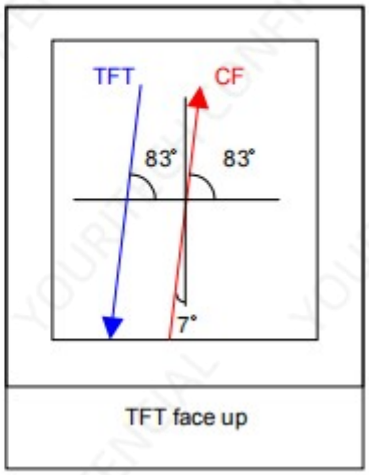
Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+70°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+60°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~60℃（30min），50 cycles	

9. Packing Method----TBD

- END -