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Mechanical design



MODEL NO : ET050HD01-KMODEL VERSION: 01SPEC VERSION : 1.0ISSUED DATE: 2018-01-05

- ☒ Preliminary Specification
☐ Final Product Specification

Customer : _____

Approved by	Notes

Table of Contents

Record of Revision.....	3
1 General Specifications	4
2 Input/Output Terminals	5
3 Absolute Maximum Ratings	6
4 Electrical Characteristics.....	7
5 Timing Chart.....	8
6 Optical Characteristics	12
7 Environmental / Reliability Test	15
9 Packing Drawing	17
10 Precautions for Use of LCD Modules	17

Record of Revision

[illegible]

1 General Specifications

Feature		Spec
Display Spec.	Size	5 inch
	Resolution	720(RGB) X 1280
	Technology Type	a-Si
	Pixel Configuration	RGB Vertical Stripe
	Pixel pitch(mm)	0.08625(H)*0.08625(V)
	Display Mode	Normally Black, Transmissive
	Viewing Direction	ALL
Mechanical Characteristics	MODEL (W x H x D) (mm)	67.56*122.35*2.6
	LCD Active Area(mm)	62.1(H)*110.4(V)
	With /Without TSP	Without CTP
	Weight (g)	TBD
Electrical Characteristics	LCD Interface	MIPI 4 lane
	Driver IC	ILI9881C
	Color Depth	16.7M

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180 degree shift.

Note 2: Requirements on Environmental Protection: Q/S0002

Note 3: LCM weight tolerance: $\pm 5\%$

2 Input/Output Terminals

2.1 LCM Interface

NO.	SYMBOL	DISCRIPTION	I/O
1	NC		
2	LEDK	Cathodepinofbacklight.	P
3	NC		
4	LEDA	Anodepinofbacklight.	P
5	NC		
6	GND	Ground.	P
7	MIPI_D0N	- MIPI DSI differential data pair. (Data lane 0) Leave it open or fix to GND level when not in use.	I
8	MIPI_D0P		I
9	GND	Ground.	P
10	MIPI_D1N	- MIPI DSI differential data pair. (Data lane 1) Leave it open or fix to GND level when not in use.	I
11	MIPI_D1P		I
12	GND	Ground.	P
13	MIPI_CLN	- MIPI DSI differential clock pair Leave it open or fix to GND level when not in use.	I
14	MIPI_CLP		I
15	GND	Ground.	P
16	MIPI_D2N	- MIPI DSI differential data pair. (Data lane 2) Leave it open or fix to GND level when not in use.	I
17	MIPI_D2P		I
18	GND	Ground.	P
19	MIPI_D3N	- MIPI DSI differential data pair. (Data lane 3) Leave it open or fix to GND level when not in use.	I
20	MIPI_D3P		I
21	GND	Ground.	P
22	GND	Ground.	P
23	NC		
24	GND	Ground.	P

25	TE	- Tearing effect output pin. Leave the pin open when not in use.	O
26	RESET	- The external reset input Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power. Fix to IOVCC level when not in use.	I
27	IOVCC	- Power supply for internal logic regulator. Connect to an external power supply of 1.65V to 3.3V	P
28	VCI	- Power supply for analog circuits. Connect to an external power supply of 2.5V to 3.3V	P
29	GND	Ground.	P
30	GND	Ground.	P

3 Absolute Maximum Ratings

GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Power Voltage	VDD	-0.3	5	V	Note1
Operating Temperature	Top	-20	70	°C	
Storage Temperature	Tst	-30	80	°C	

Table 3 Absolute Maximum Ratings

Note 1: Temperature and relative humidity range are shown in the figure below.

4 Electrical Characteristics

4.1 Driving TFT LCD Panel

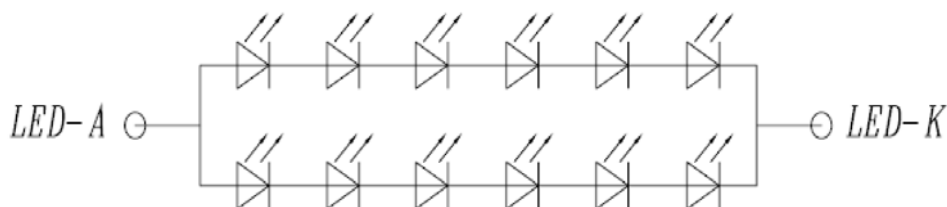
Item	Symbol	Min.	Typ	Max.	Unit
Supply power1	VIO28	2.5	2.8	3.6	V
Supply power2	VIO18	1.65	1.8	3.6	V
Logic High level input voltage	VIH	0.7* VIO18	-	VIO18	V
Logic Low level input voltage	VIL	-0.3	-	0.3* VIO18	V
Logic High level output voltage	VOH	0.8* VIO18	-	VIO18	V
Logic Low level output voltage	VOL	0	-	0.2* VIO18	V

4.2 Backlight Unit

The backlight system is an edge-lighting type with 12 LED. The characteristics of the LED are shown in the following tables.

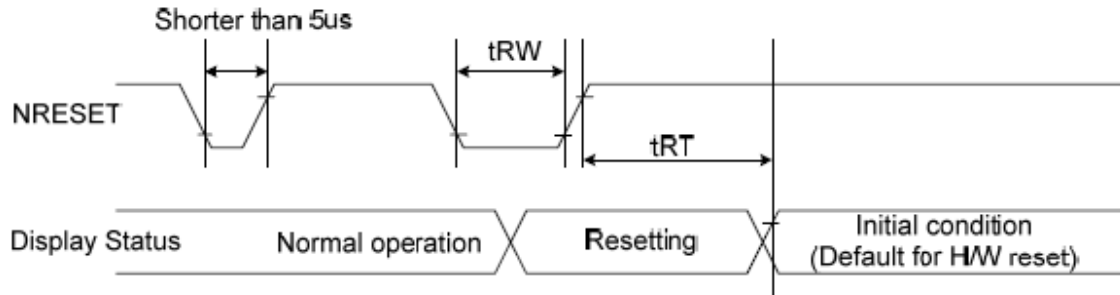
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Backlight forward voltage	V_F	-	19.2	-	V	12 LEDs
Backlight forward current	I_F	--	40	--	mA	
LED life time	--	50000	--	--	Hrs	

Note 1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: $T_a=25\pm3\text{ }^{\circ}\text{C}$, typical IL value indicated in the above table and the $f_L=50\text{kHz}$ until the brightness becomes less than 50%.



5 Timing Chart

5.1 Reset Timing



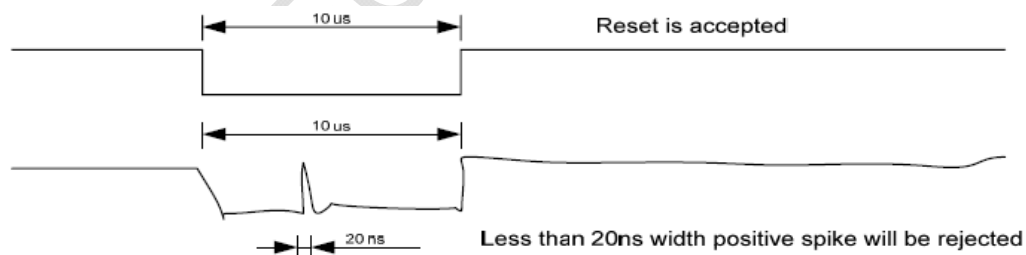
Signal	Symbol	Parameter	Min	Max	Unit
RESX	t_{RW}	Reset pulse duration	10		us
	t_{RT}	Reset cancel		5(note 1,5)	ms
				120 (note 1,6,7)	ms

Note : 1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

2. During Reset Complete Time, OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 50ms after a rising edge of RESX.

3. Spike Rejection also applies during a valid reset pulse as shown below:



5.2 AC Characteristics

5.51 High Speed Mode-Clock Channel Timing

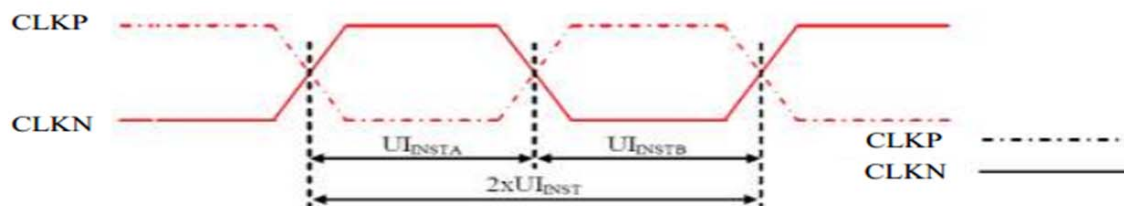


Figure 116: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	Note 2	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	Note 2	12.5	ns

Notes:1. Define the minimum value,see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

5.52 High Speed Mode-Data Clock Channel Timing

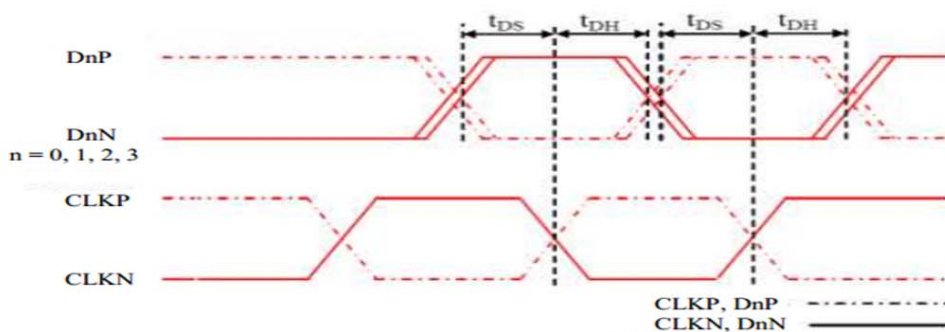
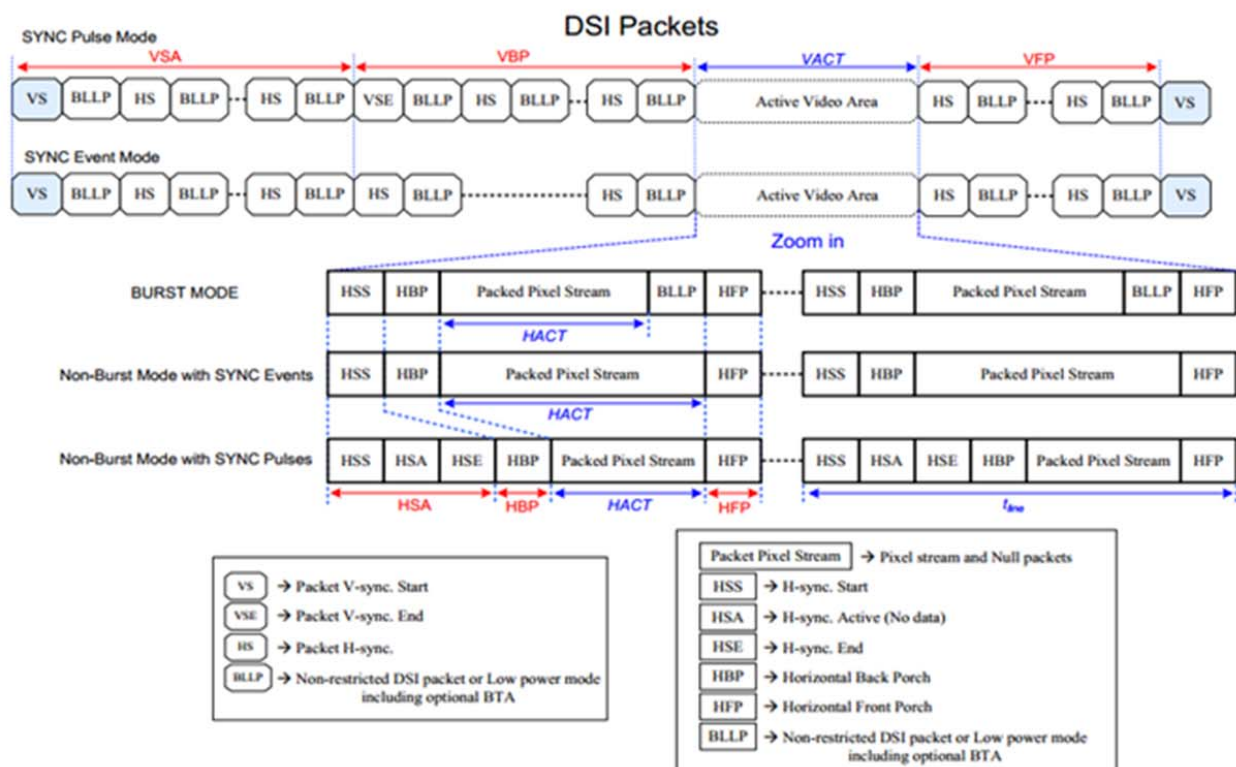


Figure: DSI Data to Clock Channel Timings

Table: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N, n=0 and 1	t_{DS}	Data to Clock Setup time	$0.15xUI$	-
	t_{DH}	Clock to Data Hold Time	$0.15xUI$	-



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	-	-	Line
Vertical Back Porch	VBP	14 (Note 6)	-	-	Line
Vertical Front Porch	VFP	8 (Note 6)	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR _{bps}	385		Note 5	Mbps/lane

1 UI=1/Bit rate

$HSA(pixel) = (tHSA \times \text{lane number}) / (UI \times \text{pixel format})$

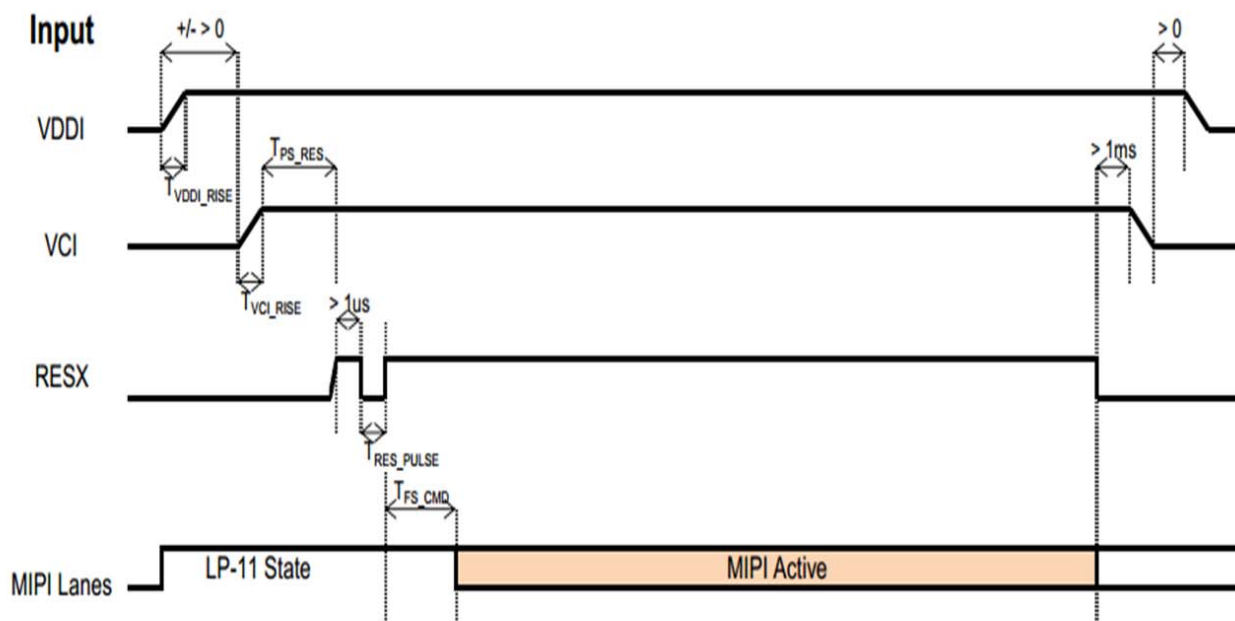
$HBP(pixel) = (tHBP \times \text{lane number}) / (UI \times \text{pixel format})$

$HFP(pixel) = (tHFP \times \text{lane number}) / (UI \times \text{pixel format})$

$$\text{Frame Rate} = \frac{BR_{bps} \times \text{Lane}_{num}}{(VACT + VSA + VBP + VFP) \times (HACT + HSA + HBP + HFP) \times \text{Pixel Format}}$$

Example : BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, Lane_{num}=4(lane), Pixel Format=24(bit).

5.3 Power Sequence



Note: SLPOUT CMD can before or after Initial code, but after SLPOUT CMD must wait at least 120ms.

Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	20	-	-	us
	Case A: VCI Rise time	200			
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

6 Optical Characteristics

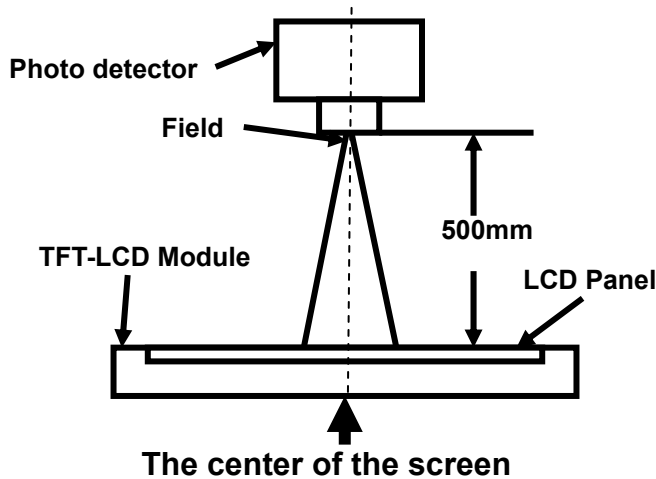
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	-	85	-	Degree	Note2,3
		θB		-	85	-		
		θL		-	85	-		
		θR		-	85	-		
Contrast Ratio		CR	θ=0°	-	800	-		Note 3
Response Time		T _{ON}	25℃	-	35	-	ms	Note 4
		T _{OFF}						
Chromaticity	White	x	Backlight is on	0.26	0.31	0.36		Note 1,5
		y		0.28	0.33	0.38		
	Red	x						Note 1,5
		y						
	Green	x						Note 1,5
		y						
	Blue	x						Note 1,5
		y						
Uniformity		U		75	80	--	%	Note 6
Luminance		L		450	500	-	cd/m ²	Note 7

Test Conditions:

1. $I_F = 20$ mA, and the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

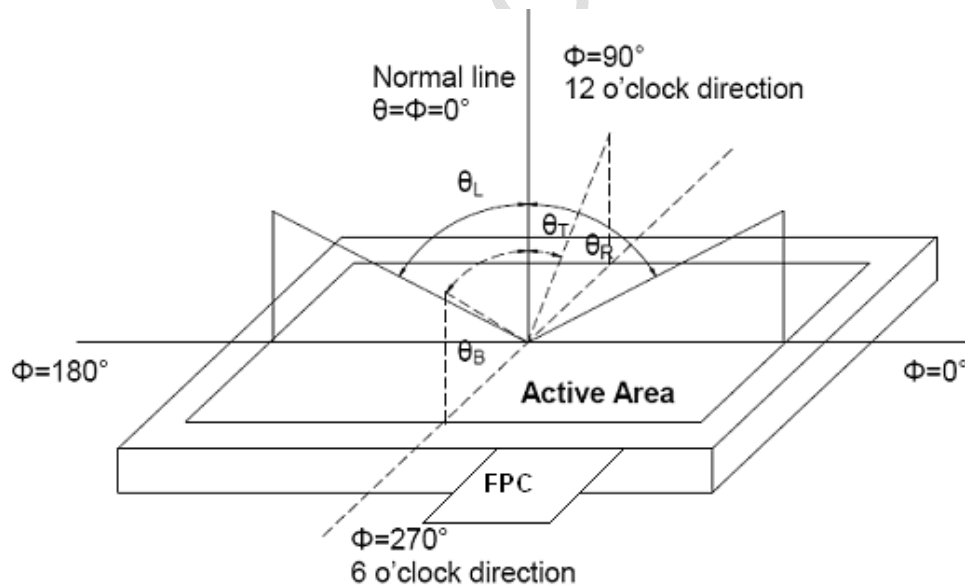
Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD.



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

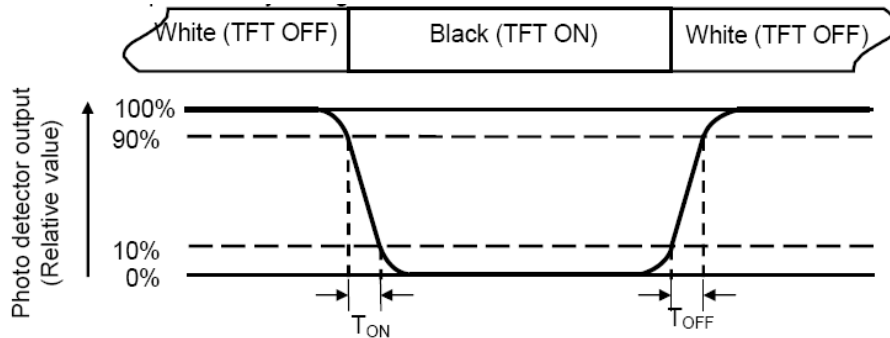
"White state ": The state is that the LCD should drive by V_{white} .

"Black state": The state is that the LCD should drive by V_{black} .

V_{white} : To be determined V_{black} : To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

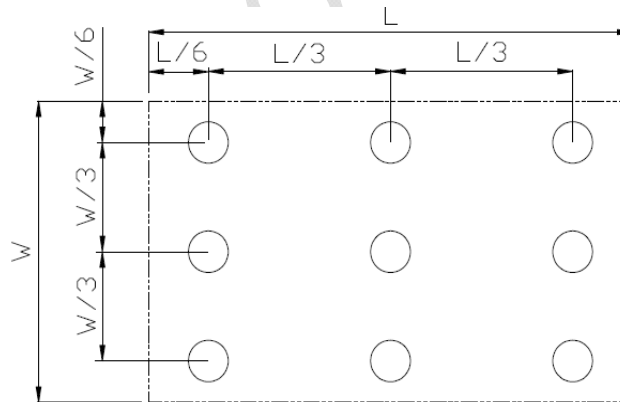
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity (U)} = L_{\min} / L_{\max}$$

L-----Active area length W----- Active area width



$L_{\max}$: The measured Maximum luminance of all measurement position.

$L_{\min}$: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

7 Environmental / Reliability Test

No	Test Item	Condition	Remarks
1	High Temperature Operation	70℃, 120Hours	IEC60068-2-1:2007 GB2423.2-2008
2	Low Temperature Operation	-20℃, 120Hours	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	80℃, 120Hours	IEC60068-2-1:2007 GB2423.2-2008
4	Low Temperature Storage	-30℃, 120Hours	IEC60068-2-1:2007 GB2423.1-2008
5	Storage at High Temperature and Humidity	60℃, 90%RH, 120Hours	IEC60068-2-78 :2001 GB/T2423.3—2006
6	Thermal Shock (non-operation)	-20℃ ↔ 70℃, ON/OFF, 20CYC	Start with cold temperature, End with high temperature, IEC60068-2-14:1984,G B2423.22-2002
7	ESD	Voltage:±8KV R:330 ohm,C:150pF Air discharge,10 times	IEC61000-4-2:2001 GB/T17626.2-2006
8	Vibration Test	10 => 55 =>10 => 55 => 10 Hz, within 1 minute;Amplitude:1.5mm. 15 minutes for each Direction (X,Y,Z)	IEC60068-2-6:1982 GB/T2423.10—1995
10	Package Drop Test	Packed, 66CM free fall 6 sides, 1 corner, 3edges	IEC60068-2-32:1990 GB/T2423.8—1995

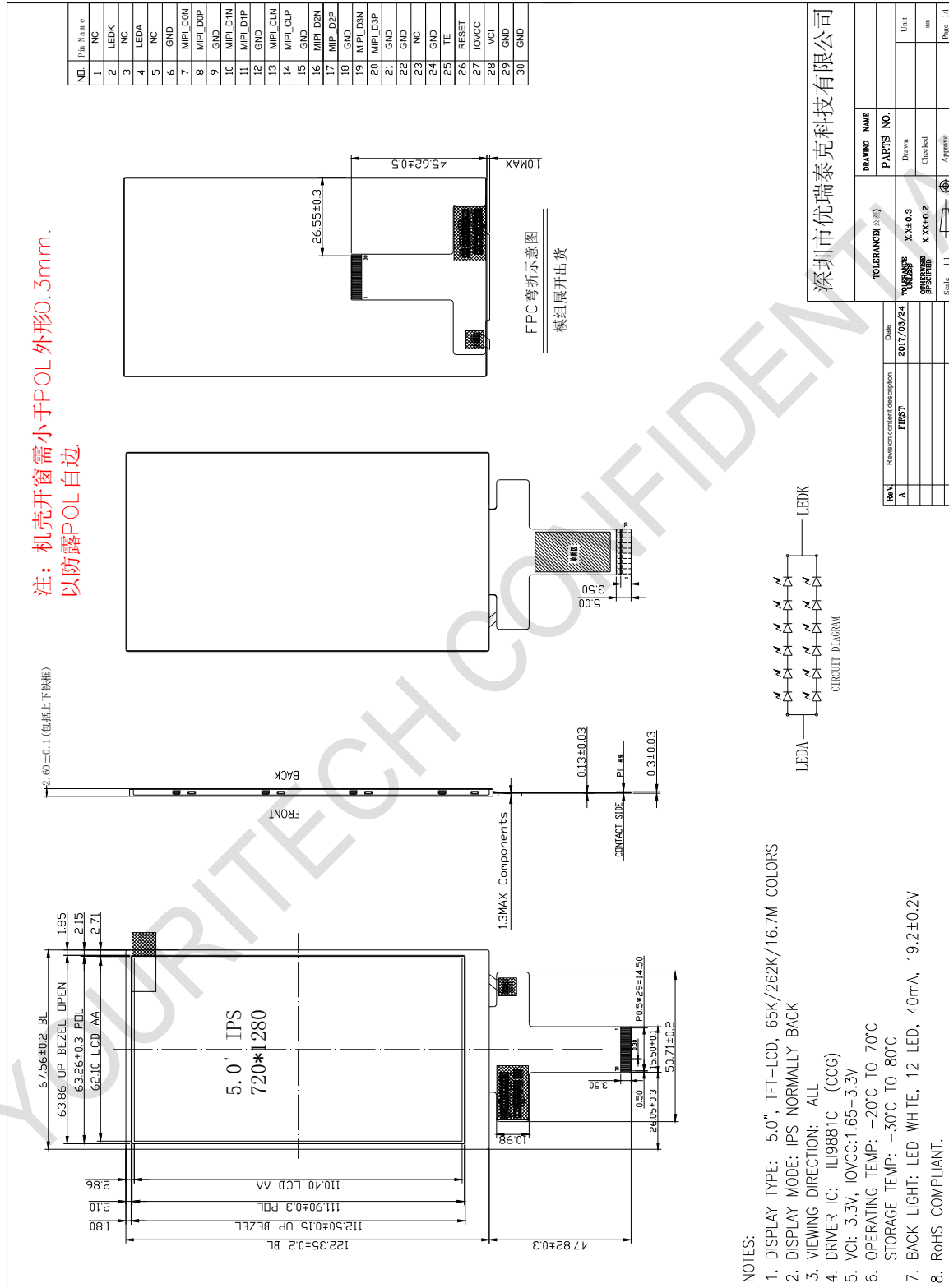
Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample.

Note3: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

8. Outline Dimension



9 Packing Drawing

TBD

10 Precautions for Use of LCD Modules

a) Handling Precautions

- i. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- ii. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.
- iii. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- iv. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- v. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:
 - Isopropyl alcohol
 - Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
 - Ketone
 - Aromatic solvents
- vi. Do not attempt to disassemble the LCD Module.
 - vii. If the logic circuit power is off, do not apply the input signals.
 - viii. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1 Be sure to ground the body when handling the LCD Modules.

10.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

b) Storage precautions

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i. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

ii. The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ~ 40℃ Relatively humidity: ≤80%

iii. The LCD modules should be stored in the room without acid, alkali and harmful gas.

c) Transportation Precautions

i. The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.