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MODEL NO : ET050HD03-TT

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2022-08-11

□Preliminary Specification

■Final Product Specification

Customer :_____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 720xRGBx1280.
As to basic specification of the driver IC, refer to the IC (ST7703) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

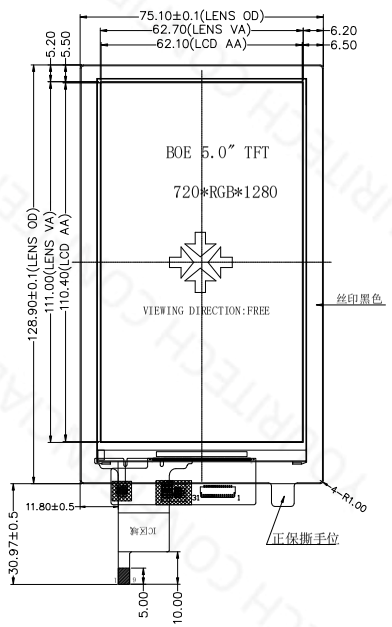
Structure: TFT PANNEL+IC +FPC+BL+CTP;
IPS Type LCD
720 dot-segment and 1280 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
4Lane MIPI interface

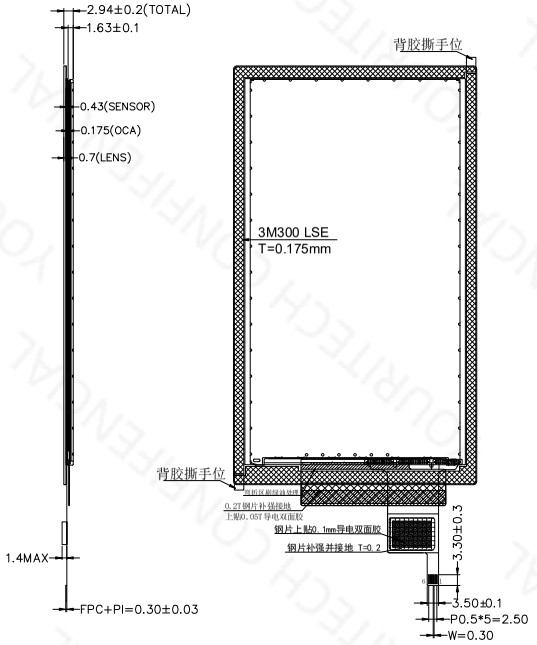
1.3 Applications:

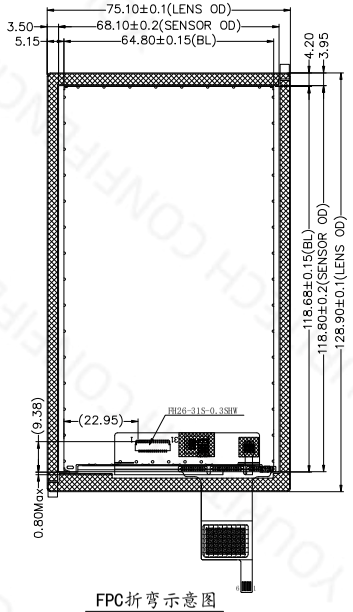
2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally black	--
Drive element	TFT active matrix	--
Number of pixels	720*3RGB(H)X1280(V)	Dots
Pixel arrangement	RGB Vertical stripe	--
Pixel Pitch (W*H)	0.08625(H) x0.08625 (V)	mm
Active area	62.10(H) x 110.40(V)	mm
Viewing direction	ALL O'CLOCK	mm
TFT Driver IC	ST7703	--
TFT interface	4Lane MIPI interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	64.80(W)x 118.68(H) x 1.63(T)	mm
LCM+CTP Size(W*H*T)	75.10(W)x 128.90(H) x 2.94(T)	mm
Touch structure	G+F+F	--
Touch Driver IC	GT911	--
Touch Interface	I2C	--

REV	DESCRIPTION	DRG DATE	DRAWN BY
	First Desing	2021.09.14	



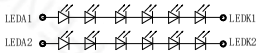




FPC折弯示意图
LCM FPC折弯出货
CTP FPC展开出货

Pad No.	Pad Name
1	LED_A
2	LED_A
3	LED_A
4	NC
5	LED_K
6	LED_K
7	LED_K
8	LED_K
9	GND
10	GND
11	MIPI_D2P
12	MIPI_D2N
13	GND
14	MIPI_D1P
15	MIPI_D1N
16	GND
17	MIPI_CLKP
18	MIPI_CLKN
19	GND
20	MIPI_D0P
21	MIPI_D0N
22	GND
23	MIPI_D3P
24	MIPI_D3N
25	GND
26	TE
27	RESET
28	GND
29	VDDIO1.8V
30	VDD3.3V
31	VDD3.3V

NOTES:
1. DISPLAY TYPE: 5.0", 720*1280 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: 80/80/80/80(TYP)
4. DRIVER IC:ST7703
5. LCM (White 9 AVG 1/9) :
   Brightness: 250cd/m^2 (TYP)
   Uniformity:80%(MIN)
6. BACK LIGHT: 12 chip white LEDs If=40mA,Vf=18V-20.4V
7. OPERATING TEMP: -20° C TO 60° C,STORAGE TEMP: -30° C TO 70° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS



技术参数：
盖板材质：旭硝子玻璃
1. 结构：G+FF
IC型号：GT911
2. 工作电压：3.3V
3. 透光率：≥82%
4. 表面硬度：6H
5. 工作环境：-20℃~+60℃，湿度20%~90%
6. 储存环境：-30℃~+70℃，湿度20%~90%
7. 未注尺寸公差按±0.2mm

NO.	SYMBOL
1	RST2.8V
2	INT2.8V
3	GND
4	SDA2.8V
5	SCL2.8V
6	VCC-2.8V

深圳市优瑞泰克科技有限公司

PART NO.:	ET050HD03-TT	MODULE NO.:	00
DRAWN BY:	LIU	DATE:	PROJECTION:
CHECKED BY:		DATE:	SCALE:N.T.S UNIT: mm
APPROVED BY:		DATE:	SHEET: 1 OF 1

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+60	°C
LCM Storage Temperature	T_{STG}	-30	+70	°C
TP Operating Temperature & Humidity(20% ~ 90%RH)	T_{OPR}	-20	+60	°C
TP SStorage Temperature & Humidity(20% ~ 90%RH)	T_{STG}	-30	+70	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	2.0	V
Supply Voltage for(DC/DC)	VDD	2.5	3.3	3.3	V
Supply Voltage for(DC/DC)	VSP	--	--	--	V
Supply Voltage for(DC/DC)	VSN	--	--	--	V

4.2 Back-Light Unit Characeristics

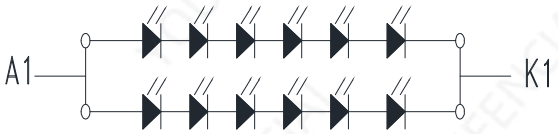
The back-light system is an edge-lighting type with 12 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	18	--	20.4	V	--
Forward current	I_F	--	40	--	mA	--
Luminance(With LCD)	Lv	--	250	--	cd/m^2	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



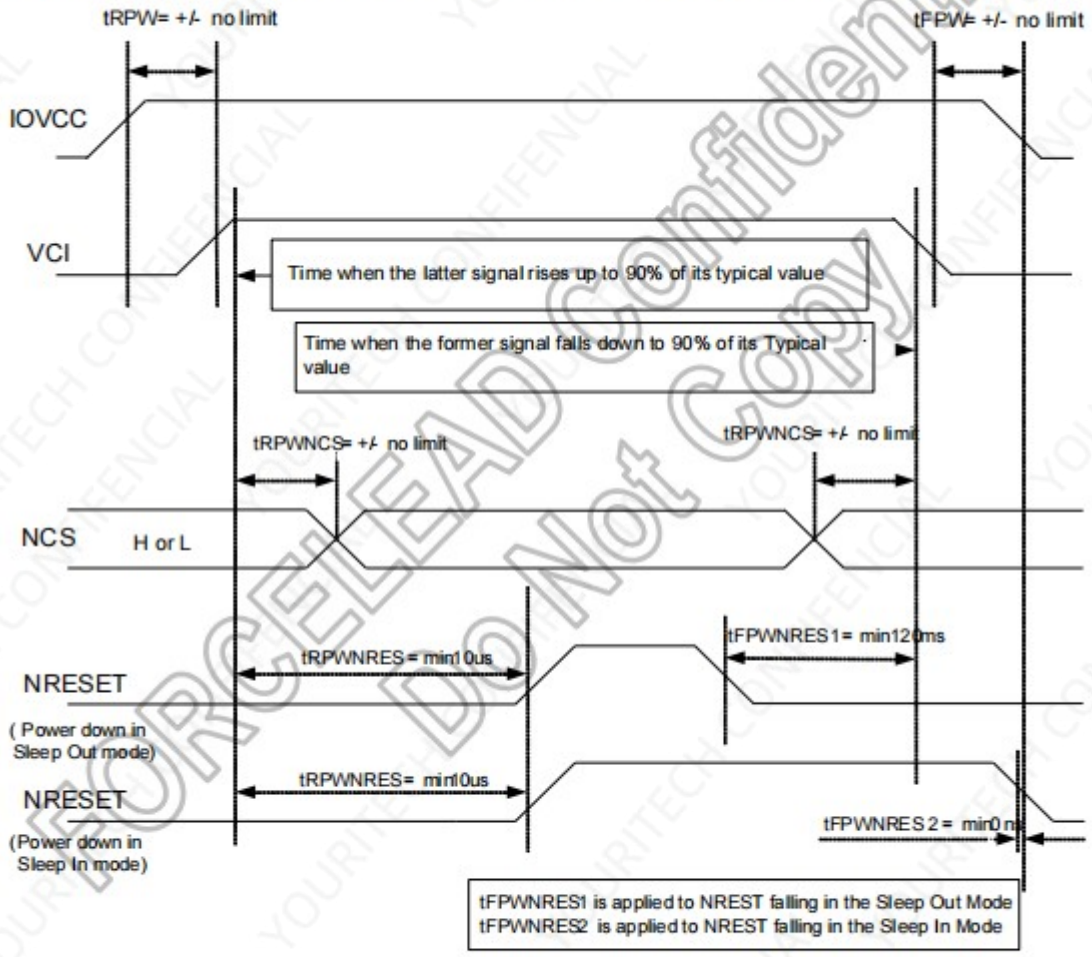
5. Module Function Description

Pin No.	Symbol	LCM Functional	Notes
1~3	LEDA	Power supply for backlight anode input terminal.	
4	NC	NC	
5~8	LEDK	Power supply for backlight cathode input terminal.	
9~10	GND	Power Ground	
11	MIPI_D2P	MIPI-DSI Data differential signal input pins	
12	MIPI_D2N	MIPI-DSI Data differential signal input pins	
13	GND	Power Ground	
14	MIPI_D1P	MIPI-DSI Data differential signal input pins	
15	MIPI_D1N	MIPI-DSI Data differential signal input pins	
16	GND	Power Ground	
17	MIPI_CKP	MIPI-DSI CLOCK differential signal input pins	
18	MIPI_CKN	MIPI-DSI CLOCK differential signal input pins	
19	GND	Power Ground	
20	DSI0_D0P	MIPI-DSI Data differential signal input pins	
21	DSI0_D0N	MIPI-DSI Data differential signal input pins	
22	GND	Power Ground	
23	DSI0_D3P	MIPI-DSI Data differential signal input pins	
24	DSI0_D3N	MIPI-DSI Data differential signal input pins	
25	GND	Power Ground	
26	TE	Tearing effect output pin.	
27	RESET	The external reset input initializes the chip with a low input.	
28	GND	Power Ground	
29	IOVCC 1.8V	power supply for the I/O circuit(1.65~2.0V)	
30~31	VCI 3.3V	power supply for DC/DC circuit(2.5~3.3V)	

Pin No.	Symbol	TP Functional	Notes
1	CTP_RESET 2.8V	CTP RESET PIN	
2	CTP_INT 2.8V	CTP INT PIN	
3	GND	Power Ground	
4	CTP_SDA 2.8V	CTP SDA PIN	
5	CTP_SCL 2.8V	CTP SCL PIN	
6	CTP_VDD 2.8V	CTP VDD PIN	

6. Timing Characteristics

If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10µsec after both VDD1, VDD2 and VDD3 have been applied.



Note: Unless otherwise specified timings herein show cross point at 50% of signal/power level

Figure 5.34: Case 2: RESX line is held low by host at power on

DSI Interface Timing Characteristics:

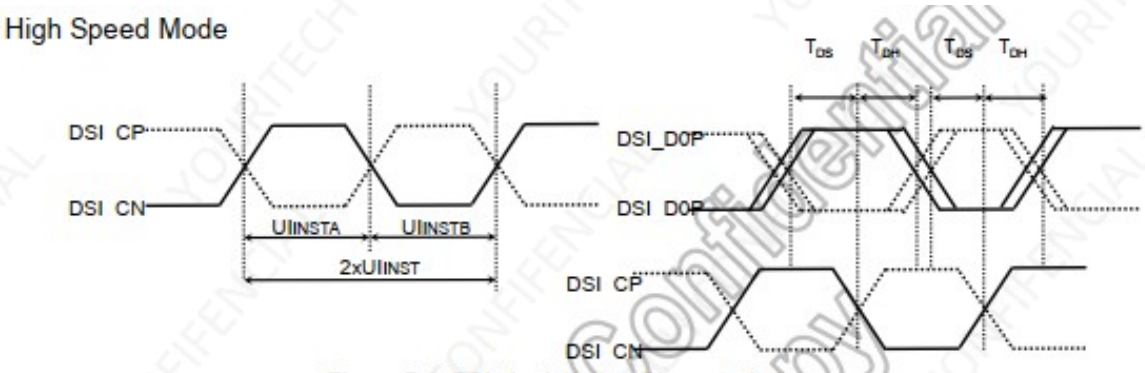


Figure 7.4: DSI clock timing Characteristics

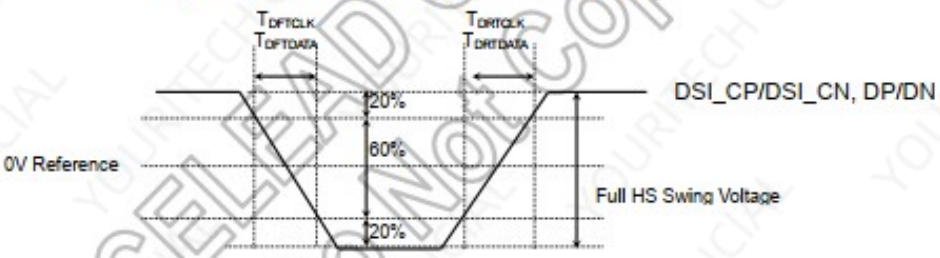


Figure 7.5: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xUINST	TBD	-	25	ns
	UI instantaneous	UINSTA UINSTB	TBD	-	12.5	ns
DP/DN	Data to clock setup time	TDS	0.15xUI	-	-	ps
	Data to clock hold time	TDH	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	TDRTCLK	150	-	0.3UI	ps
	Differential fall time for clock	TDFTCLK	150	-	0.3UI	ps
DP/DN	Differential rise time for data	TDRTDATA	150	-	0.3UI	ps
	Differential fall time for data	TDFTDATA	150	-	0.3UI	ps

Table 7.3: DSI High Speed Mode Characteristics

Low Power Mode

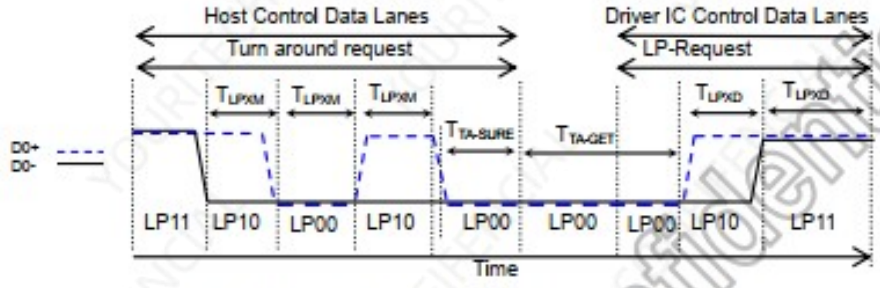


Figure 7.6: BTA from HOST to Display Module Timing

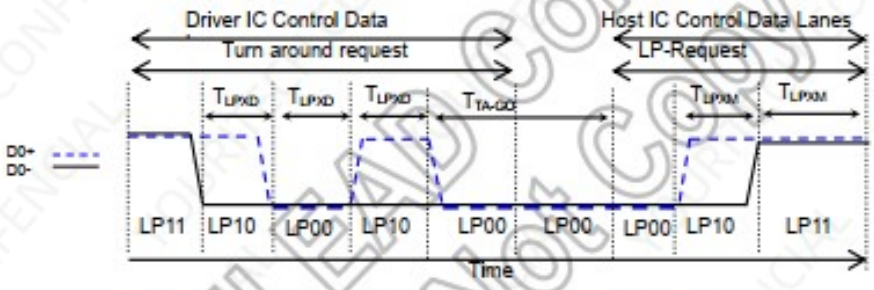


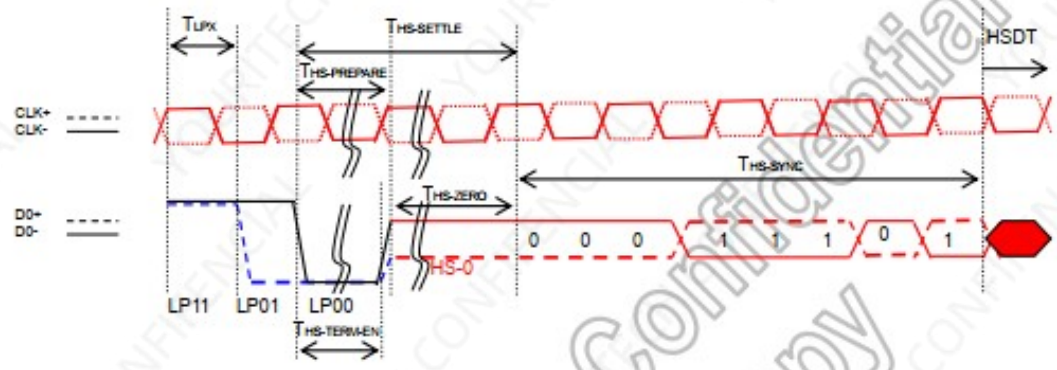
Figure 7.7: BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	2xT_{LPXD}	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

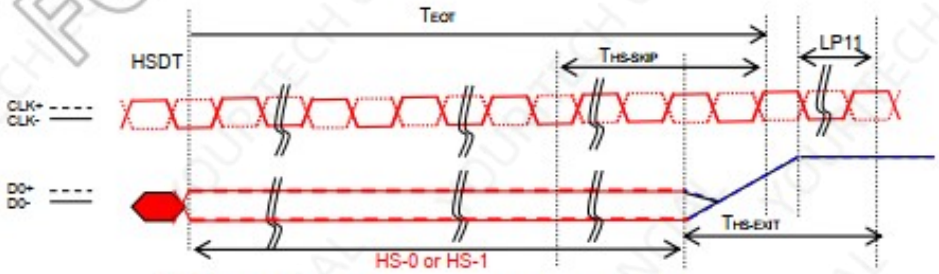
Table 7.4: DSI Low Power Mode Characteristics

DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

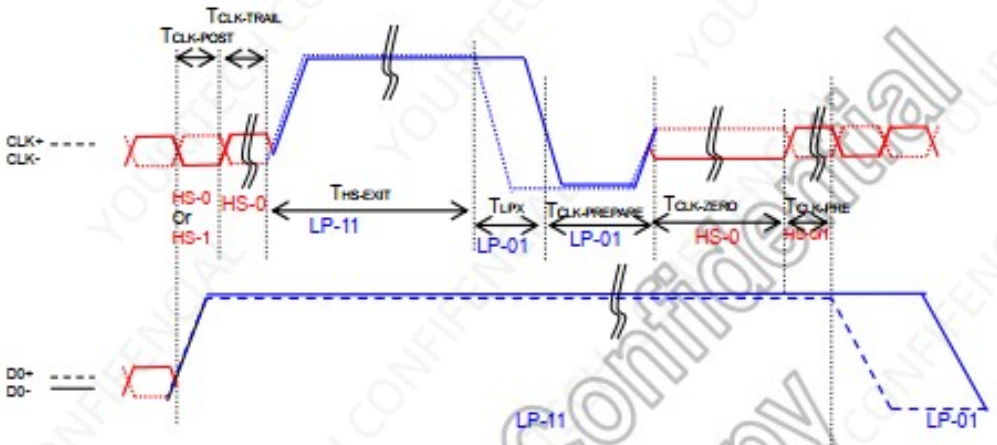
Table 7.5: DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

Table 7.6: DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK\ TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Table 7.7: Clock Lanes High Speed Mode to/from Low Power Mode Timing

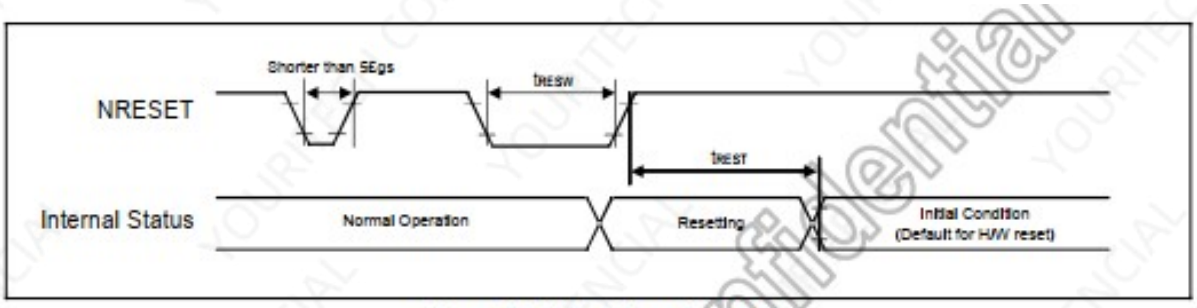


Figure 7.8: Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	μs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 7.8: Reset Input Timing

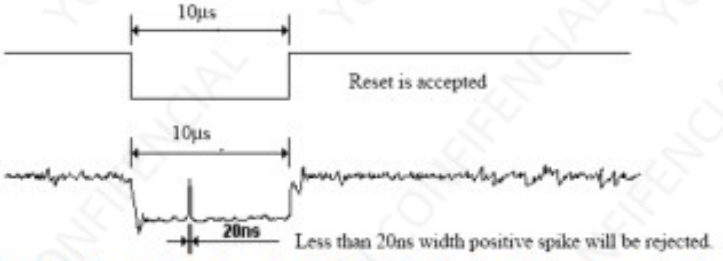
Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 15ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	-	80	-	Deg.	Note 1
		Θ_9		-	80	-	Deg.	
	Vertical	Θ_{12}		-	80	-	Deg.	
		Θ_6		-	80	-	Deg.	
Luminance Contrast ratio		CR	Θ = 0°	600	900	-		Note 2
Transmittance		T(%)	Θ = 0°	2.9 4.06 (APF)	3.22 4.51 (APF)	-	%	Base on C light Note 3
Color Gamut		CG	Θ = 0°	-	67	-	%	NTSC
White Chromaticity		x_w	Θ = 0°		0.29			Color Filter (with ITO) Based On C light Note 4
		y_w			0.33			
Reproduction of color	Red	x_R	Θ = 0°		0.661			
		y_R			0.323			
	Green	x_G			0.274			
		y_G			0.583			
	Blue	x_B			0.134			
		y_B			0.124			
Threshold Voltage		Vsat		3.7	3.9	4.1	V	Figure 3
		Vth		1.8	2.0	2.2	V	
Response Time (Rising + Falling)		T_{RT}	Ta= 25° C Θ = 0°	-	30	35	ms	Note 5

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. Theviewing angles are determined for the horizontal or 3, 9 o"clock direction and the vertical or 6, 12 o"clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 4 shown in Appendix).
2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (see Figure 4) Luminance Contrast Ratio (CR) is defined mathematically.
3. Transmittance is the Value with Polarizer
4. The color chromaticity coordinates specified in Table 4 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.Measurement condition is C light Source & Halogen Lamper
5. The electro-optical response time measurements shall be made as Figure 5 by switching the “data” input signal ON and OFF. The times needed for the transmittance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+70°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+60°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~60℃（30min），50 cycles	

9. Packing Method----TBD

- END -