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**MODEL NO :** ET055FH06-OT

**MODEL VERSION:** 01

**SPEC VERSION :** 1.0

**ISSUED DATE:** 2021-03-10

■Preliminary Specification
□Final Product Specification

Customer :_____

| Approved by | Notes |
|---|---|
| | |

Youri Confirmation

| Prepared by | Reviewed by | Approved by |
|---|---|---|
| John | Johnny | Wang |

| Record of Revision | | | |
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| Version | Revise Date | Page | Content |
| 00 | 2021/03/10 | all | First issue |
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# Contents

# 1. General Specifications

| No. | Item | Specification | Remark |
|---|---|---|---|
| 1 | LCD size | 5.5 inch | |
| 2 | Driver element | a-Si TFT active matrix | |
| 3 | Resolution | 1080(W) RGB x1920(H) | |
| 4 | Display mode | Normally Black, Transmissive | |
| 5 | Dot pitch | 0.063(W) x 0.063(H)mm | |
| 6 | Active area | 68.04(W) x 120.96(H) mm | |
| 7 | Module size | 75.94(W) x 134.56(H) ×3.285(D) mm | Note 1 |
| 9 | View direction | ALL | O ‘clock |
| 10 | Surface treatment | Anti-Glare | |
| 11 | Color arrangement | RGB-stripe | |
| 12 | Interface | MIPI | |
| 13 | Drive IC | HX8398 | |

Note 1: Refer to Mechanical drawing.

# 2. Pin Assignmen

FPC Connector is used for the module electronics interface. The recommended model is DF40C-40DP-0.4V(51)

| Pin No | Symbol | Function | Remark |
|---|---|---|---|
| 1 | GND | GND Ground | |
| 2 | GND | GND Ground | |
| 3 | TOUCH_RST | Touch reset（1.8V) | |
| 4 | LCD_RST | LCD reset | |
| 5 | TOUCH_INT | Touch INT（1.8V) | |
| 6 | LCD_TE | LCD_TE LCD Tearing effect output | |
| 7 | I2C4_SDA_TP | Touch I2C SDA（1.8V) | |
| 8 | LCD_ID | LCD_ID signal | |
| 9 | I2C4_SCL_TP | Touch I2C SCL（1.8V) | |
| 10 | GND | Ground | |
| 11 | VCC_TP | Touch power(+2.8V) | |
| 12 | MIPI_TXO_D0N | MIPI data lane 0 negative end input/output pin | |
| 13 | GND | Ground | |
| 14 | MIPI_TXO_D0P | MIPI data lane 0 positive end input/output pin | |
| 15 | VCC_LED+ | Backlight LED+ | |
| 16 | GND | Ground | |
| 17 | VCC_LED+ | Backlight LED+ | |
| 18 | MIPI_TXO_D1N | MIPI data lane 1 negative end input/output pin | |
| 19 | GND | Ground | |
| 20 | MIPI_TXO_D1P | MIPI data lane 1 positive end input/output pin | |
| 21 | VCC_LED_3- | Backlight LED3- | |
| 22 | GND | Ground | |
| 23 | VCC_LED_2- | Backlight LED2- | |
| 24 | MIPI_TXO_CLKN | MIPI DSI clock lane negative end input pin | |
| 25 | VCC_LED_1- | Backlight LED1- | |
| 26 | MIPI_TXO_CLKP | MIPI DSI clock lane positive end input pin | |
| 27 | GND | Ground | |
| 28 | GND | Ground | |
| 29 | 7P0_PWM_OUT | PWM out for brightness of backlight | |
| 30 | MIPI_TXO_D2N | MIPI data lane 2 negative end input/output pin | |

| | | | |
|---|---|---|---|
| 31 | VCC_LCD | LCD power | |
| 32 | MIPI_TXO_D2P | MIPI data lane 2 positive end input/output pin | |
| 33 | GND | Ground | |
| 34 | GND | Ground | |
| 35 | VSP | VSP LCD power | |
| 36 | MIPI_TXO_D3N | MIPI data lane 3 negative end input/output pin | |
| 37 | VSN | VSN LCD power | |
| 38 | MIPI_TXO_D3P | MIPI data lane 3 positive end input/output pin | |
| 39 | GND | GND Ground | |
| 40 | GND | GND Ground | |

Note I: input; O: output; P: Power or Ground(0V).

# 3. Operation Specifications

## 3.1. Electrical Specifications

**Test condition: GND=0V, $T_A$=25 °C**

Note1

| Item | Symbol | Values | | | Unit | Remark |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Power voltage | VCC_LCD | 1.65 | 1.8 | 1.95 | V | |
| | VCC_TP | 2.7 | 2.8 | 3.4 | | |
| | VSP | 5.44 | 5.54 | 5.64 | V | |
| | VSN | -5.64 | -5.54 | -5.44 | | |
| Input logic high voltage | $V_{IH}$ | 0.7 VCC_LCD | - | VCC_LCD | V | |
| Input logic low voltage | $V_{IL}$ | GND | - | 0.3 VCC_LCD | V | |

## 3.2. Current Consumption

| Item | Symbol | Values | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Current for Driver | $I_{VCC\_LCD}$ | - | 27 | 40 | mA | Note1 |
| | $I_{VSP}$ | - | 7 | 15 | mA | Note1 |
| | $I_{VSN}$ | - | 7 | 15 | mA | Note1 |

Note1:Max. specification： White test Pattern

### 3.2.1.LED drive conditions

| Item | Symbol | Values | | | Unit | Remark |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Voltage for LED Backlight | $V_L$ | 27.5 | - | 32.0 | | Note 1 |
| Current for LED Backlight | $I_L$ | | 60 | | mA | |
| LED life time | - | 20,000 | - | - | Hr | Note 2 |

Note1: $I_L$=60mA (Backlight circuit: 5 series connection, 3 parallel connection), the ambient temperature is 25℃.

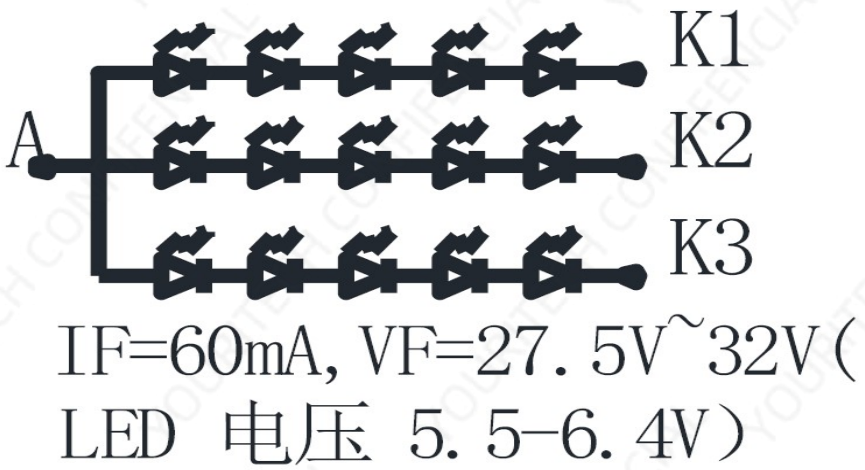
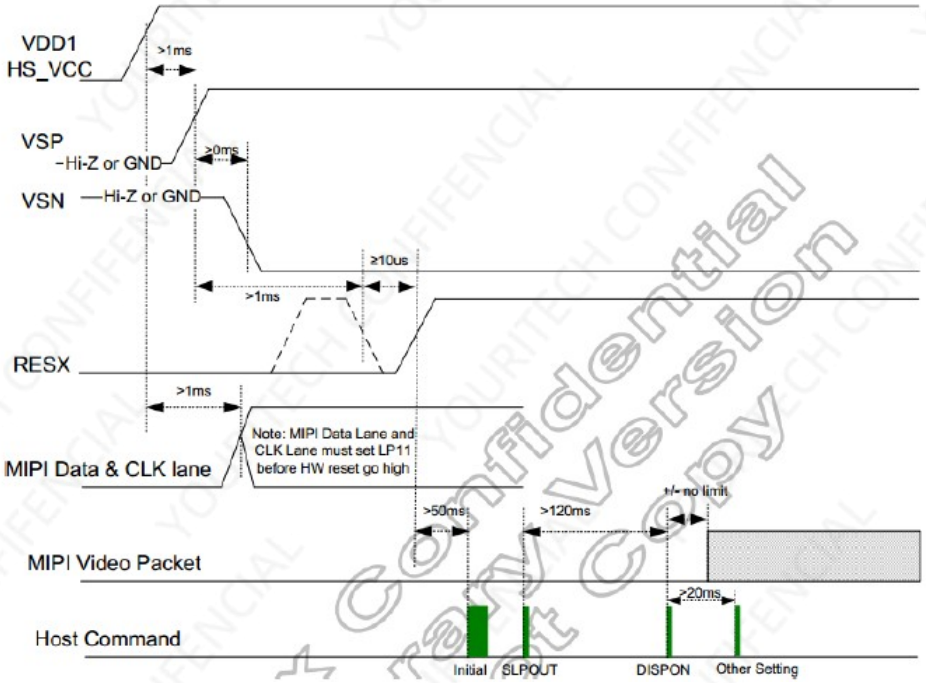


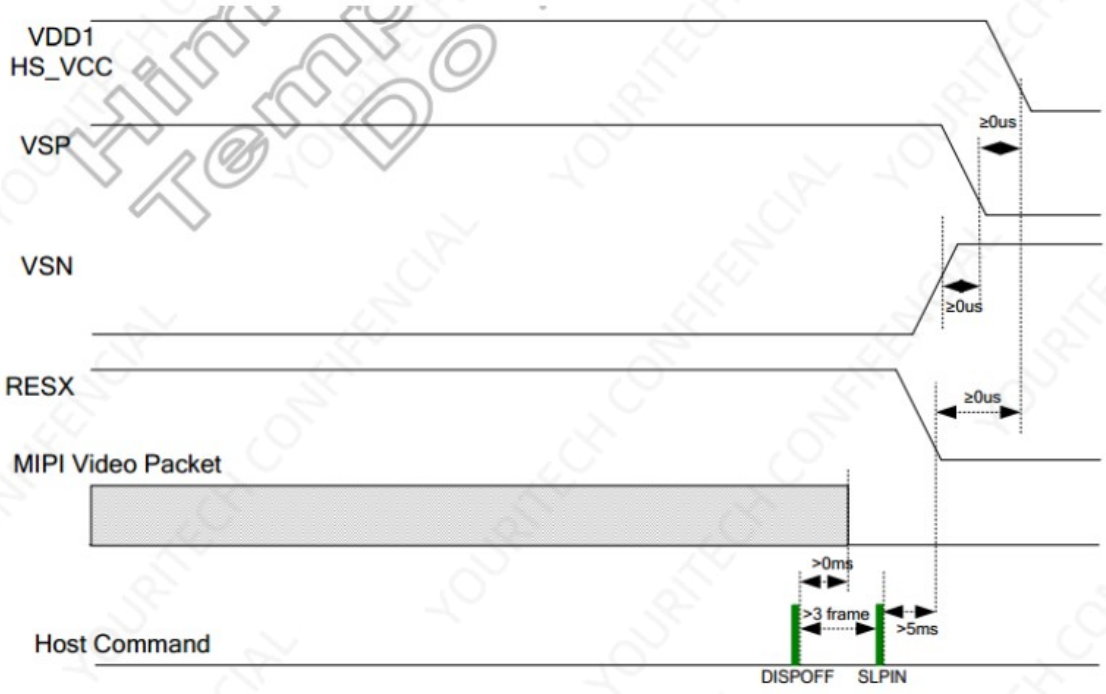

Fig. 3-1 LED test circuit diagram

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and 1/2 rated current . The LED lifetime could be decreased if operating $I_L$ is larger than 60 mA.

## 3.3. Power Sequence




Power on




Power off

## 3.4. Reset input timings

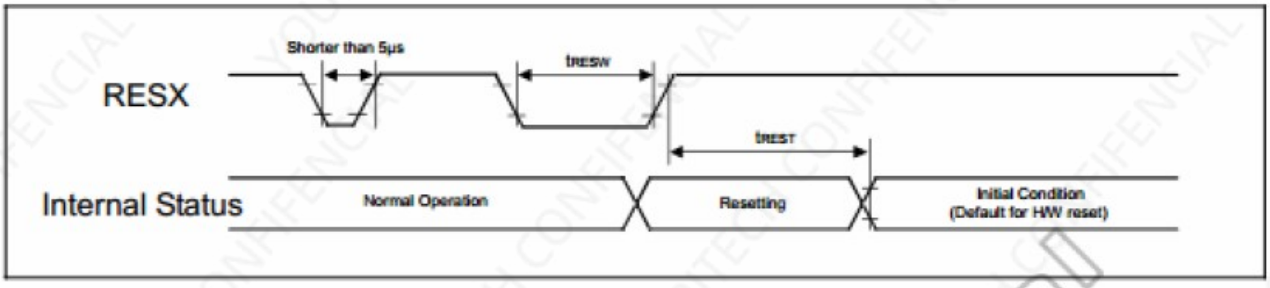



**Figure 8.12: Reset input timing**

| Symbol | Parameter | Related pins | Spec. | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| $t_{RESW}$ | Reset low pulse width[1] | RESX | 10 | - | - | µs | - |
| $t_{REST}$ | Reset complete time[2] | - | - | - | 50 | ms | - |

**Note:** (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

| RESX Pulse | Action |
|---|---|
| Shorter than 5 µs | Reset Rejected |
| Longer than 10 µs | Reset |
| Between 5 µs and 10 µs | Reset Start |

(2) During Reset Complete Time, OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 50ms after a rising edge of RESX.
(3) Spike Rejection also applies during a valid reset pulse as shown below:

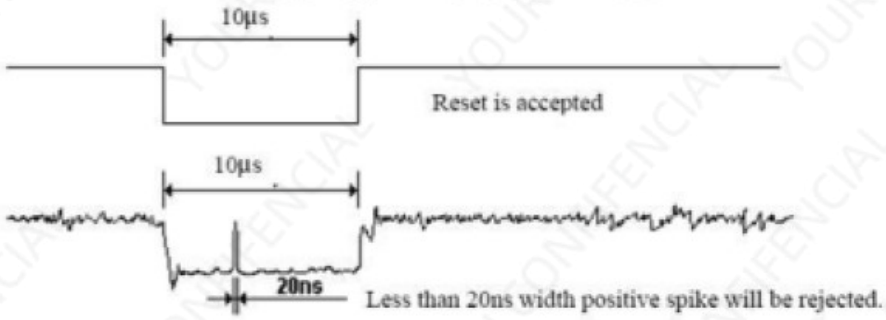
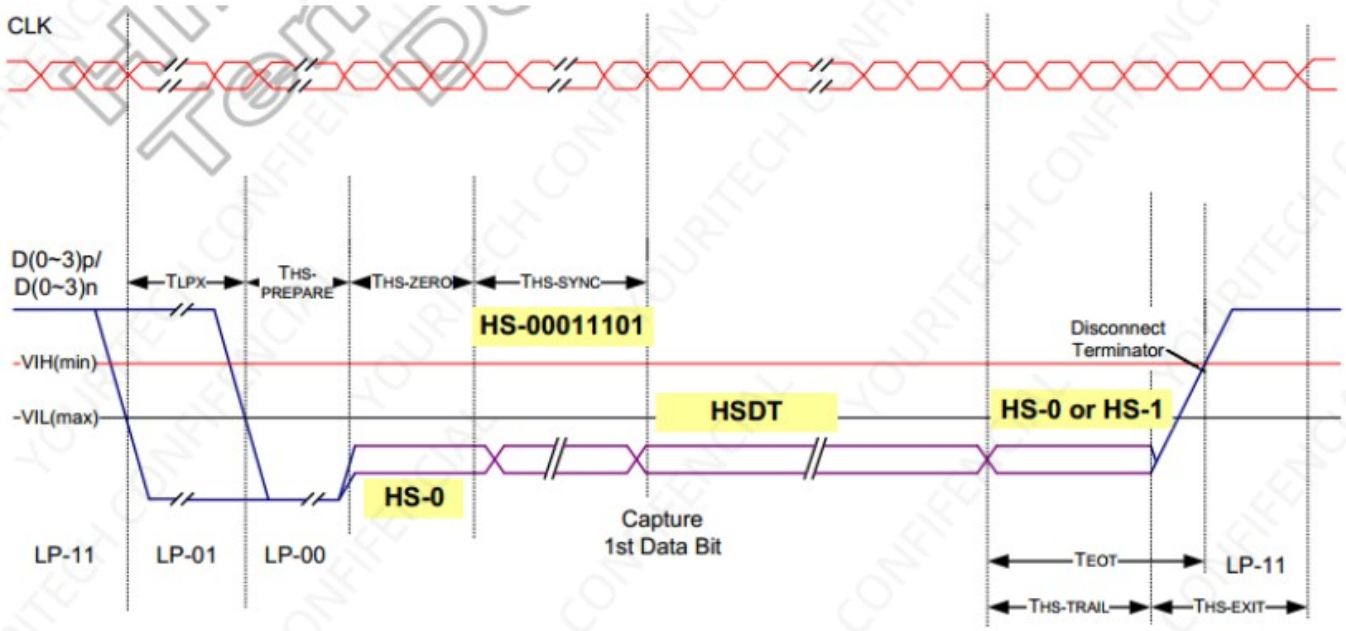



**Table 8.16: Reset timing**

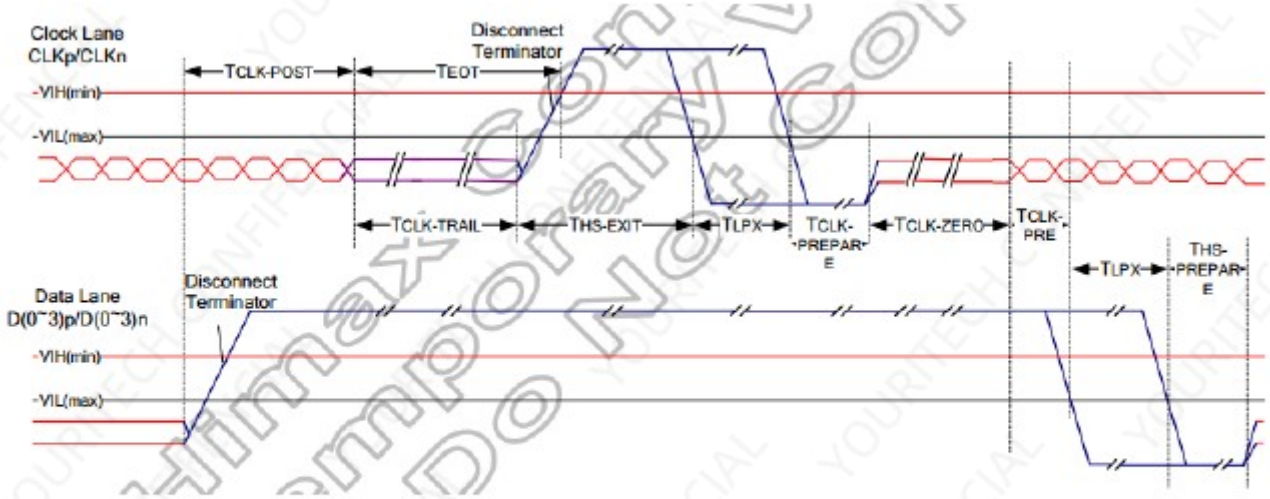
## 3.5. Power sequence read/write timing characteristics

### 3.5.1. Reset sequence




| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{HS-PREPARE}$ | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | 40+4*UI | - | 85+6*UI | ns |
| $T_{HS-PREPARE}$+ $T_{HS-ZERO}$ | THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. | 145+10*UI | - | - | ns |
| $T_{EOT}$ | Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst. | - | - | 105ns+12*UI | ns |
| $T_{HS-TRAIL}$ | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst. | 60ns+4*UI | - | - | ns |
| $T_{HS-EXIT}$ | Time that the transmitter drives LP-11 following a HS burst. | 100 | - | - | ns |

## 3.5.2.Power sequence read/write timing characteristics




| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{CLK-POST}$ | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. | 60+52*UI | - | - | ns |
| $T_{CLK-TRAIL}$ | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst. | 60 | - | - | ns |
| $T_{CLK-PREPARE}$ | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 38 | - | 95 | ns |
| $T_{CLK-PREPARE+}$ $T_{CLK-ZERO}$ | TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock. | 300 | - | - | ns |
| $T_{CLK-PRE}$ | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8*UI | - | - | ns |

# 4. Optical Specifications

| Item | Symbol | Condition | Values | | | Unit | Remark |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Viewing angle (CR≥ 10) | $\theta_L$ | Φ=180°(9 o'clock) | - | 80 | - | degree | Note 1 |
| | $\theta_R$ | Φ=0°(3 o'clock) | - | 80 | - | | |
| | $\theta_T$ | Φ=90°(12 o'clock) | - | 80 | - | | |
| | $\theta_B$ | Φ=270°(6 o'clock) | - | 80 | - | | |
| Response time | $T_{ON+}$ $T_{OFF}$ | Normal θ=Φ=0° | - | 35 | 45 | msec | Note 3 |
| Contrast ratio | CR | | 1100 | 1500 | - | - | Note 4 |
| Color chromaticity | $W_X$ | | 0.2727 | 0.3027 | 0.3327 | - | Note 2 Note 5 Note 6 |
| | $W_Y$ | | 0.2732 | 0.3032 | 0.3332 | - | |
| Luminance | L | | 800 | 900 | - | cd/m² | Note 6 |
| Luminance uniformity | $Y_U$ | | 70 | 80 | - | % | Note 7 |
| Color Gamut | NTSC | CIE1931 | 60 | 70 | - | % | |

The test systems refer to Note 2.

Note 1: Definition of viewing angle range

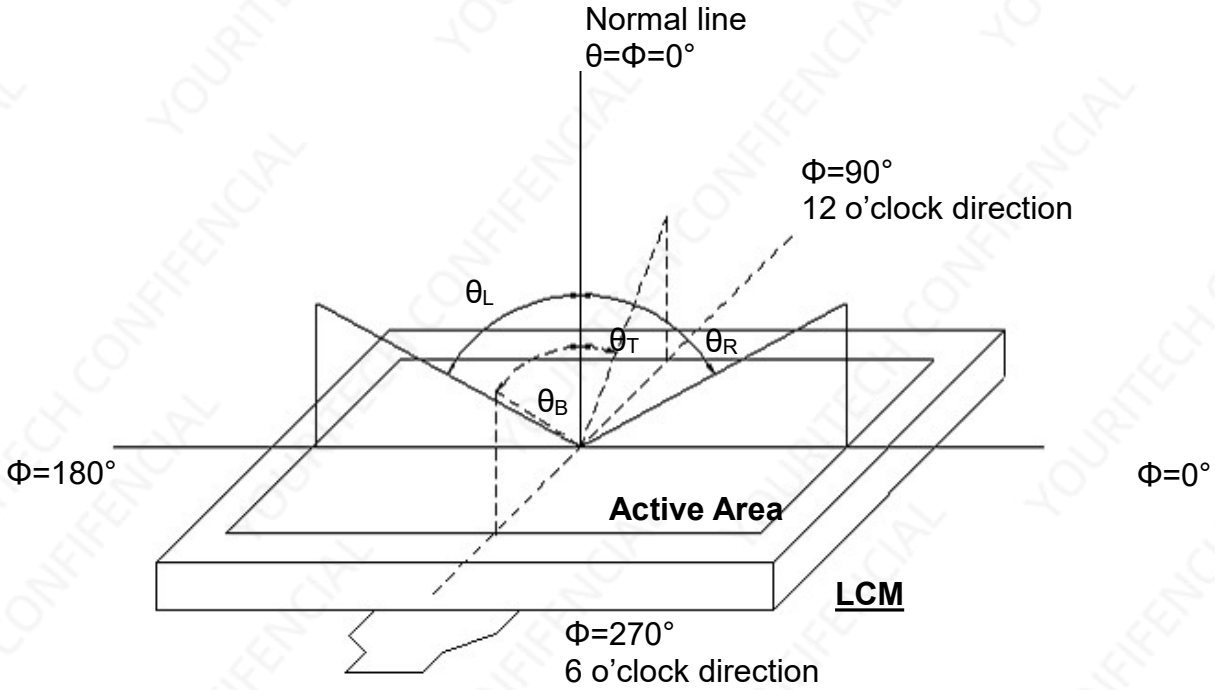



Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Viewing angle is measured by ELDIM-EZ contrast/Height :1.2mm, Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/ Field of view: 1° /Height: 500mm.) or CA-210.

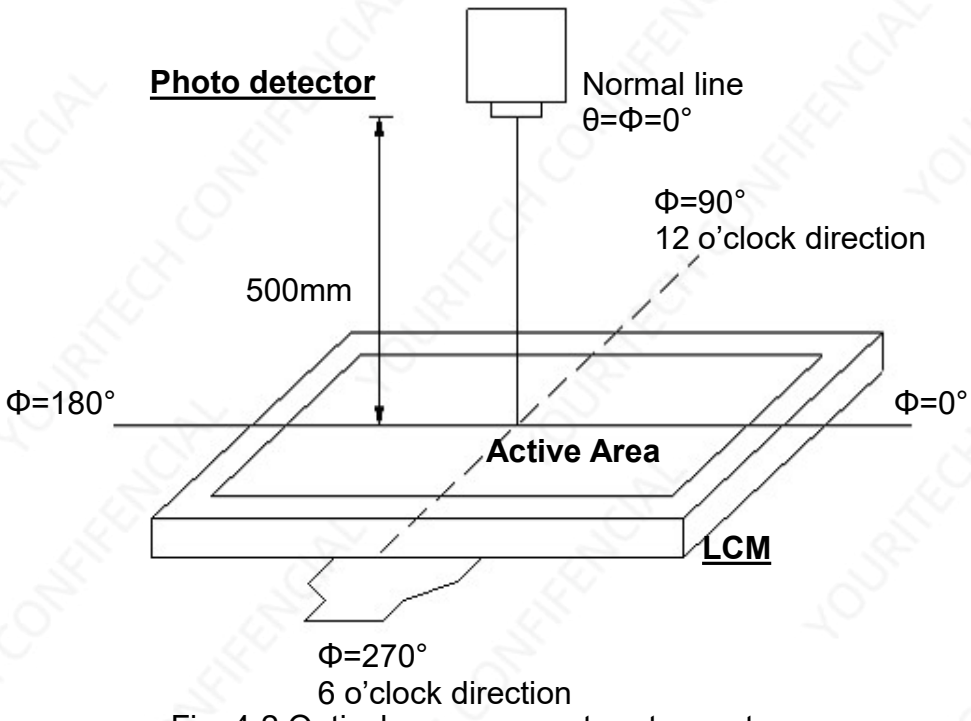



Fig. 4-2 Optical measurement system setup

Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time ($T_{ON}$) is the time between photo detector output intensity changed from 90% to 10%. And fall time ($T_{OFF}$) is the time between photo detector output intensity changed from 10% to 90%.

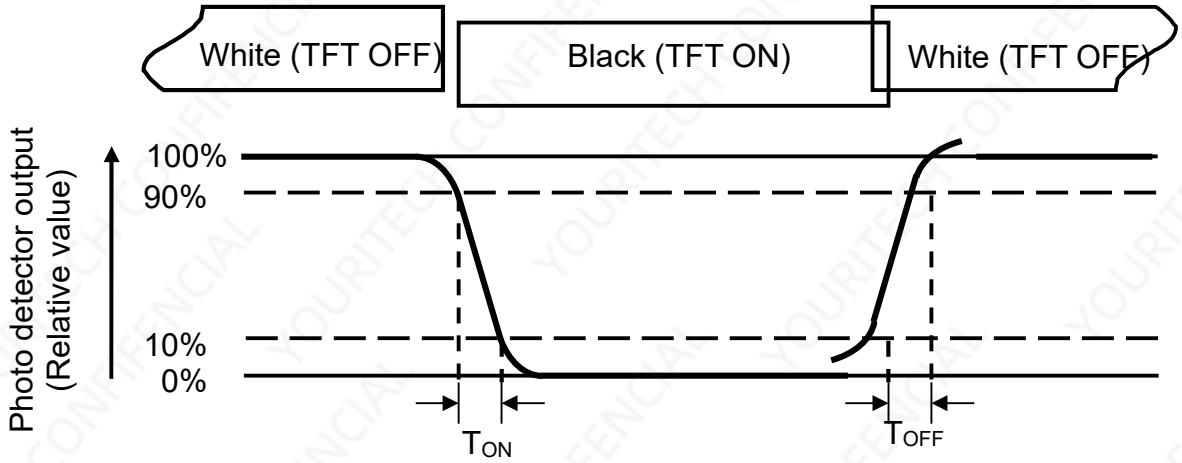



Fig. 4- 3 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground while measuring the center area of the panel. The LED driving condition is $I_L$=120mA .

Note 7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas(Refer to Fig. 4-4).
Every measuring point is placed at the center of each measuring area.

$$Luminance\ \ Uniformity\ (Yu) = \frac{B_{min}}{B_{max}}$$

L-------Active area length  W----- Active area width

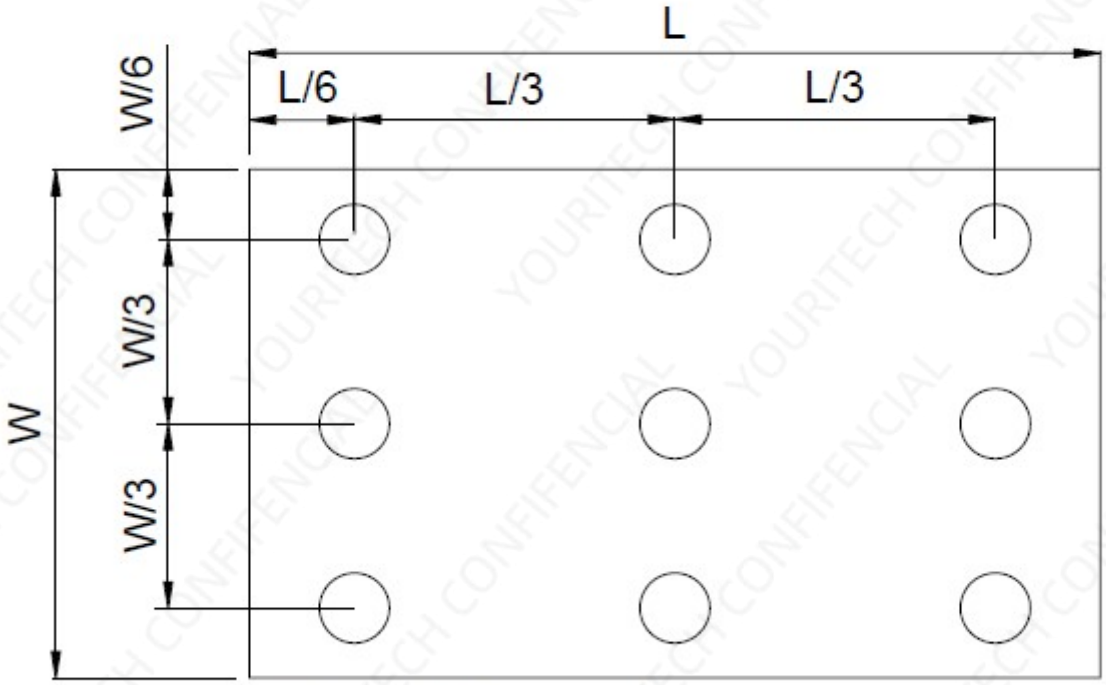



Fig. 4-4 Definition of measuring points

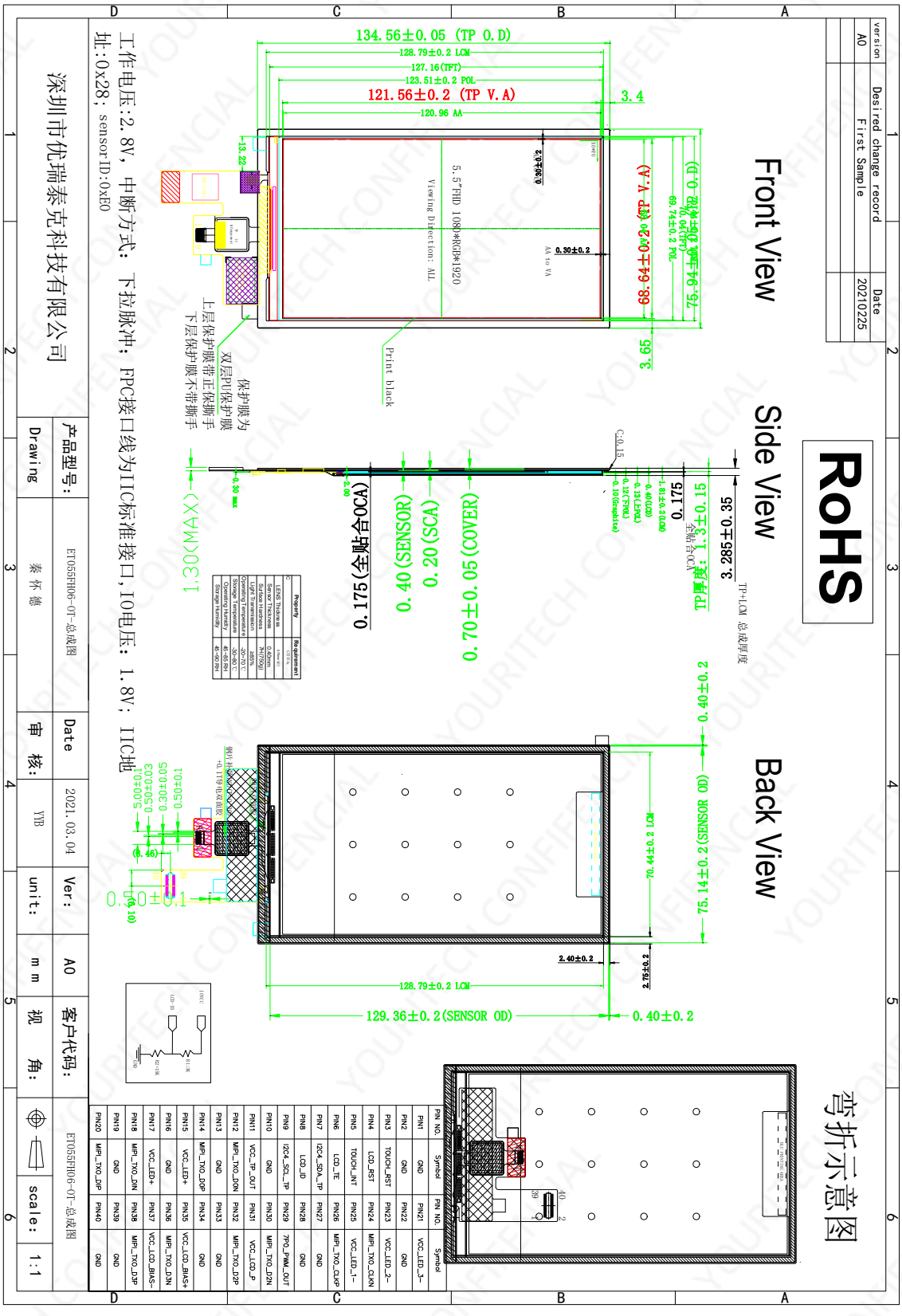
$B_{MAX}$: The measured maximum luminance of all measurement position.
$B_{MIN}$: The measured minimum luminance of all measurement position.

# 5. Reliability Test

| Item | Test Conditions | Criterion |
|---|---|---|
| High Temperature Storage | Ta = 80℃ 240hrs | A,B,C,D,E |
| Low Temperature Storage | Ta = -30℃ 240hrs | A,B,C,D,E |
| High Temperature Operation | Ts = 70℃ 240hrs | A,B,C,D,E |
| Low Temperature Operation | Ta =-20℃ 240hrs | A,B,C,D,E |
| Operate at High Temperature and Humidity | +60℃, 90%RH 240hrs | A,B,C,D,E |
| Thermal Shock(non operation) | -30℃/30 min ~ +80℃/30 min for a total 24 cycles, Start with cold temperature and end with high temperature. | A,B,C,D,E |
| Vibration Test | Sweep:10Hz~55Hz~10Hz 2G<br>2 hours for each direction of X. Y. Z.<br>(6 hours for total) | A,B,C,D,E |
| Package Vibration Test | Random Vibration :<br>0.015G*G/Hz from 5-200HZ, -6dB/Octave from 200-500HZ<br>2 hours for each direction of X. Y. Z.<br>(6 hours for total) | A,B,C,D,E |
| Package Drop Test | Height:60 cm<br>1 corner, 3 edges, 6 surfaces | A,B,C,D,E |
| Electro Static Discharge | Contact=+/-4KV,<br>Air=+/-8KV,(R=330R,C=150pF), 1 sec,9point,10times/point; | A,B,C,D,E |

※Criterion:
A.LCM each function is OK,.
B.LCM appearance inspection without abnormalities (Including scratch, damage, corrosion and serious deformation)
C.LCM brightness above the Min. value of Spec.
D. Luminance uniformity above the Min. value of Spec.
E. Color chromaticity within tolerance range

# 6. Mechanical Drawing



# 7. Package Drawing

TBD

# 8. General Precautions

## 8.1. Safety

Liquid crystal is poisonous. Do not put it in your mouth. If liquid crystal touches your skin or clothes, wash it off immediately by using soap and water.

## 8.2. Handling

1. The LCD panel is plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
2. The polarizer attached to the display is easily damaged. Please handle it carefully to avoid scratch or other damages.
3. To avoid contamination on the display surface, do not touch the module surface with bare hands.
4. Keep a space so that the LCD panels do not touch other components.
5. Put cover board such as acrylic board on the surface of LCD panel to protect panel from damages.
6. Transparent electrodes may be disconnected if you use the LCD panel under environmental conditions where the condensation of dew occurs.
7. Do not leave module in direct sunlight to avoid malfunction of the ICs.

## 8.3. Static Electricity

1. Be sure to ground module before turning on power or operating module.
2. Do not apply voltage which exceeds the absolute maximum rating value.

## 8.4. Storage

1. Store the module in a dark room where must keep at 25±10℃ and 65%RH or less.
2. Do not store the module in surroundings containing organic solvent or corrosive gas.
3. Store the module in an anti-electrostatic container or bag.

## 8.5. Cleaning

1. Do not wipe the polarizer with dry cloth. It might cause scratch.
2. Only use a soft sloth with IPA to wipe the polarizer, other chemicals might permanent damage to the polarizer.