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| | |
|---|---|
| Project No.<br>项目编号 | ET055HD11-T |
| Customer<br>客户名称 | |
| Module No.<br>客户型号 | |
| Product type<br>产品内容 | **Standard LCD Module**<br>**TFT：720*RGBx1280Dots**<br>**5.5”TFT LCD** |

| 客户确认Customer Approval | |
|---|---|
| 项目负责人Project Manager | |
| 品质主管Director of Quality | |
| 采购工程师Purchasing Engineer | |

| PREPARED BY | CHECKED BY | APPROVED BY |
|---|---|---|
| | | |
| | | |

# 1. Introduction

## 1.1 Scope of application

This specification applies to the LCD module that is supplied by YOURITECH Technology CO., LTD.
LCD specification: Dots 720xRGBx1280.
As to basic specification of the driver IC, refer to the IC (ILI9881C) specification and data book.
All material & processing of the LCD module should be Lead Free.

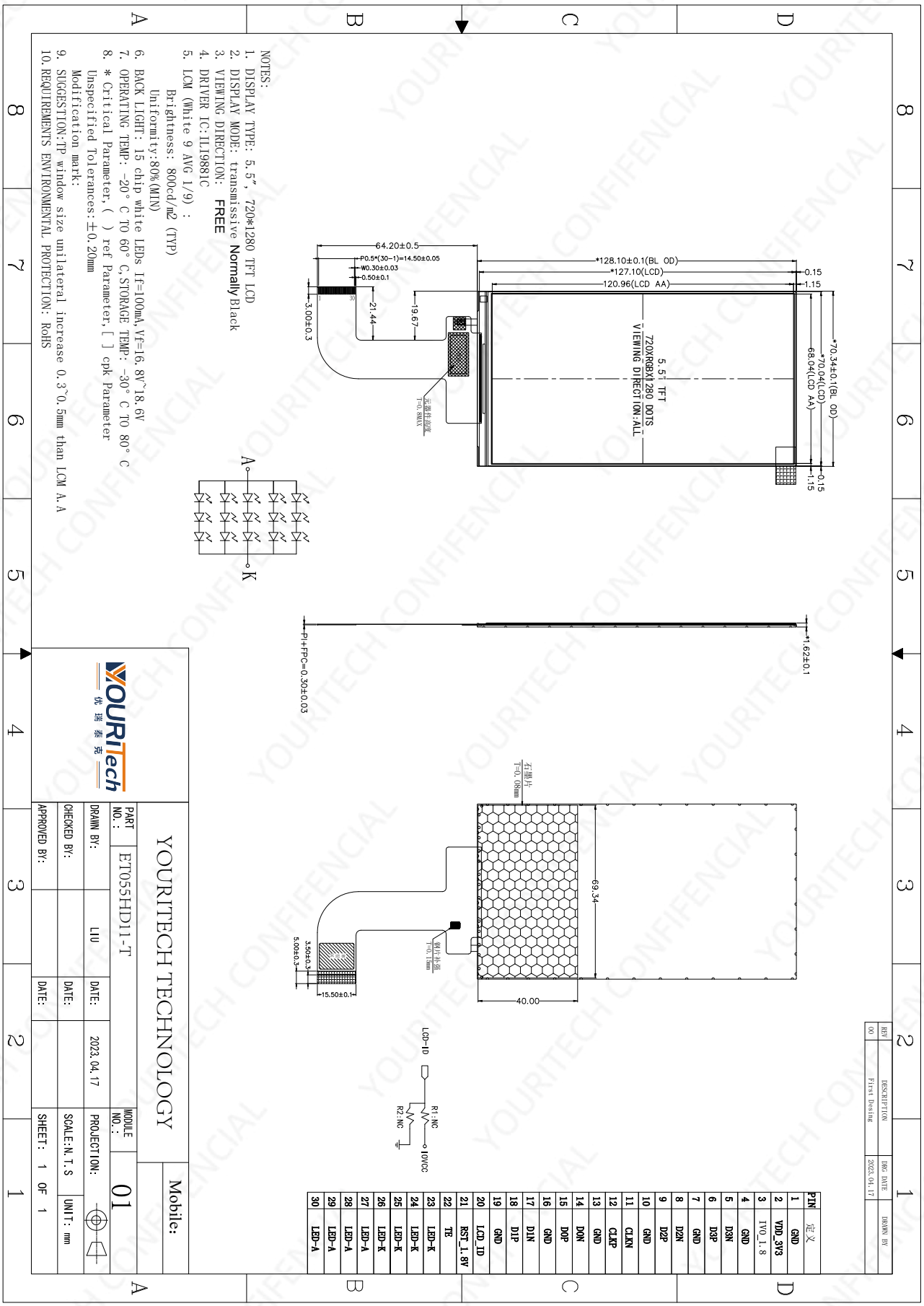
## 1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL;
IPS Type LCD
720dot-segment and 1280 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
4lane MIPI interface

## 1.3 Applications:

## 2. LCM General specification

| ITEM | Sandard value | Unit |
|---|---|---|
| LCD Type | Normally Black | -- |
| Drive element | TFT active matrix | -- |
| Number of pixels | 720*3RGB(H)X1280(V) | Dots |
| Pixel arrangement | RGB stripe | -- |
| Pixel Pitch (W*H) | 0.0945(W) × 0.0945 (H) | mm |
| Active area | 68.04(W) × 120.96(H) | mm |
| Viewing direction | ALL O'CLOCK | -- |
| TFT Driver IC | ILI9881C | -- |
| TFT interface | 4lane MIPI interface | -- |
| Approx. Weight | TBD | g |
| LCM Size(W*H*T) | 70.34(W) ×128.10(H) ×1.62(T) | mm |
| Touch structure | -- | -- |
| Touch Driver IC | -- | -- |
| Touch Interface | -- | -- |


NOTES:
1. DISPLAY TYPE: 5.5", 720*1280 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: FREE
4. DRIVER IC:ILI9881C
5. LCM (White 9 AVG 1/9) :
Brightness: 800cd/m2 (TYP)
Uniformity:80%(MIN)
6. BACK LIGHT: 15 chip white LEDs If=100mA, Vf=16.8V~18.6V
7. OPERATING TEMP: -20° C TO 60° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
Unspecified Tolerances:±0.20mm
Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS
64.20±0.5
P0.5*(30-1)=14.50±0.05
W0.30±0.03
0.50±0.1
3.00±0.3
21.44
19.67
*128.10±0.1(BL OD)
*127.10(LCD)
120.96(LCD AA)
0.15
1.15
*70.34±0.1(BL OD)
*70.04(LCD)
68.04(LCD AA)
5.5" TFT
720XRGBX1280 DOTS
VIEWING DIRECTION:ALL
A
K
PI+FPC=0.30±0.03
*1.62±0.1
69.34
40.00
15.50±0.1
3.50±0.3
5.00±0.3
LCD-ID
R1:NC
R2:NC
10VCC
PIN 定义
1 GND
2 VDD_3V3
3 IVO_1.8
4 GND
5 D3N
6 D3P
7 GND
8 D2N
9 D2P
10 GND
11 CLKN
12 CLKP
13 GND
14 DON
15 DOP
16 GND
17 D1N
18 D1P
19 GND
20 LCD_ID
21 RST_1.8V
22 TE
23 LED-K
24 LED-K
25 LED-K
26 LED-K
27 LED-A
28 LED-A
29 LED-A
30 LED-A
REV 00
DESCRIPTION First Drawing
DRG DATE 2023.04.17
DRAWN BY
YOURITECH TECHNOLOGY
Mobile:
PART NO.: ET055HD11-T
MODULE NO.: 01
DRAWN BY: LIU
DATE: 2023.04.17
PROJECTION:
CHECKED BY:
DATE:
SCALE:N.T.S
UNIT: mm
APPROVED BY:
DATE:
SHEET: 1 OF 1

# 3.Absolute Maximum Rating

| Characteristics | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| LCM Operating Temperature | $T_{OPR}$ | -20 | +60 | °C |
| LCM Storage Temperature | $T_{STG}$ | -30 | +80 | °C |
| Humidity | RH | -- | 90 | % |

# 4.Electrical Characteristics

## 4.1 TFT DC Characteristics

| Characteristics | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply Voltage for I/O | VDDIO | 1.65 | 1.8 | 3.3 | V |
| Supply Voltage for(DC/DC) | VDD | 2.5 | 3.3 | 3.3 | V |
| Supply Voltage for(DC/DC) | AVDD | -- | -- | -- | V |
| Supply Voltage for(DC/DC) | AVEE | -- | -- | -- | V |

## 4.2 Back-Light Unit Characeristics

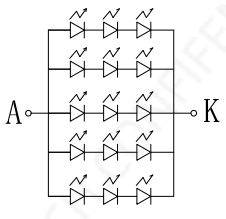
The back-light system is an edge-lighting type with 15 white LEDs. The characteristics of the back-light are shown in the following tables.

| Characteristics | Symbol | Min. | Type | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Forward Voltage | $V_F$ | 16.8 | -- | 18.6 | V | -- |
| Forward current | $I_F$ | -- | 100 | -- | mA | -- |
| Luminance(With LCD) | Lv | -- | 800 | -- | $cd/m^2$ | -- |
| LED life time | N/A | -- | 20,000 | -- | Hr | Note 1 |

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at $I_L$=20mA/LED. The LED life time could be decreased if operating $I_L$ is larger than 25mA/LED.

Backlight circuit diagram shown in below:

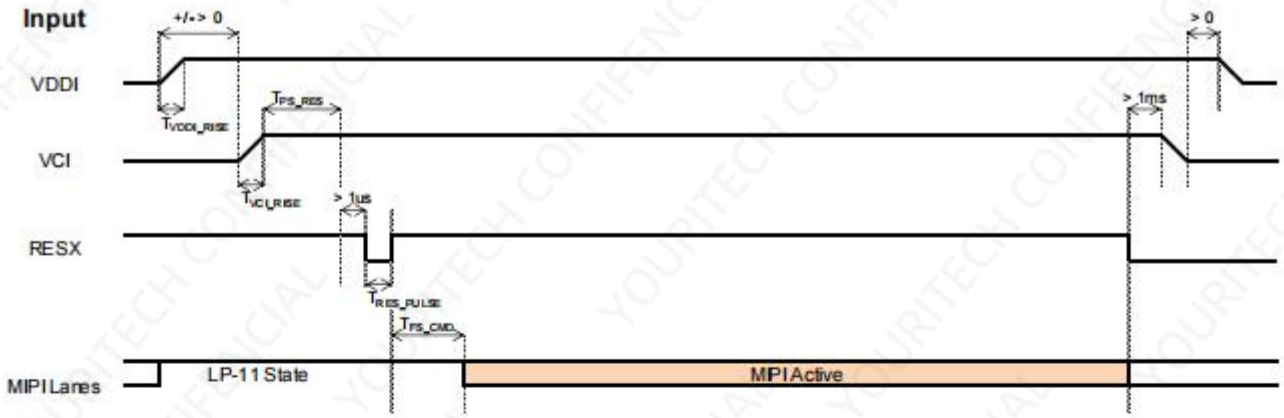


# 5. Module Function Description

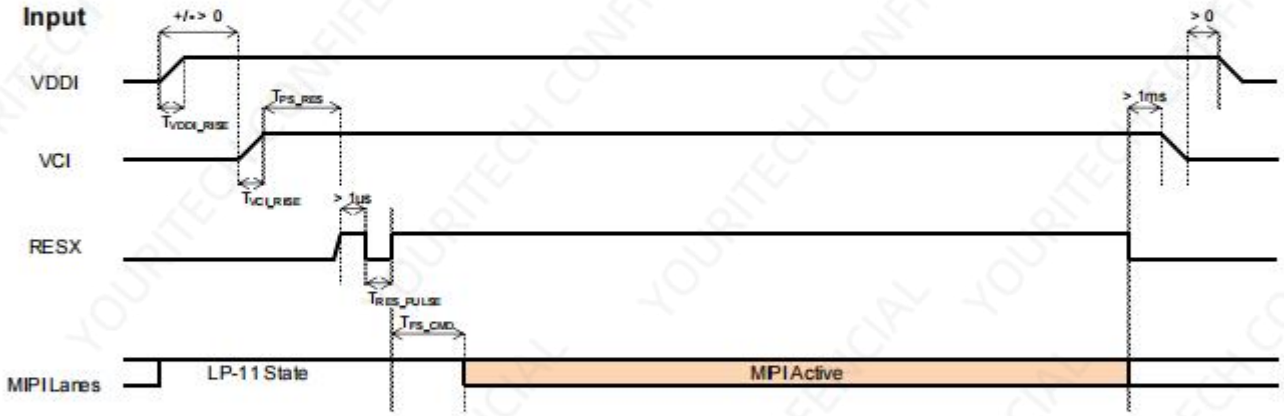
| Pin No. | Symbol | LCM Description |
|---|---|---|
| 1 | GND | Power Ground |
| 2 | VDD_3.3V | Power Supply For LCD. |
| 3 | IOV_ 1.8V | Power Supply For I/O. |
| 4 | GND | Power Ground |
| 5 | D3N | High speed interface data differential signal input/output pins |
| 6 | D3P | High speed interface data differential signal input/output pins |
| 7 | GND | Power Ground |
| 8 | D2N | High speed interface data differential signal input/output pins |
| 9 | D2P | High speed interface data differential signal input/output pins |
| 10 | GND | Power Ground |
| 11 | CLKN | High speed interface clock differential signal input/output pins |
| 12 | CLKP | High speed interface clock differential signal input/output pins |
| 13 | GND | Power Ground |
| 14 | D0N | High speed interface data differential signal input/output pins |
| 15 | D0P | High speed interface data differential signal input/output pins |
| 16 | GND | Power Ground |
| 17 | D1N | High speed interface data differential signal input/output pins |
| 18 | D1P | High speed interface data differential signal input/output pins |
| 19 | GND | Power Ground |
| 20 | LCD_ID | ID read PIN for ID circuit. |
| 21 | RST_ 1.8V | Reset signal input terminal. Active at ‘L’. |
| 22 | TE | Frame head pulse for tearing effect. |
| 23 | LEDK | Power supply for backlight cathode input terminal. |
| 24 | LEDK | Power supply for backlight cathode input terminal. |
| 25 | LEDK | Power supply for backlight cathode input terminal. |
| 26 | LEDK | Power supply for backlight cathode input terminal. |
| 27 | LEDA | Power supply for backlight anode input terminal. |
| 28 | LEDA | Power supply for backlight anode input terminal. |
| 29 | LEDA | Power supply for backlight anode input terminal. |
| 30 | LEDA | Power supply for backlight anode input terminal. |

# 6. Timing Characteristics

**Case A:**




**Case B:**




| Symbol | Characteristics | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $T_{VDDI\_RISE}$ | VDDI Rise time | 20 | - | - | us |
| $T_{VCI\_RISE}$ | Case A: VCI Rise time | 200 | - | - | us |
| | Case B: VCI Rise time | 40 | | | |
| $T_{PS\_RES}$ | VDDI/VCI on to Reset high | 5 | - | - | ms |
| $T_{RES\_PULSE}$ | Reset low pulse time | 10 | - | - | us |
| $T_{FS\_CMD}$ | Reset to first command | 10 | - | - | ms |

**Figure 106: Power on/off sequence with Power Mode 3**

## High Speed Mode – Data Clock Channel Timing

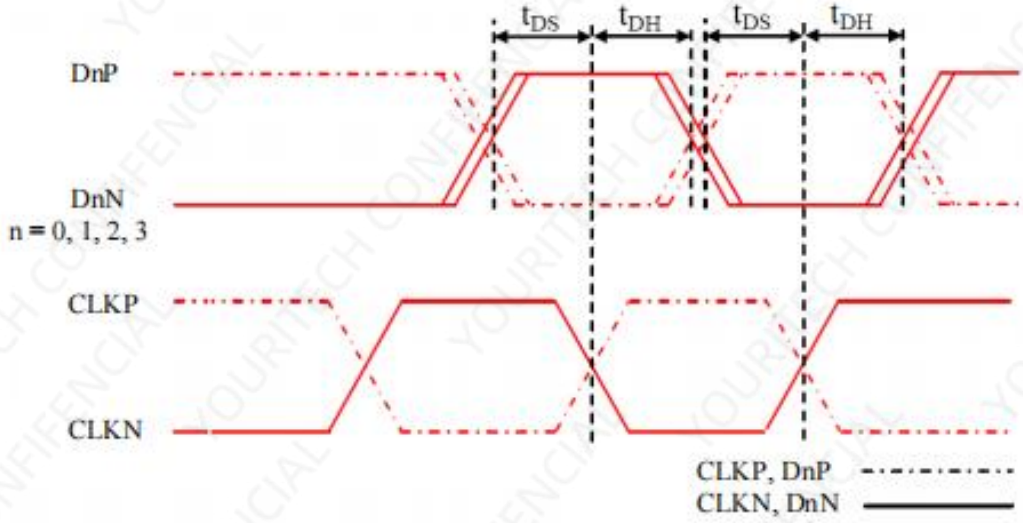



**Figure 118: DSI Data to Clock Channel Timings**

**Table 40: DSI Data to Clock Channel Timings**

| Signal | Symbol | Parameter | Min | Max |
|---|---|---|---|---|
| DnP/N , n=0 and 1 | $t_{DS}$ | Data to Clock Setup time | 0.15xUI | - |
| | $t_{DH}$ | Clock to Data Hold Time | 0.15xUI | - |

## Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

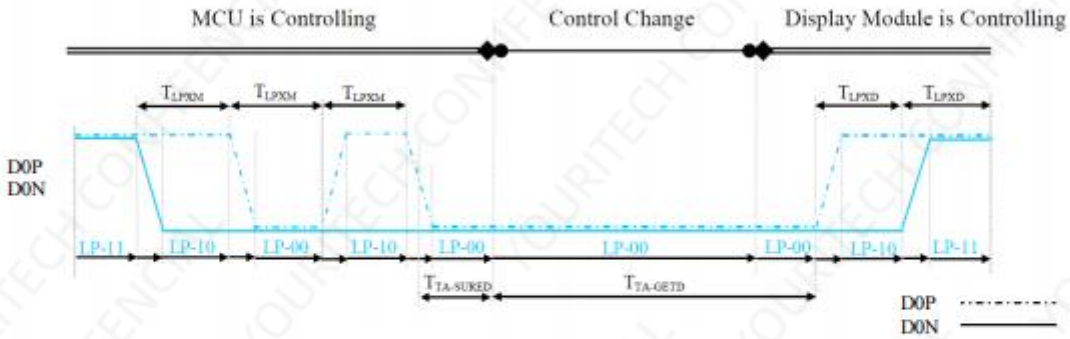



**Figure 120: BTA from the MCU to the Display Module**

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

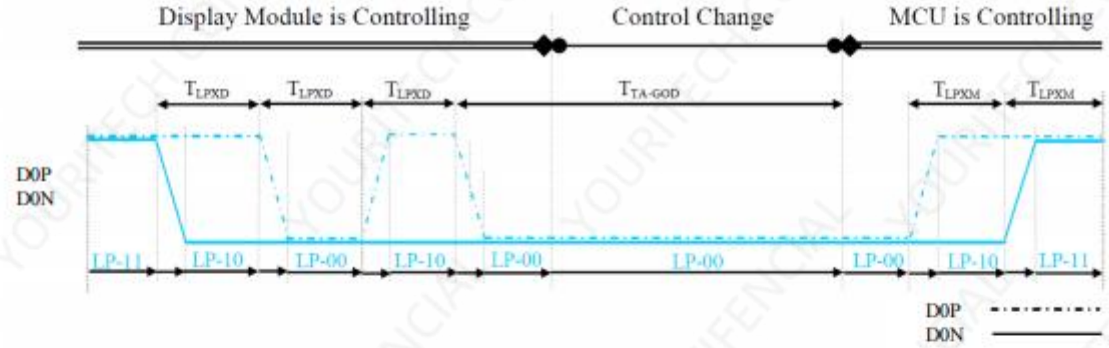



**Figure 121: BTA from the Display Module to the MCU**

**Table 42: Low Power State Period Timings – A**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| D0P/N | $T_{LPXM}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods<br>MCU → Display Module (ILI9881C) | 50 | 75 | ns |
| D0P/N | $T_{LPXD}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods<br>Display Module (ILI9881C) → MCU | 50 | 75 | ns |
| D0P/N | $T_{TA-SUREO}$ | Time-out before the Display Module (ILI9881C) starts driving | $T_{LPXD}$ | $2xT_{LPXD}$ | ns |

**Table 43: Low Power State Period Timings – B**

| Signal | Symbol | Description | Time | Unit |
|---|---|---|---|---|
| D0P/N | $T_{TA-GETO}$ | Time to drive LP-00 by Display Module (ILI9881C) | $5xT_{LPXD}$ | ns |
| D0P/N | $T_{TA-GOO}$ | Time to drive LP-00 after turnaround request - MCU | $4xT_{LPXD}$ | ns |

## DSI Clock Burst – High Speed Mode to/from Low Power Mode

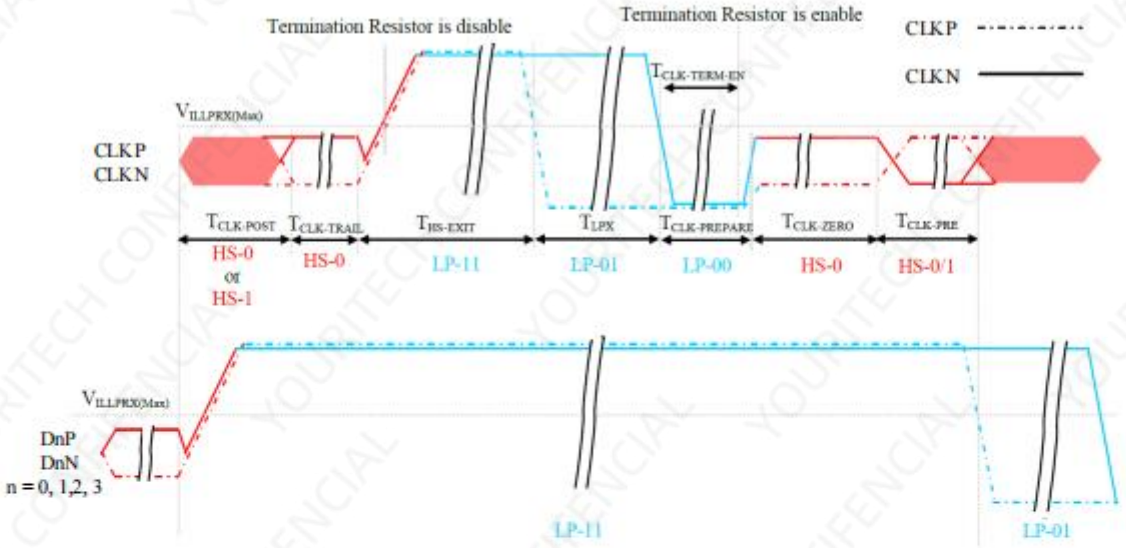



**Figure 124: Clock Lanes - High Speed Mode to/from Low Power Mode Timings**

**Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| CLKP/N | $T_{CLK-POST}$ | Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode | 60+52xUI | - | ns |
| CLKP/N | $T_{CLK-TRAIL}$ | Time to drive HS differential state after last payload clock bit of a HS transmission burst | 60 | - | ns |
| CLKP/N | $T_{HS-EXIT}$ | Time to drive LP-11 after HS burst | 100 | - | ns |
| CLKP/N | $T_{CLK-PREPARE}$ | Time to drive LP-00 to prepare for HS transmission | 38 | 95 | ns |
| CLKP/N | $T_{CLK-TERM-EN}$ | Time-out at Clock Lane to enable HS termination | - | 38 | ns |
| CLKP/N | $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | Minimum lead HS-0 drive period before starting Clock | 300 | - | ns |
| CLKP/N | $T_{CLK-PRE}$ | Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode | 8xUI | - | ns |

## Reset Timing

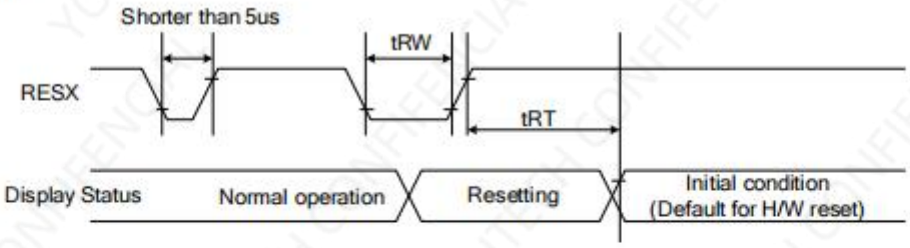



**Figure 125: Reset Timing**

**Table 47: Reset Timing**

| Signal | Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| RESX | tRW | Reset pulse duration | 10 | | uS |
| | tRT | Reset cancel | | 5 (note 1,5) | mS |
| | | | | 120 (note 1,6,7) | mS |

***Notes:***

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

**Table 48: Reset Descript**

| RESX Pulse | Action |
|---|---|
| Shorter than 5us | Reset Rejected |
| Longer than 10us | Reset |
| Between 5us and 10us | Reset starts |

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

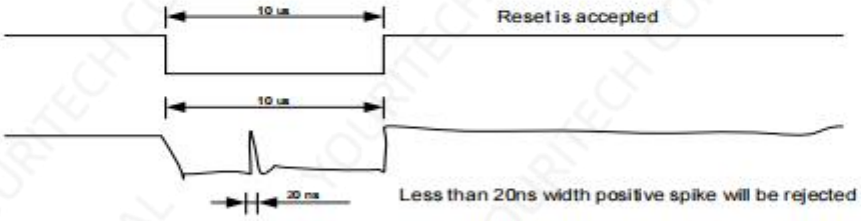



**Figure 126: Positive Noise Pulse during Reset Low**

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

## 7.Optical Characteristics

| Item | | Symbol | Conditions | Specifications | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| Transmittance (without DBEF) | | T% | Viewing normal angle $\theta_x = \theta_y = 0$ | | 3.5 | -- | % | All left side data are based on INX's following condition (at 25 ℃)<br>1.LC : AAS<br>2.Light Source : INX BLU Spectrum.<br>3.CF / TFT side Film : SRW062APN1HC5 / SRW062APN1<br>4.Machine : DMS 803 (Cono Scope for View Angle)<br>5. VLC white > 4.5 V<br>VLC dark < 0.2 V |
| Contrast Ratio | | CR | | 600 | 1000 | -- | -- | |
| Response Time | | $T_{on}+T_{off}$ | | -- | 25 | 35 | ms | |
| Viewing Angle | Hor. | $\theta_{x+}$ | CR ≧10 at 25 ℃ | 75 | 80 | -- | deg. | |
| | | $\theta_{x-}$ | | 75 | 80 | -- | | |
| | Ver. | $\theta_{y+}$ | | 75 | 80 | -- | | |
| | | $\theta_{y-}$ | | 75 | 80 | -- | | |
| CF Only Color Chromaticity (CIE1931) | Red | $X_R$ | Viewing normal angle $\theta_x = \theta_y = 0$ at 25 ℃ | | | | -- | Under C light simulation |
| | | $Y_R$ | | | | | | |
| | Green | $X_G$ | | | | | | |
| | | $Y_G$ | | | | | | |
| | Blue | $X_B$ | | | | | | |
| | | $Y_B$ | | | | | | |
| | White | $X_W$ | | 0.274 | 0.294 | 0.314 | | |
| | | $Y_W$ | | 0.294 | 0.314 | 0.334 | | |
| Color Gamut | | CG | | 60 | 68 | -- | % | |

*Note (1)Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

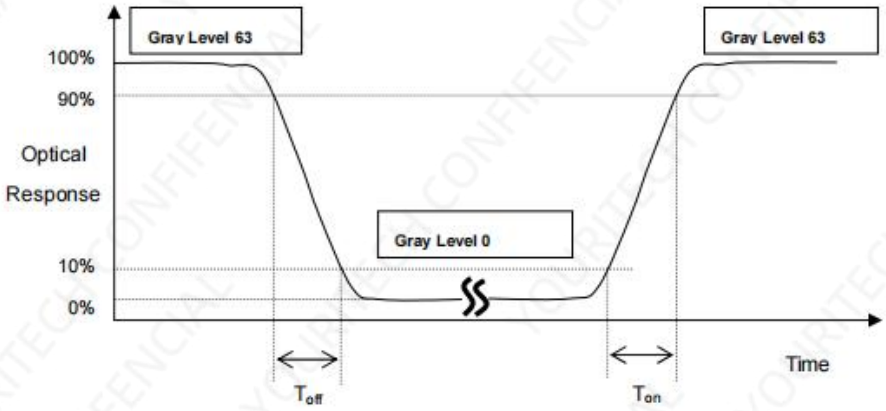
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

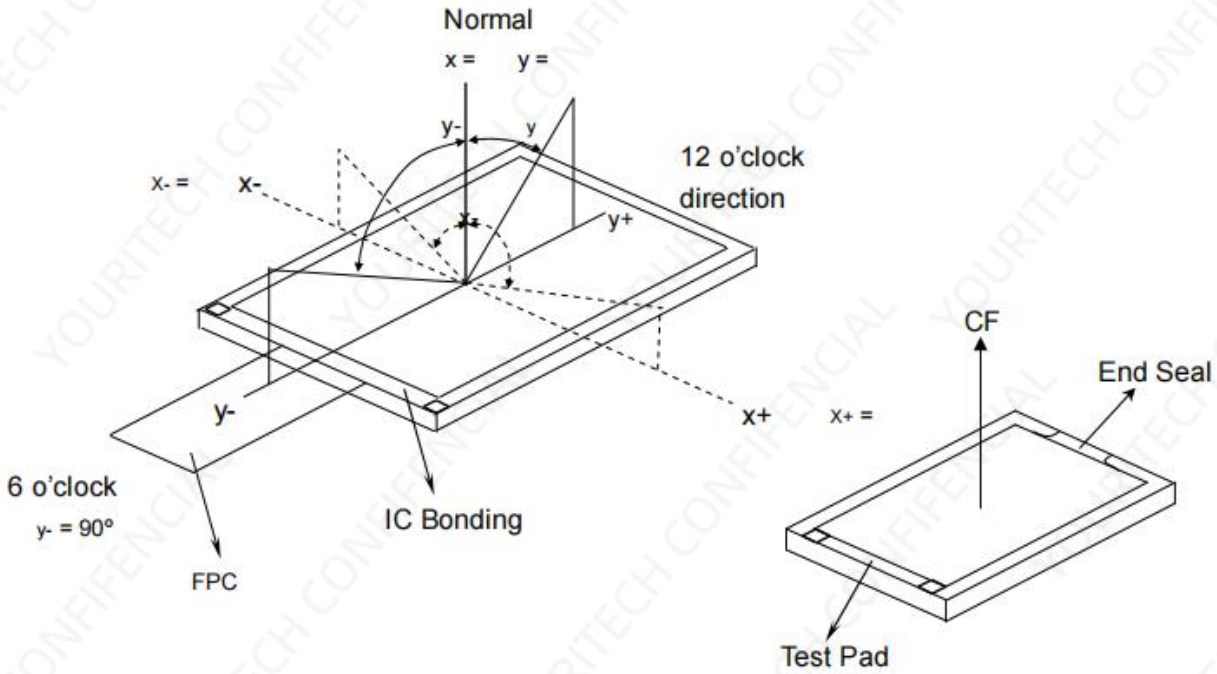
CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

*Note (2) Definition of Response Time ($T_{on}$, $T_{off}$):

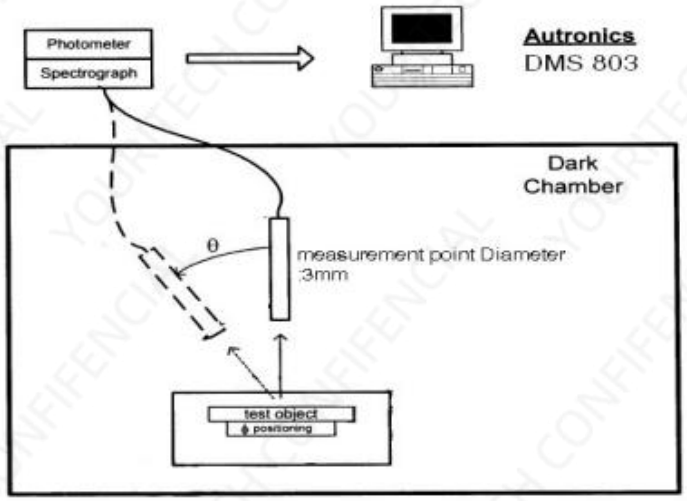



*Note(3) Definition of Viewing Angle

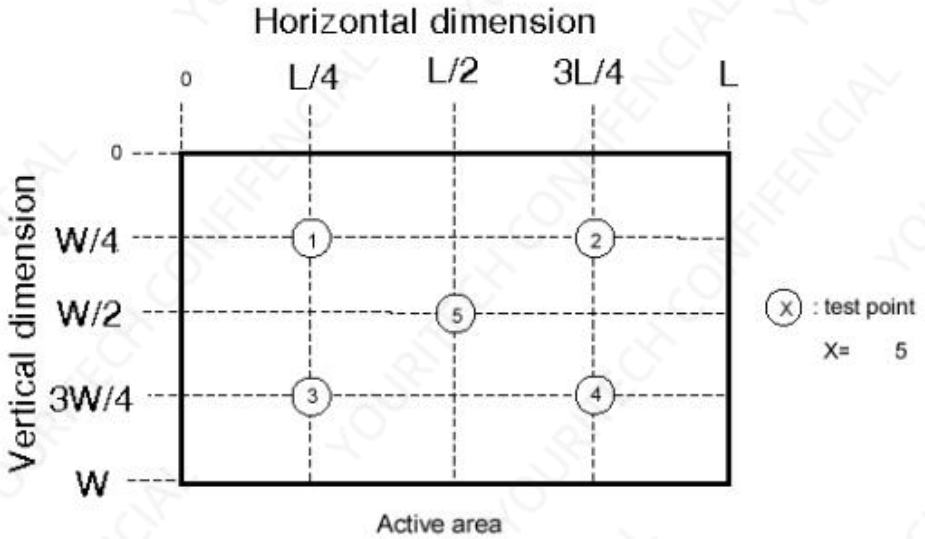


*Note (4) Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.




*Note (5)



## 8. Reliability Test Item

| No. | Test Item | Test Condition | Notes |
|---|---|---|---|
| 1 | High Temp. Storage | +80°C / 96H | 1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow. |
| 2 | Low Temp. Storage | -30°C / 96H | |
| 3 | High Tempe. Operating | +60°C / 96H | |
| 4 | Low Tempe. Operating | -20°C / 96H | |
| 5 | High Temperature /Humidity storage | 60°C x 90%RH / 96H | |
| 6 | Thermal and cold shock | Static state，-30℃（30min）~80℃（30min），10 cycles | |

## 9. Packing Method----TBD

- END -