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Project No. 项目编号	ET057VG01-T
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	**Standard LCD Module** **TFT：640*RGBx480Dots** **5.7”TFT LCD**

客户确认Customer Approval	
项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	

PREPARED BY	CHECKED BY	APPROVED BY

1. Introduction

1.1 Scope of application

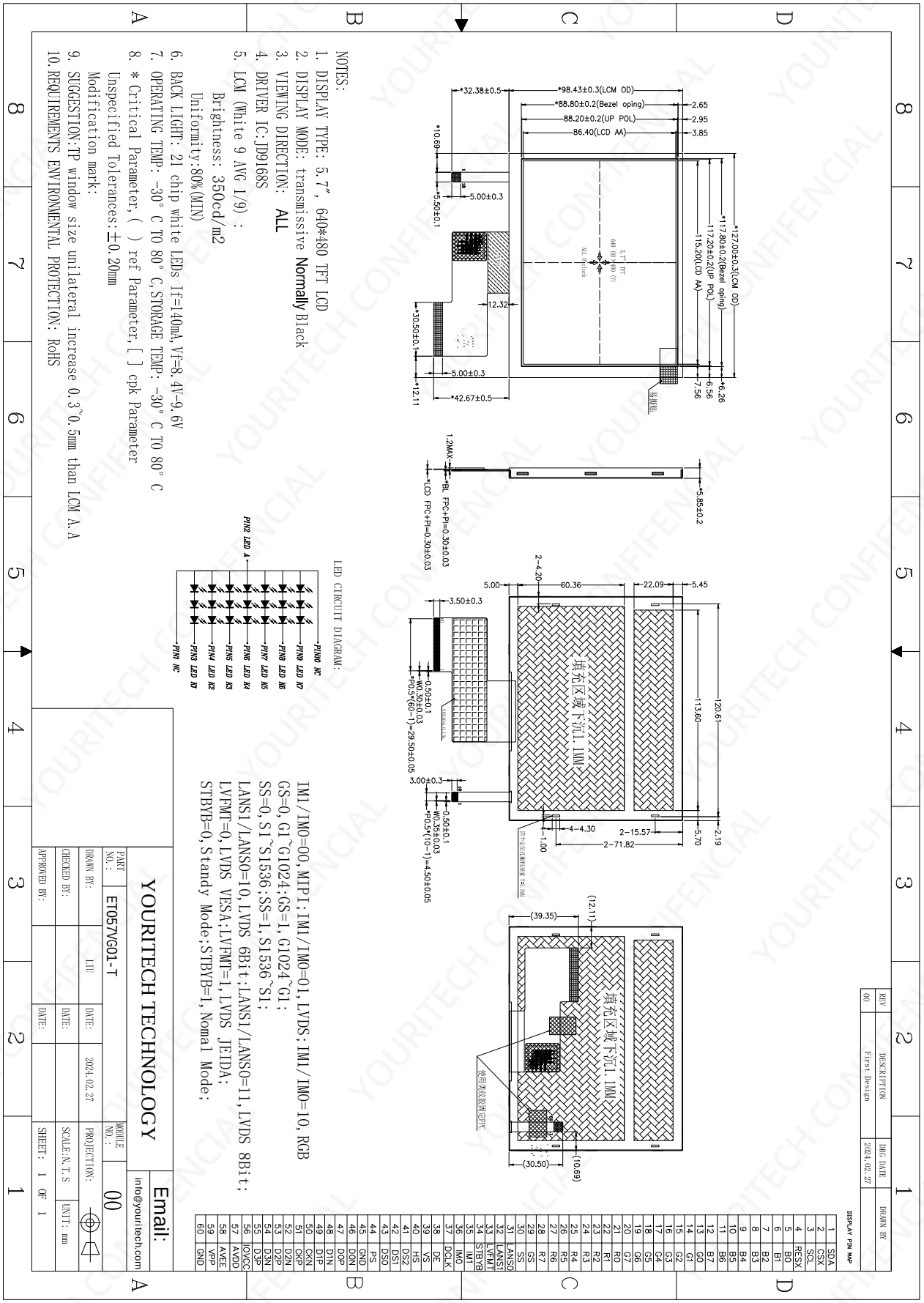
This specification applies to the LCD module that is supplied by YOURITECH Technology .
LCD specification: Dots 640xRGBx480
As to basic specification of the driver IC, refer to the IC (JD9168S) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC1+BL;
ALL O'CLOCK Type LCD
640 dot-segment and 480 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
RGB or LVDS or MIPI interface

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	640*3RGB(H)X480(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.18 (H) x 0.18 (V)	mm
Active area	115.20(H) x 86.40(V)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	JD9168S	--
TFT interface	RGB or LVDS or MIPI Interface	--
Module Size(W*H*T)	127.00(W) ×98.43(H) ×5.85(T)	mm
Approx. Weight	TBD	g
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--


NOTES:
1. DISPLAY TYPE: 5.7", 640*480 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL
4. DRIVER IC:JD9168S
5. LCM (White 9 AVG 1/9) :
Brightness: 350cd/m2
Uniformity:80%(MIN)
6. BACK LIGHT: 21 chip white LEDs If=140mA, Vf=8.4V~9.6V
7. OPERATING TEMP: -30° C TO 80° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
Unspecified Tolerances:±0.20mm
Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS
LED CIRCUIT DIAGRAM:
IM1/IM0=00,MIPI;IM1/IM0=01,LVDS;IM1/IM0=10,RGB
GS=0,G1~G1024;GS=1,G1024~G1;
SS=0,S1~S1536;SS=1,S1536~S1;
LANS1/LANS0=10,LVDS 6Bit;LANS1/LANS0=11,LVDS 8Bit;
LVFMT=0,LVDS VESA;LVFMT=1,LVDS JEIDA;
STBYB=0,Standy Mode;STBYB=1,Nomal Mode;
DISPLAY PIN MAP
REV
DESCRIPTION
DRG DATE
DRAWN BY
00
First Design
2024.02.27
YOURITECH TECHNOLOGY
Email:
info@youritech.com
PART NO.:
ET057VG01-T
MODULE NO.:
00
DRAWN BY:
LIU
DATE:
2024.02.27
PROJECTION:
CHECKED BY:
DATE:
SCALE:N.T.S
UNIT: mm
APPROVED BY:
DATE:
SHEET: 1 OF 1

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-30	+80	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Parameter		Symbol	Values			Unit	Notes
			Min.	Typ.	Max.		
Power Supply Input Voltage		IOVCC	2.5	3.3	3.3	V	Ta = 25 ℃ Note 1
		VSP	4.5	5.5	6.0	V	
		VSN	-4.5	-5.5	6.0	V	
Current Consumption	Operating	IOVCC	5	5.09	6.1	mA	@L255
		VSP	9.2	9.49	11.4	mA	
		VSN	8.25	8.44	10.1	mA	
		Power	112.5	115.5	138.5	mA	
	Sleep in	IOVCC	-	0.45	-	mA	
		VSP	-	0.0068	-	mA	
		VSN	-	0.065	-	mA	
		Power	-	1.88	-	mW	

4.2 Back-Light Unit Characeristics

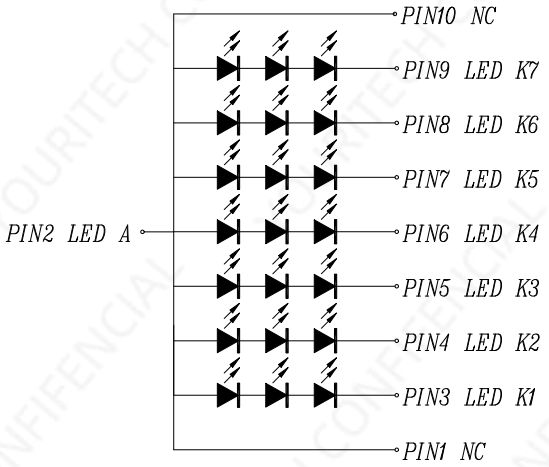
The back-light system is an edge-lighting type with 21 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	8.4	--	9.6	V	--
Forward current	I_F	--	140	--	mA	--
Luminance(With LCD)	Lv	--	350	--	cd/m^2	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

(1) The "LED life time" is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:

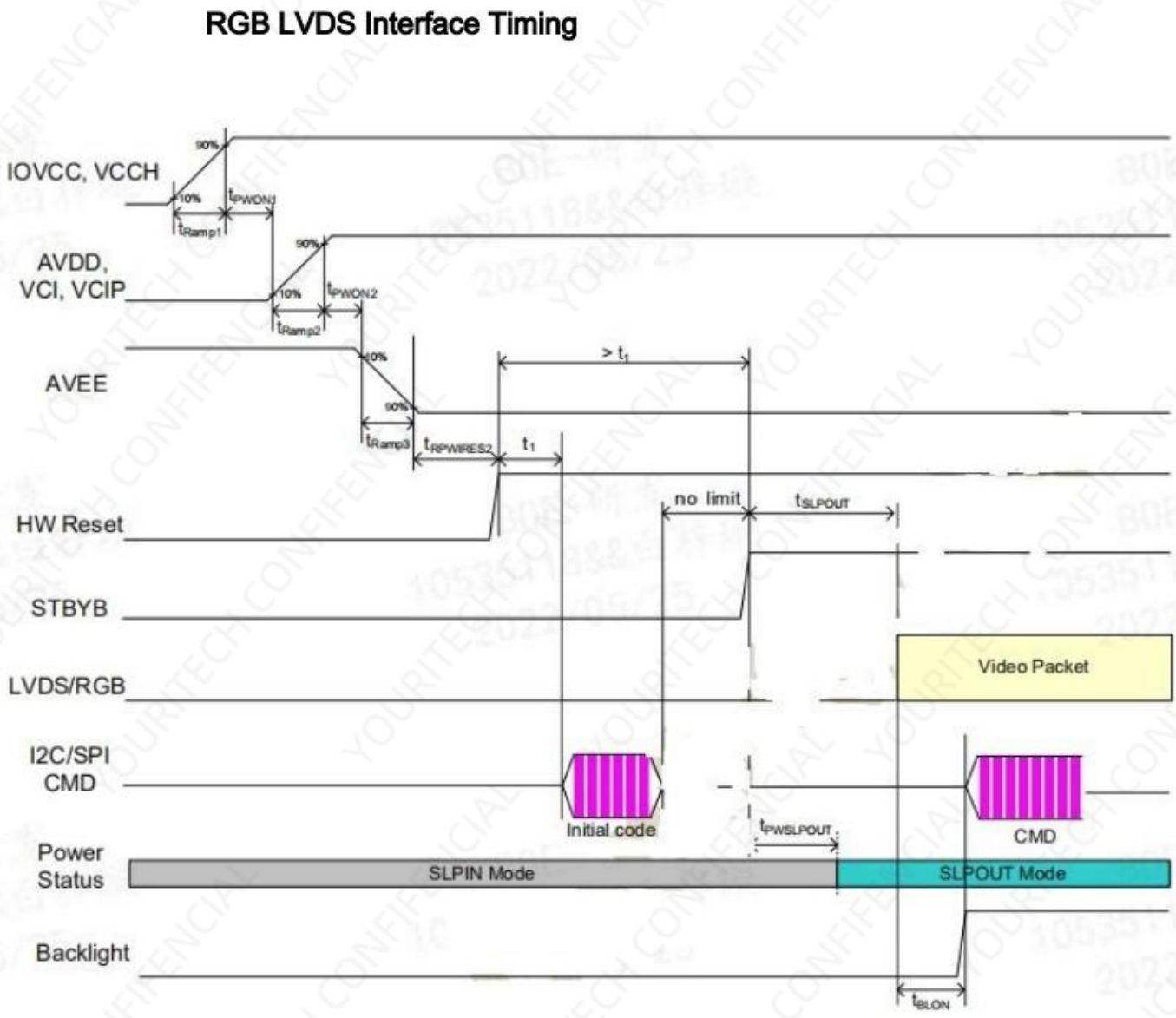


5. Module Function Description

Pin NO.	Pin name	Description	Pin NO.	Pin name	Description	Pin NO.	Pin name	Description	Pin NO.	Pin name	Description
1	SDA	SPI data	16	G3	RGB data	31	LAN0	lane mode	46	D0N	LVDS D0N
2	CSX	Chip select	17	G4	RGB data	32	LAN1	lane mode	47	D0P	LVDS D0P
3	SCL	SPI clock	18	G5	RGB data	33	LVFMT	LVDS data for mat	48	D1N	LVDS D1N
4	RESX	Reset	19	G6	RGB data	34	STBYB	standy mode	49	D1P	LVDS D1P
5	B0	RGB data	20	G7	RGB data	35	IM1	IF mode slect	50	CKN	LVDS CKN
6	B1	RGB data	21	R0	RGB data	36	IM0	IF mode slect	51	CKP	LVDS CKP
7	B2	RGB data	22	R1	RGB data	37	DCLK	RGB clock	52	D2N	LVDS D2N
8	B3	RGB data	23	R2	RGB data	38	DE	RGB data enable	53	D2P	LVDS D2P
9	B4	RGB data	24	R3	RGB data	39	VS	RGB V-sync	54	D3N	LVDS D3N
10	B5	RGB data	25	R4	RGB data	40	HS	RGB H-sync	55	D3P	LVDS D3P
11	B6	RGB data	26	R5	RGB data	41	DS2	data lane seq	56	IOVCC	Power
12	B7	RGB data	27	R6	RGB data	42	DS1	data lane seq	57	AVDD	Power
13	G0	RGB data	28	R7	RGB data	43	DS0	data lane seq	58	AVEE	Power
14	G1	RGB data	29	GS	gate scan	44	PS	data lane seq	59	VPP	OTP power
15	G2	RGB data	30	SS	source scan	45	GND	Ground	60	GND	Ground

IM1/IM0=00,MIPI;IM1/IM0=01,LVDS;IM1/IM0=10,RGB
GS=0,G1~G1024;GS=1,G1024~G1;
SS=0,S1~S1536;SS=1,S1536~S1;
LANS1/LANS0=10,LVDS 6Bit;LANS1/LANS0=11,LVDS 8Bit;
LVFMT=0,LVDS VESA;LVFMT=1,LVDS JEIDA;
STBYB=0,Standy Mode;STBYB=1,Nomal Mode;

6. Timing Characteristics

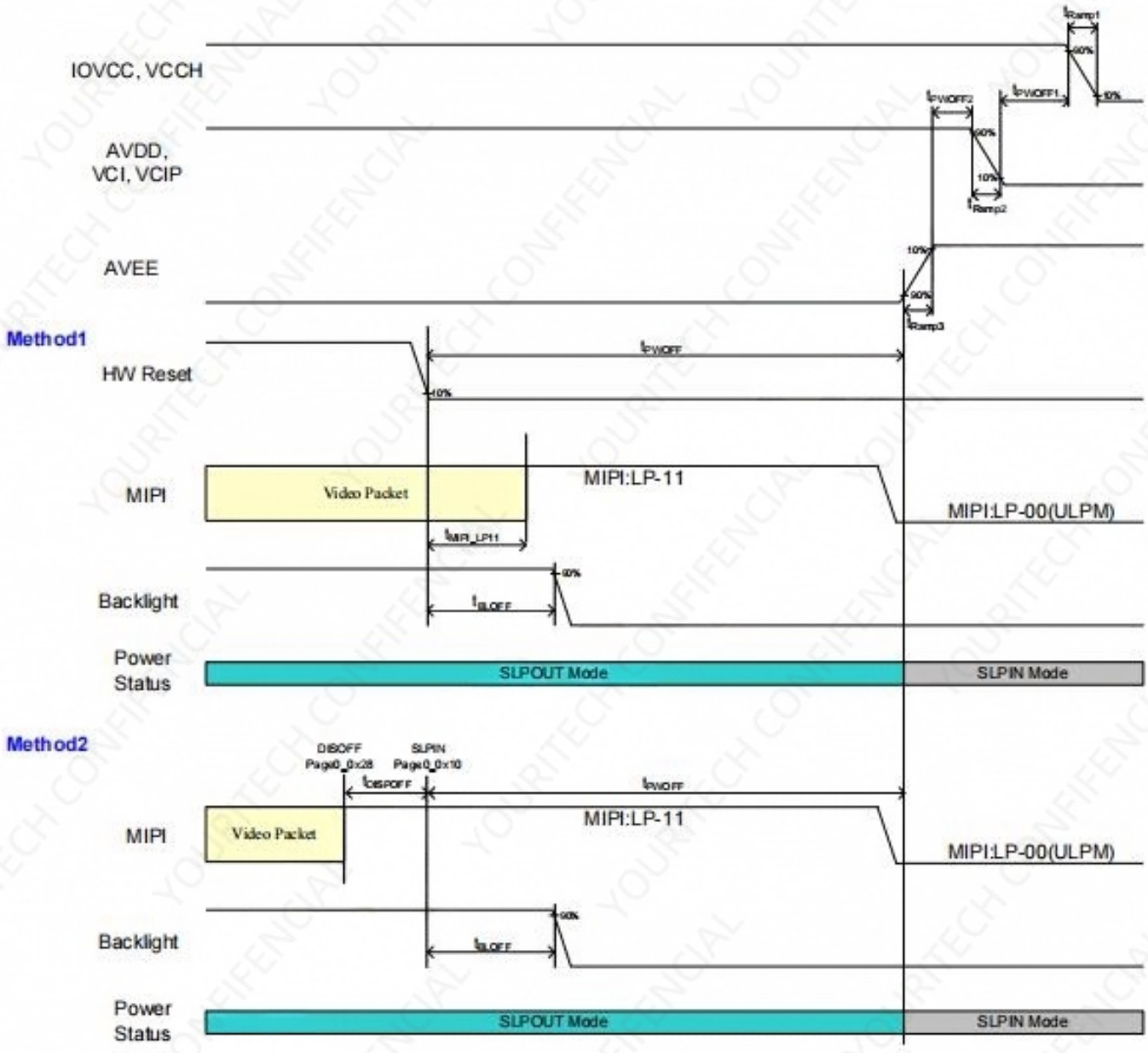


MIPI Interface Timing

input power mode (EXT_VGL=0, BOOSTM [1:0]=01)

- External IOVCC, AVDD, AVEE Power.
- IOVCC=VCCH=2.5~3.3V, VCI=VCIP=AVDD=4.5~5.5V, AVEE=-4.5~-5.5V.

power mode power off sequence – DSI:



6. DC characteristics

6.1. RGB Interface DC electrical characteristics

(T_A=-40 ~ 85 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VCI	V_{IN}	Analog Supply Voltage	2.5	-	6.0	
IOVCC	V_{IN}	Interface Supply Voltage	2.5	-	3.3	
AVDD	V_{IN}	Analog Supply Voltage	4.5	-	6.0	
AVEE	V_{IN}	Analog Supply Voltage	2.5	-	6.0	
VCCH	V_{IN}	High speed interface Supply Voltage	2.5	-	3.3	
Input high voltage	V_{IH}	IOVCC= 2.5 ~ 3.3V VCIP= 2.5 ~ 6.0V VCI= 2.5 ~ 6.0V	0.7 x IOVCC	-	IOVCC	V
Input low voltage	V_{IL}		0	-	0.3 x IOVCC	V
Output high voltage (SDA, GPIO)	V_{OH1}	I_{OH} = -1.0 mA	0.8 x IOVCC	-	IOVCC	V
Output low voltage (SDA, GPIO)	V_{OL1}	IOVCC= 2.5 ~ 3.3V I_{OL} = 1.0 mA	0	-	0.2 x IOVCC	V
Logic High level input current	I_{IH}	VSYNC, HSYNC	-	-	1	µA
		RESX, SCL, CSX,	-	-	1	µA
	I_{IHD}	DB[23...0], SDA	-	-	1	µA
		DB[23...0]	-	-	1	µA
Logic Low level input current	I_{IL}	VSYNC, HSYNC	-1	-		µA
		RESX, CSX, SCL	-1	-		µA
	I_{ILD}	DB[23...0], SDA	-1	-		µA
		DB[23...0]	-1	-		µA
Current consumption standby mode (VCIP/VCI-VSSD)	$I_{ST(VDD)}$	VCI/VCCH=3.3V, IOVCC=3.3V T_A =25°C	-	TBD	-	µA
Current consumption standby mode (IOVCC– VSSD)	$I_{ST(IOVCC)}$		-	TBD	-	µA
Current consumption during Deep-standby mode (VCIP/VCI-VSSD)	$I_{DP-ST(VDD)}$	VCI/VCCH=3.3V, IOVCC=3.3V T_A =25°C	-	TBD	-	µA
Current consumption during Deep-standby mode (IOVCC– VSSD)	$I_{DP-ST(IOVCC)}$		-	TBD	-	µA

Table 11.2: RGB Interface DC characteristic

6.2. LVDS DC electrical characteristics

(T_A=-40 ~ 85 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential input high threshold voltage	Rx_{VTH}	Rx_{VCM}=1.2V	+0.1	+0.2	+0.3	V
Differential input low threshold voltage	Rx_{VTL}		-0.3	-0.2	-0.1	V
Input voltage range (singled-end)	Rx_{VIN}		0.7	-	1.7	V
Differential input common mode voltage	Rx_{VCM}	|VID|=0.2	1	1.2	1.4	V
Differential input impedance	ZID		80	100	125	ohm
Differential input voltage	|VID|		0.2	-	0.6	V
Differential input leakage current	I_{LCLVDS}		-10	-	+10	uA
LVDS Digital Stand-by Current	I_{STLVDS}	Clock & all Functions are stopped	-	TBD	-	uA

Table 11.3: LVDS DC characteristic

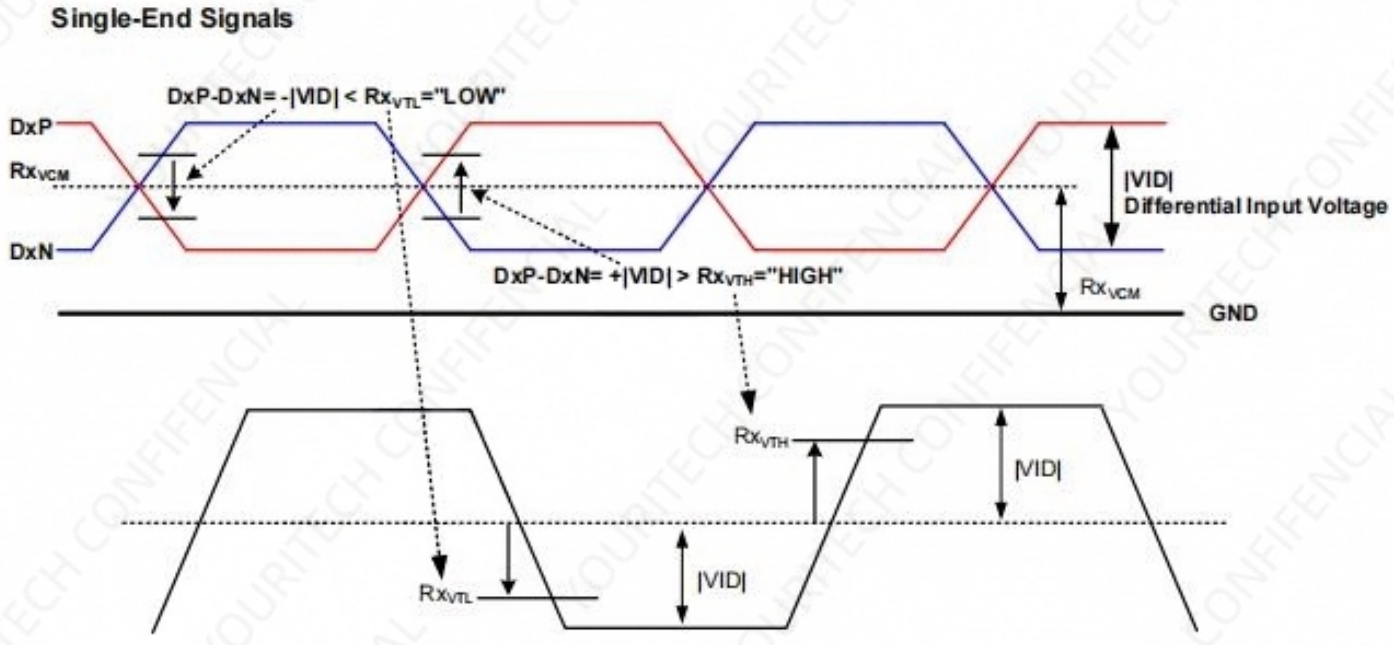


Figure 11.1: LVDS input timings

6.3.SPI electronic characteristics

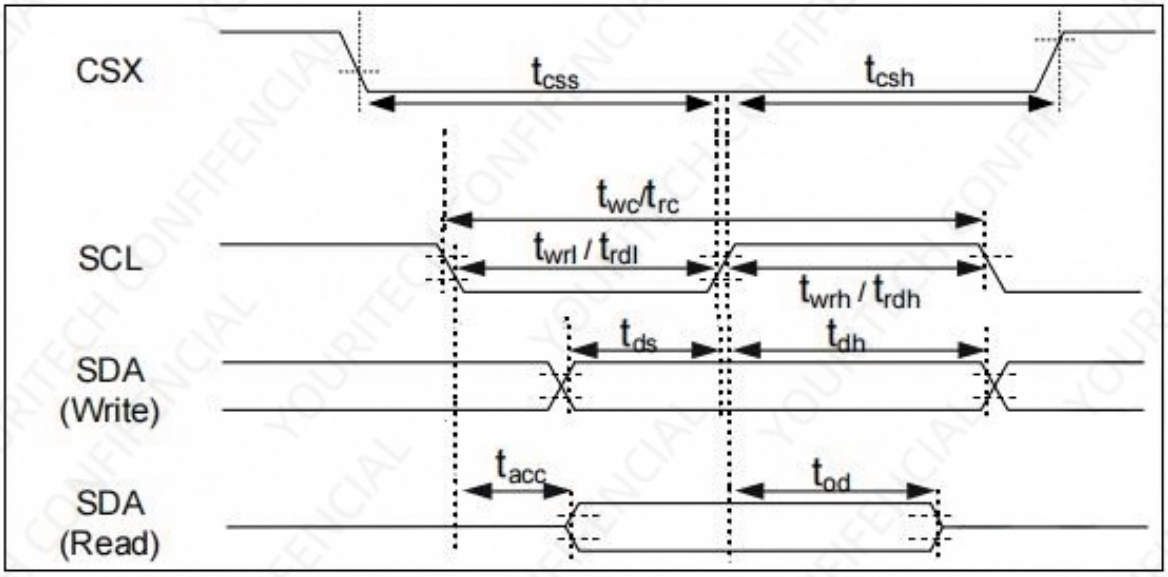


Figure 11.3: SPI interface AC characteristics

(T_A=25°C, IOVCC=3.3V, VCI=3.3V)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{css} t_{csh}	Chip select setup time (Write) Chip select setup time (Read)	40 40	- -	ns	-
SCL (Write)	t_{wc} t_{wrh} t_{wrl}	Write cycle Control pulse "H" duration Control pulse "L" duration	100 40 40	- - -	ns	-
SCL (Read)	t_{rc} t_{rdh} t_{rdl}	Read cycle Control pulse "H" duration Control pulse "L" duration	150 60 60	- - -	ns	-
SDA (Write)	t_{ds} t_{dt}	Data setup time Data hold time	30 30	- -	ns	Note(1)
SDA (Read)	t_{acc} t_{od}	Read access time Output disable time	- 10	35 50	ns	

Note: (1) For maximum C_L=30pF, for minimum C_L=8pF.
(2) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(3) Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Table 11.5: SPI interface AC characteristics

6.4. LVDS electronic characteristics

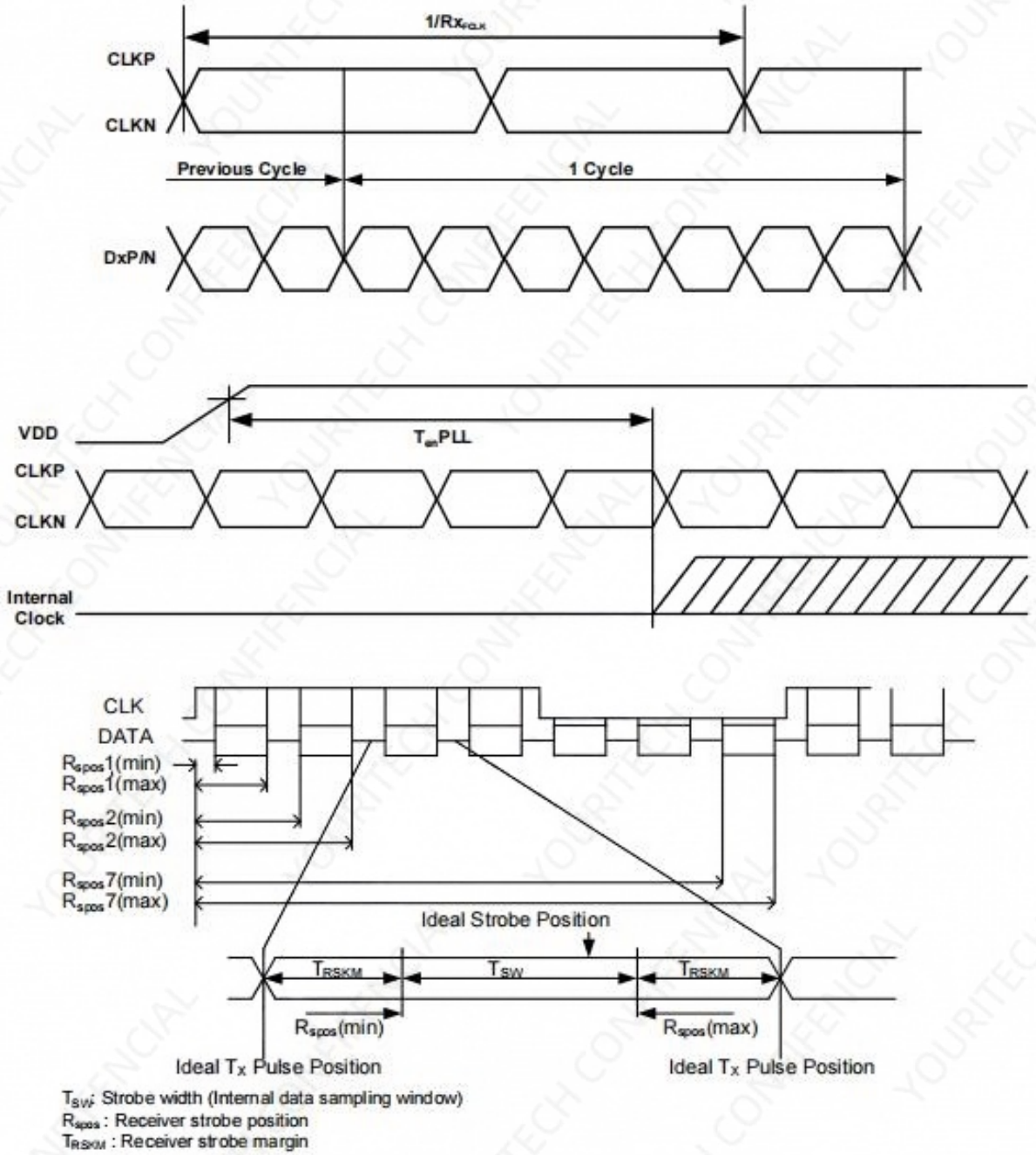


Figure 11.4: LVDS AC characteristics

Signal	Symbol	Min.	Typ	Max.	Unit	Description
Clock frequency	Rx_{FCLK}	30	-	75	MHz	-
Input data skew margin	T_{RSKM}	500	-	-	ps	|VID| = 200mV RxVCM = 1.2V @Rx_{FCLK}=75MHz
Clock high time	T_{LVCH}	-	4/(7 x Rx_{FCLK})	-	ns	-
Clock low time	T_{LVCL}	-	3/(7xRx_{FCLK})	-	ns	-
PLL wake-up time	T_{enPLL}	-	-	150	us	-

Table 11.6: LVDS AC characteristics

Burst Mode Data Transmission

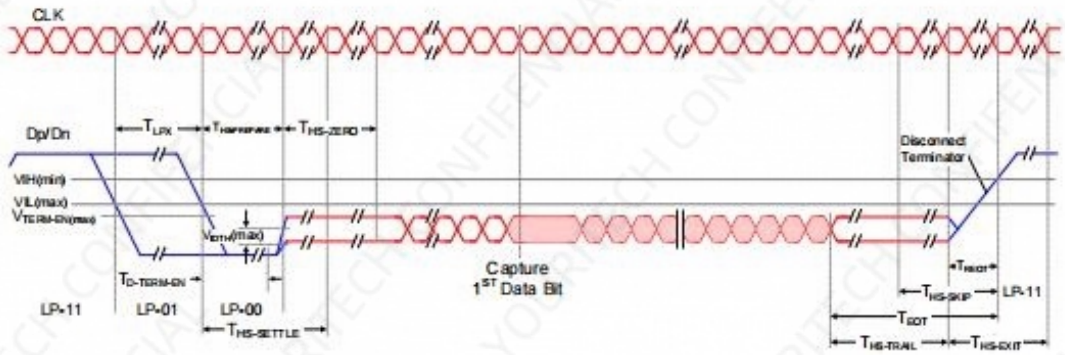


Figure 11.10: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	Max(n*8*UI, 60+n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

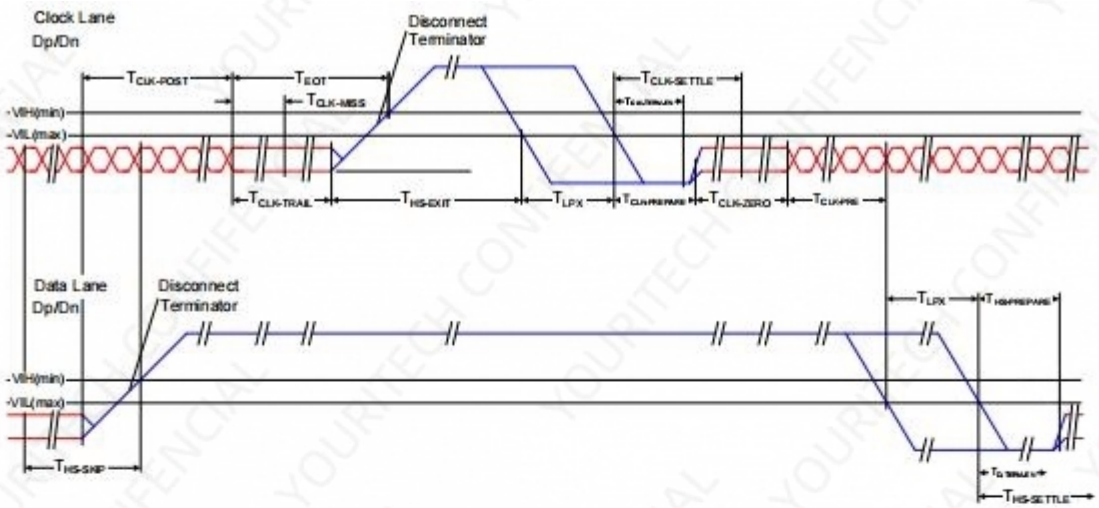
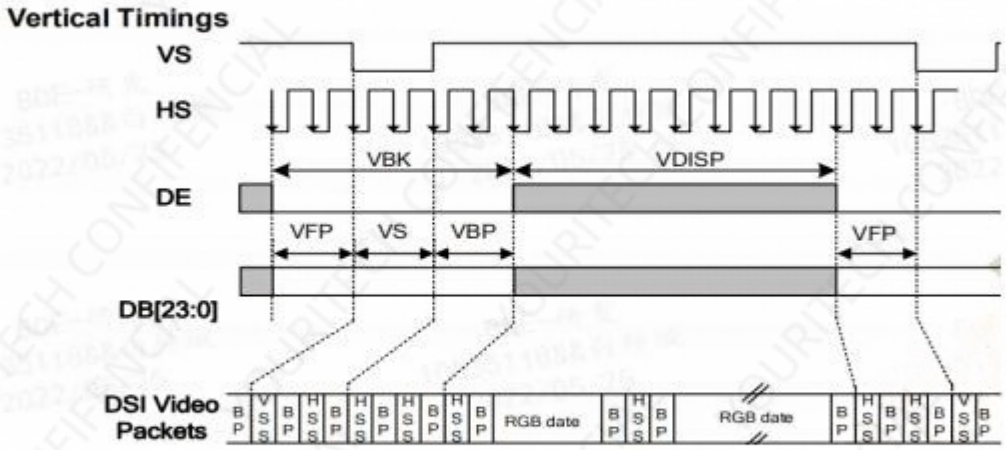


Figure 11.11: Switching the Clock Lane between Clock Transmission and Low-Power Mode

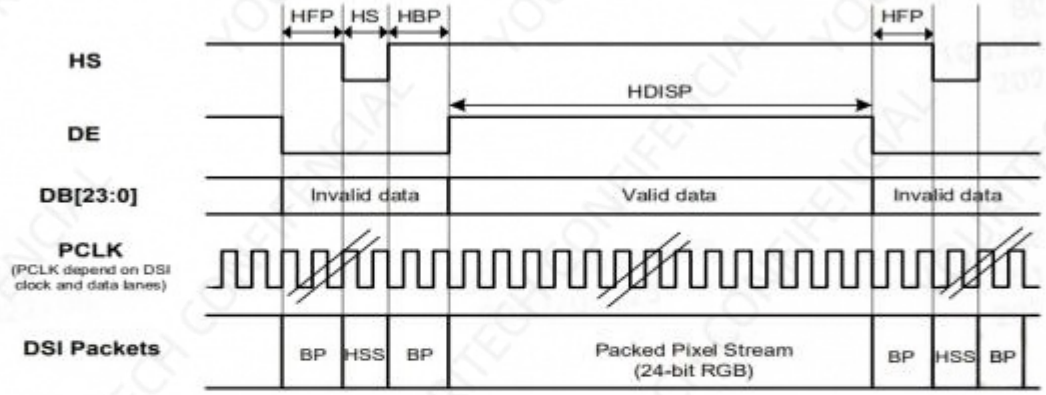
Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

RGB Interface Timing

< Figure 4. Timing Chart of Signals in RGB Interface >



Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	480	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz



Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	100			ns
Horizontal back porch	HBP	-	100			ns
Horizontal front porch	HFP	-	400			ns
Horizontal blanking period	HBLK	HS+HBP+HFP		900(1)		ns
Horizontal active area	HDISP	800 pixels	-	12(2)	-	us

Remark : Porch setting is related to MCU PCLK and Frames

Reset Description:

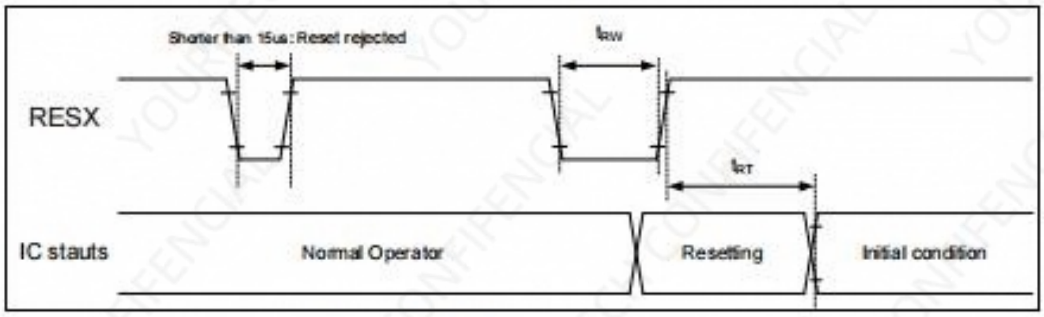


Figure 11.2: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset "L" pulse width(2)	RESX	20	-	µs
t_{RT}	Reset complete time(3)	-	-	5(5)	ms
		-	-	120(6) (7) (8)	ms

Note:

(1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset complete time (t_{RT}) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 15 µs	Reset Rejected
Longer than 20 µs	Reset
Between 15 µs and 20 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for HW reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:

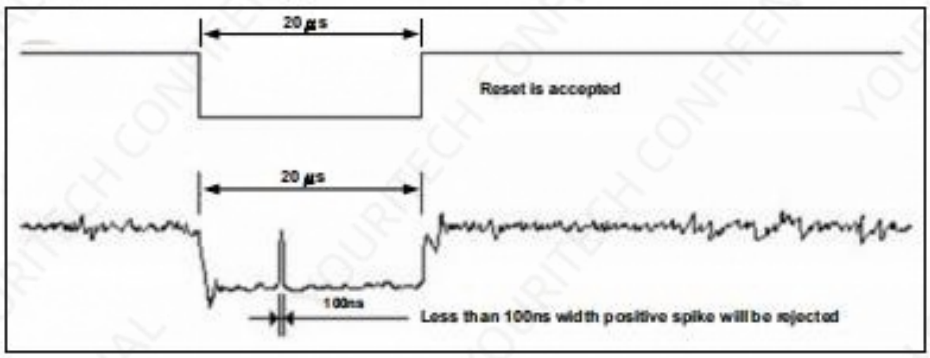


Table 11.4: Reset timings

(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out command, it is necessary to wait 120msec then send RESX.

7.Optical Characteristics

Optical Specification

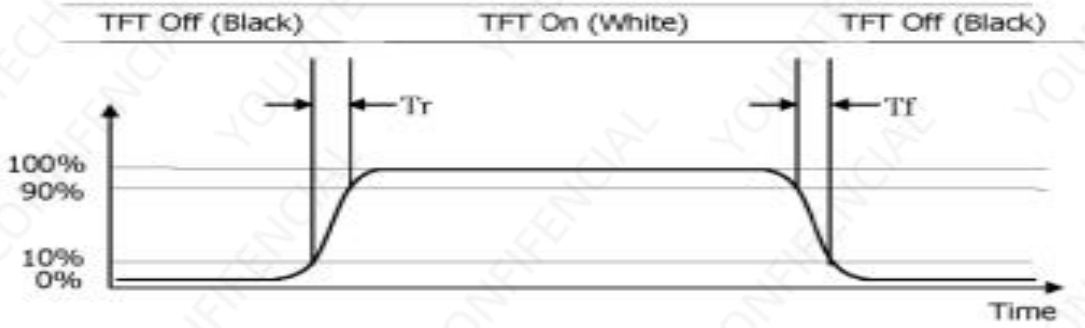
Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	Note 1
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Luminance Contrast ratio		CR	Θ = 0°	1000	1200	-		Note 2 POL使用HC/Clear BLU使用双层棱镜
Color Gamut	NTSC	CIE1931	Θ = 0°	60	65	-	%	@C Light
Reproduction of color	White	Wx	Θ = 0°	Typ -0.03	0.308	Typ +0.03	-	Note 3/4
		Wy			0.344		-	
	Red	Rx	Θ = 0°	Typ -0.03	0.650	Typ +0.03	-	
		Ry			0.340		-	
	Green	Gx	Θ = 0°	Typ -0.03	0.293	Typ +0.03	-	
		Gy			0.598		-	
	Blue	Bx	Θ = 0°	Typ -0.03	0.137	Typ +0.03	-	
		By			0.157		-	
Response Time		Tr+Td	Ta= 25° C Θ = 0°	-	30	35	ms	Note 5
Cross Talk		CT	Θ = 0°	-	-	2.0	%	

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 4 for a total of the measurements per display.
4. The color chromaticity coordinates specified in Table 5. shall be calculated from the spectral data measured with C light. Measurements shall be made at the center of the panel.
5. The electro-optical response time measurements shall be made as FIGURE 5 shown in Appendix by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Td, and 90% to 10% is Tr.



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+80°C / 96H	
4	Low Tempe. Operating	-30°C / 96H	
5	High Temperature /Humidity storage	60°C x 90%RH /96H	
6	Thermal and cold shock	Static state， -30℃（30min） ~80℃（30min），10 cycles	