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Project No. 项目编号	ET060FH05-TT
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	**Standard LCD Module** **TFT：1080*RGBx1920Dots** **6.0”TFT LCD+CG**

客户确认Customer Approval	
项目负责人Project Manager	
品质主管Director of Quality	
采购工程师Purchasing Engineer	

PREPARED BY	CHECKED BY	APPROVED BY

1. Introduction

1.1 Scope of application

This specification applies to the LCD module that is supplied by YOURITECH TECHNOLOGY Technology CO., LTD.

LCD specification: Dots 1080xRGBx1920.

As to basic specification of the driver IC, refer to the IC (FT8725) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

Structure: TFT PANNEL+IC +FPC+BL+CG;

IPS Type LCD

1080dot-segment and 1920 dot-common outputs;

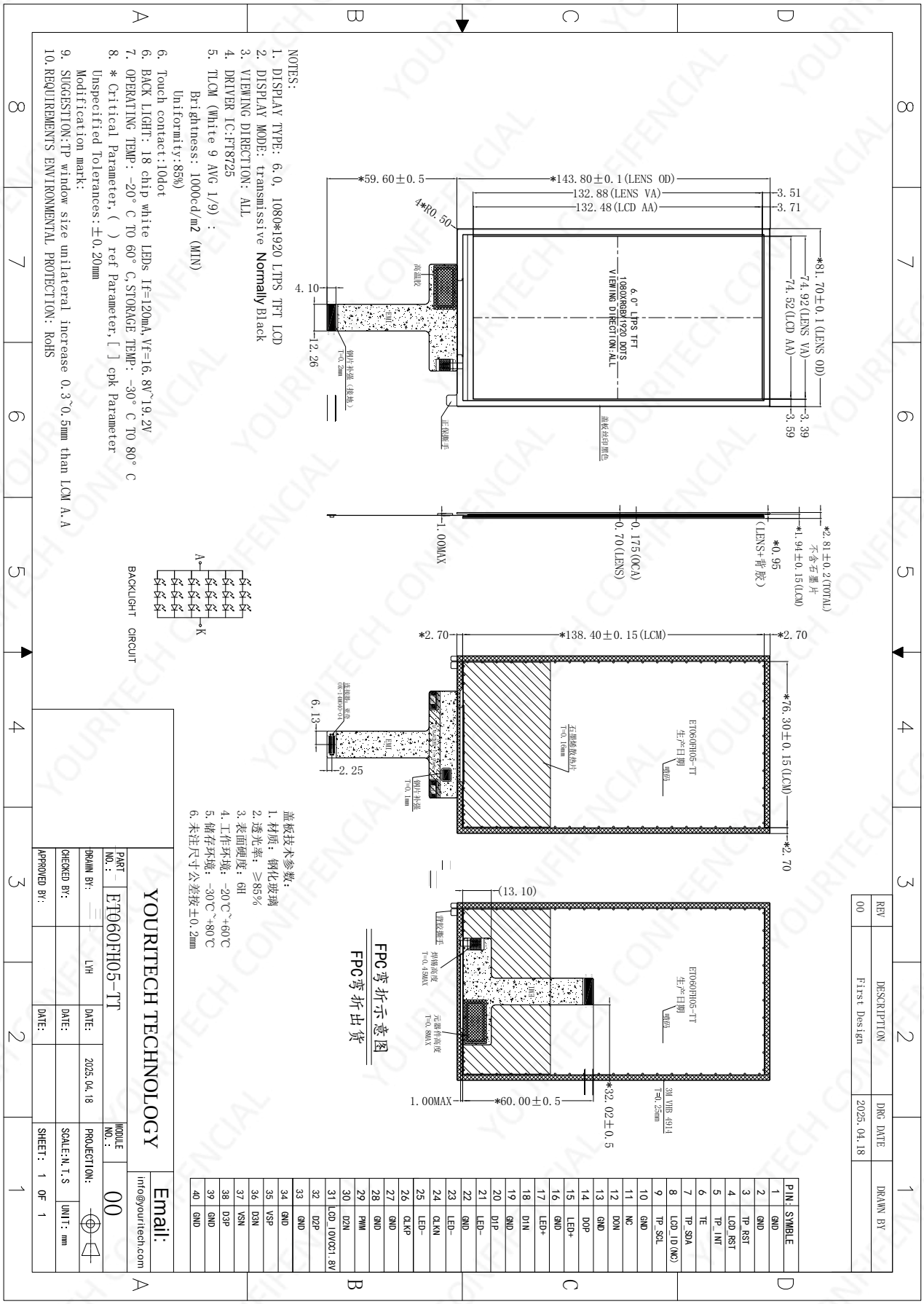
16.7M Color can be selected by software;

White LED back light;

4lane MIPI interface

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	1080*3RGB(H)X1920(V)	Dots
Pixel arrangement	RGB stripe	--
Pixel Pitch (W*H)	0.023(W) × 0.069 (H)	mm
Active area	74.52(W) × 132.48(H)	mm
Viewing direction	IPS Type LCD	--
TFT Driver IC	FT8725	--
TFT interface	4lane MIPI interface	--
Approx. Weight	TBD	g
LCM Size(W*H*T)	76.30(W) ×138.40(H) ×1.94(T)	mm
LCM+CG Size(W*H*T)	81.70(W) ×143.80(H) ×2.81(T)	mm
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--


NOTES:
1. DISPLAY TYPE: 6.0, 1080*1920 LTPS TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL
4. DRIVER IC:FT8725
5. TLCM (White 9 AVG 1/9) :
Brightness: 1000cd/m2 (MIN)
Uniformity:85%)
6. Touch contact:10dot
6. BACK LIGHT: 18 chip white LEDs If=120mA,Vf=16.8V~19.2V
7. OPERATING TEMP: -20° C TO 60° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter, ( ) ref Parameter, [ ] cpk Parameter
Unspecified Tolerances:±0.20mm
Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS
BACKLIGHT CIRCUIT
盖板技术参数:
1. 材质: 钢化玻璃
2. 透光率: ≥85%
3. 表面硬度: 6H
4. 工作环境: -20℃~+60℃
5. 储存环境: -30℃~+80℃
6. 未注尺寸公差按±0.2mm
FPC弯折示意图
FPC弯折出货
YOURITECH TECHNOLOGY
Email: info@youritech.com
PART NO.: ET060FH05-TT
MODULE NO.: 00
DRAWN BY: LYH DATE: 2025.04.18
CHECKED BY: DATE:
APPROVED BY: DATE:
PROJECTION:
SCALE:N.T.S
UNIT: mm
SHEET: 1 OF 1
REV 00 DESCRIPTION First Design DRG DATE 2025.04.18 DRAWN BY
PIN SYMBLE
1 GND
2 GND
3 TP_RST
4 LCD_RST
5 TP_INT
6 TE
7 TP_SDA
8 LCD_ID(NC)
9 TP_SCL
10 GND
11 NC
12 DDN
13 GND
14 DDP
15 LED+
16 GND
17 LED+
18 D1N
19 GND
20 D1P
21 LED-
22 GND
23 LED-
24 CLKN
25 LED-
26 CLKP
27 GND
28 GND
29 PWM
30 D2N
31 LCD_IOVCC1.8V
32 D2P
33 GND
34 GND
35 VSP
36 D3N
37 VSN
38 D3P
39 GND
40 GND

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+60	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
CG Operating Temperature & Humidity (20%～90%RH)	T_{OPR}	-20	+60	°C
CG SStorage Temperature & Humidity (20%～90%RH)	T_{STG}	-30	+80	°C

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for(IOVCC)	IOVCC	1.65	1.8	1.95	V
Analog voltage	VSP	4.5	--	6	V
Analog voltage	VSN	-6	--	-4.5	V

4.2 Back-Light Unit Characeristics

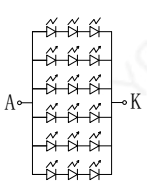
The back-light system is an edge-lighting type with 18 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	16.8	--	19.2	V	--
Forward current	I_F	--	120	--	mA	--
Luminance(With LCD+CG)	Lv	--	1000	--	cd/m^2	--
LED life time	N/A	--	20,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:

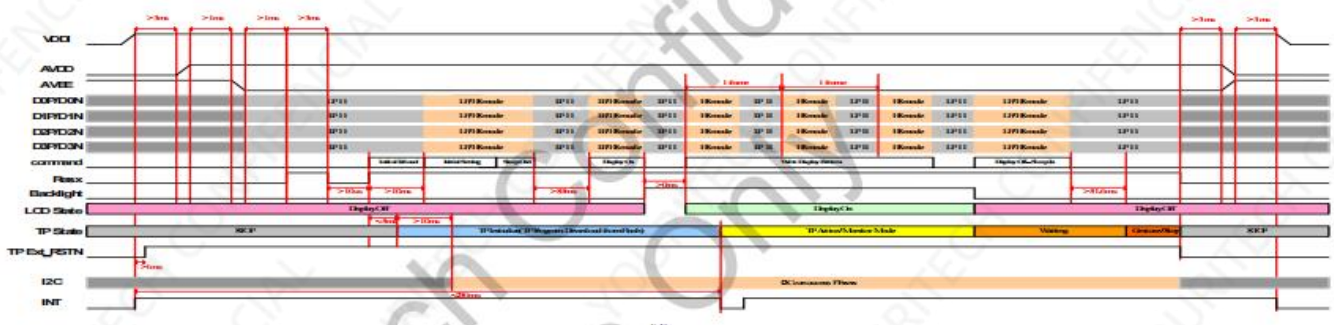


5. Module Function Description

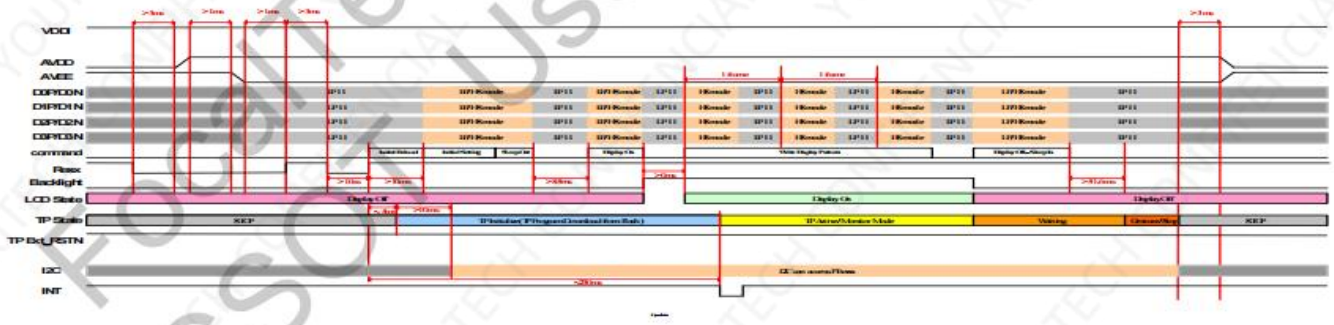
1	GND	Power Ground	
2	GND	Power Ground	
3	CTP_RST	Touch panel reset	
4	LCD_RST 1.8V	Reset signal input terminal. Active at 'L'.	
5	CTP_INT	Interrupt signal	
6	TE	Frame head pulse for tearing effect.	
7	CTP_SDA	Touch panel I2C data	
8	LCD_ID(NC)	No Connection.	
9	CTP_SCL	Touch panel I2C clock	
10	GND	Power Ground	
11	NC	No Connection.	
12	D0N	Negative polarity of low voltage differential data 0 signal	
13	GND	Power Ground	
14	D0P	Positive polarity of low voltage differential data 0 signal	
15	LED+	Power supply for backlight anode input terminal.	
16	GND	Power Ground	
17	LED+	Power supply for backlight anode input terminal.	
18	D1N	Negative polarity of low voltage differential data 1 signal	
19	GND	Power Ground	
20	D1P	Positive polarity of low voltage differential data 1 signal	
21	LED-	Power supply for backlight cathode input terminal.	
22	GND	Power Ground	
23	LED-	Power supply for backlight cathode input terminal.	
24	CLKN	Negative polarity of low voltage differential clock signal	
25	LED-	Power supply for backlight cathode input terminal.	
26	CLKP	Positive polarity of low voltage differential clock signal	
27	GND	Power Ground	
28	GND	Power Ground	
29	PWM	PWM (Pulse Width Modulation) Signal Of LED Driving.	
30	D2N	Negative polarity of low voltage differential data 2 signal	
31	LCD_IOVCC 1.8V	Power Supply For I/O.	
32	D2P	Positive polarity of low voltage differential data 2 signal	
33	GND	Power Ground	
34	GND	Power Ground	
35	VSP	External input voltage（4.5V~6V）	
36	D3N	Negative polarity of low voltage differential data 3 signal	
37	VSN	External input voltage（-6V~-4.5V）	
38	D3P	Positive polarity of low voltage differential data 3 signal	
39	GND	Power Ground	
40	GND	Power Ground	

6. Timing Characteristics

w/i Flash (3 Power mode)

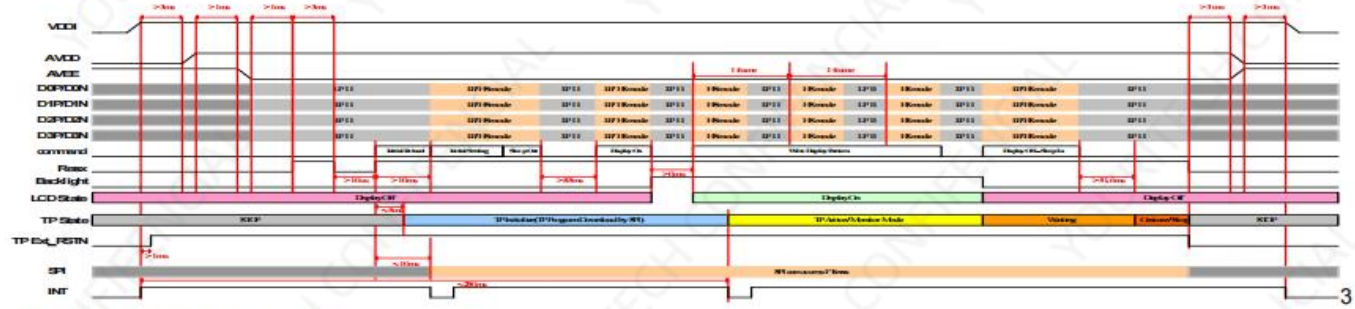


3 Power mode Power on/off sequence

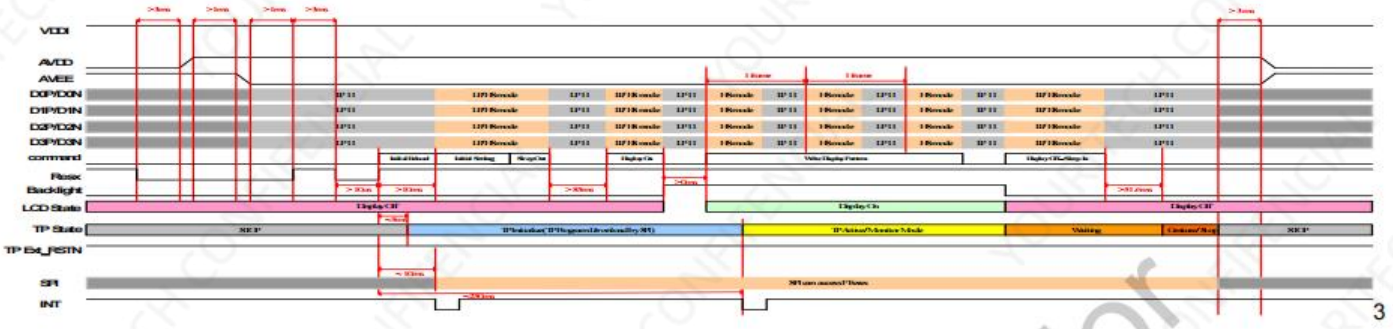


3 Power mode Power on/off sequence(VDDI keep)

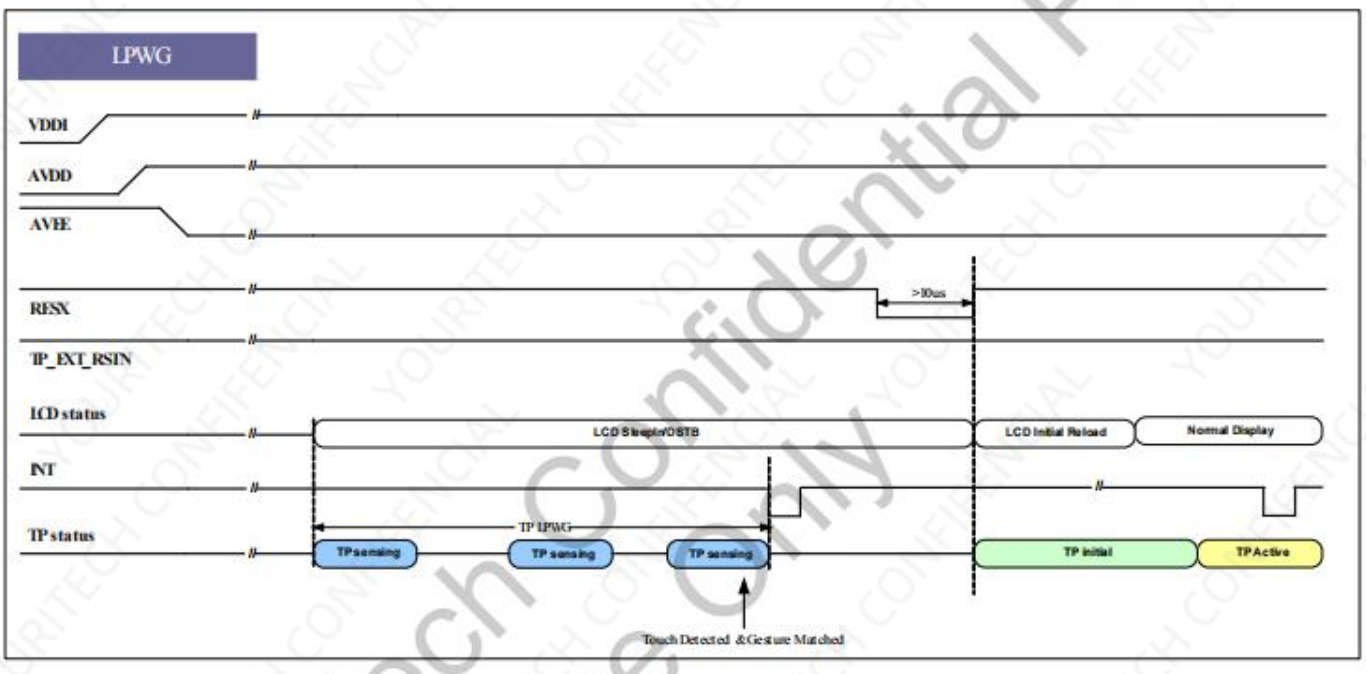
w/o Flash (3 Power mode)



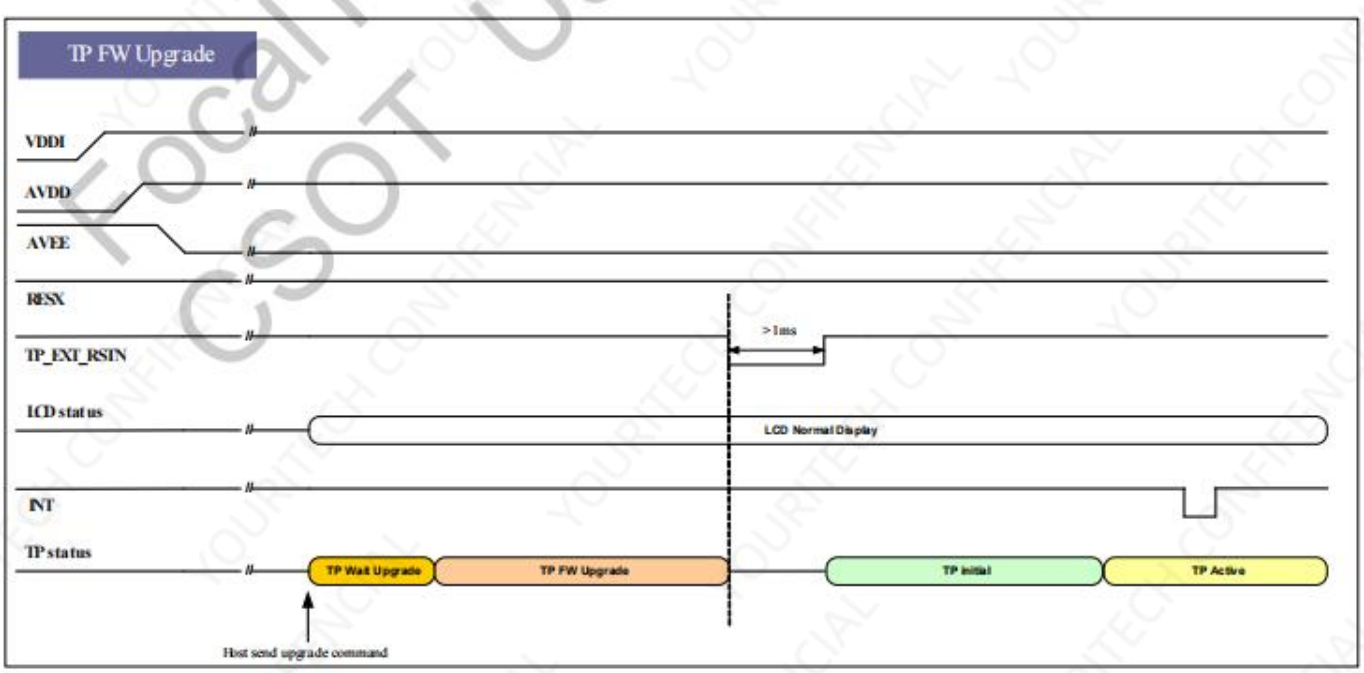
Power mode Power on/off sequence



Power mode Power on/off sequence(VDDI keep)



3 Power mode LPWG sequence



3

Power mode TP FW Upgrade

D-PHY HS Mode

Symbol	Description	Notes	Specification			Unit
			MIN	TYP	MAX	
UI_{INST}	UI instantaneous	1	0.769	-	12.5	ns
$T_{skew[TX]}$	Data to clock Skew for ≦1Gbps (measure at Transmitter)	2	-0.15	-	0.15	UI
	Data to clock Skew for ≧1Gbps (measure at Transmitter)	2	-0.2	-	0.2	UI
$T_{setup[RX]}$	Data to clock Setup Time for ≦1Gbps (measure at Receiver)	3	0.15	-	-	UI
	Data to clock Setup Time for ≧1Gbps (measure at Receiver)	3	0.2	-	-	UI
$T_{hold[RX]}$	Data to clock Hold Time for ≦1Gbps (measure at Receiver)	3	0.15	-	-	UI
	Data to clock Hold Time for ≧1Gbps (measure at Receiver)	3	0.2	-	-	UI
T_R & T_F	20% ~ 80% rise time & fall time ≦1Gbps (measure at Transmitter)	4	-	-	0.3	UI
	20% ~ 80% rise time & fall time ≧1Gbps (measure at Transmitter)	4	-	-	0.35	UI

Note:

Date rate range: 80Mbps ~ 1.3Gbps.

Total silicon and package skew delay budget.

Total setup and hold window for receiver.

To avoid excessive radiation, bit $rates_{\leqq 1Gbps}$ should not use values below 150ps.Bit $rates_{\geqq 1Gbps}$ should not use values below 100ps.

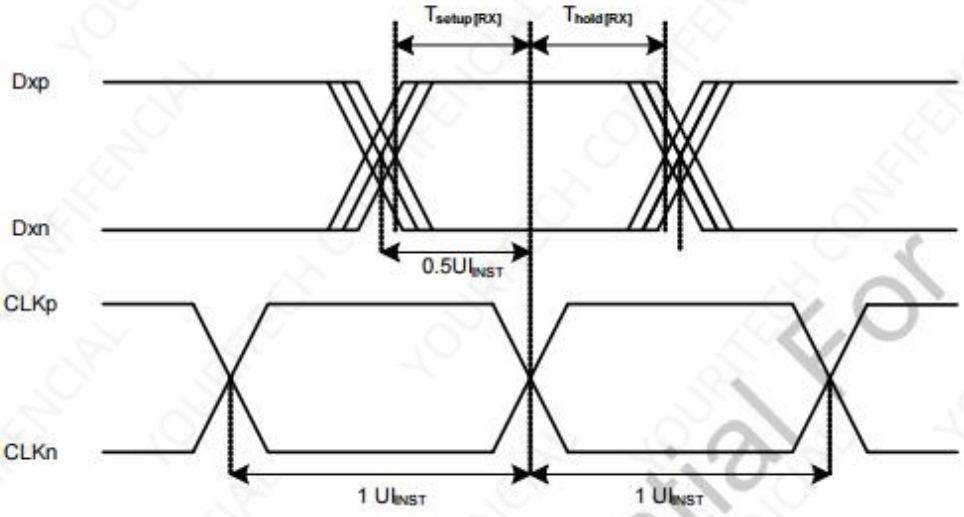


Figure: Data to Clock Timing Definitions for HS mode

—

D-PHY LP Mode

Symbol	Description	Notes	Specification			Unit
			MIN	TYP	MAX	
T_{LPX-M}	Transmitted length of any Low-Power state period (MCU)	-	50	-	-	ns
$T_{TA-SURE-M}$	The display module waits after the LP-10 before transmitting the LP-00 (MCU)	-	T_{LPX-M}	-	$2*T_{LPX-M}$	ns
$T_{TA-GO-M}$	The display module drives the LP-00 before releasing MCU control	-		$4*T_{LPX-M}$		ns
$T_{TA-GET-M}$	The display drives the LP-00 after accepting control	-		$5*T_{LPX-M}$		ns
Ratio T_{LPX}	Ratio of (T_{LPX-M}/T_{LPX-D}) for driving overlap	-	2/3	-	3/2	
T_{LPX-D}	Transmitted length of any Low-Power state period (Display)	-	58	-	-	ns
$T_{TA-SURE-D}$	The MCU waits after the LP-10 before transmitting the LP-00 (Display)	-	T_{LPX-D}	-	$2*T_{LPX-D}$	ns
$T_{TA-GO-D}$	The MCU drives the LP-00 before releasing Display control	-		$4*T_{LPX-D}$		ns
$T_{TA-GET-D}$	The MCU drives the LP-00 after accepting control	-		$5*T_{LPX-D}$		ns

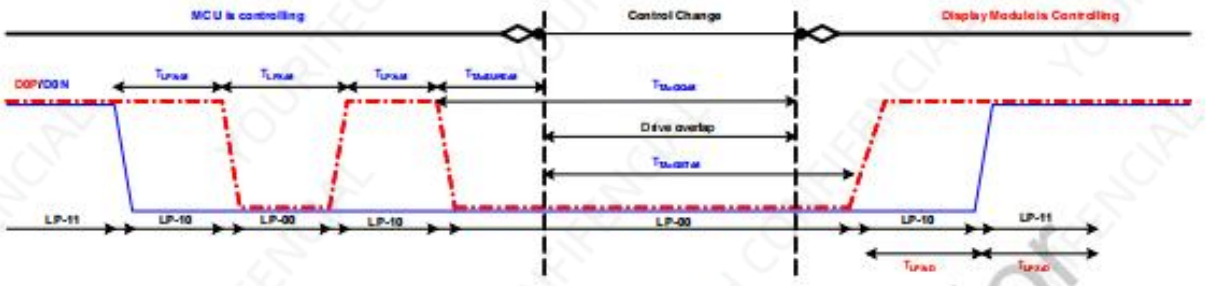


Figure: BTA from the MCU to the Display Module

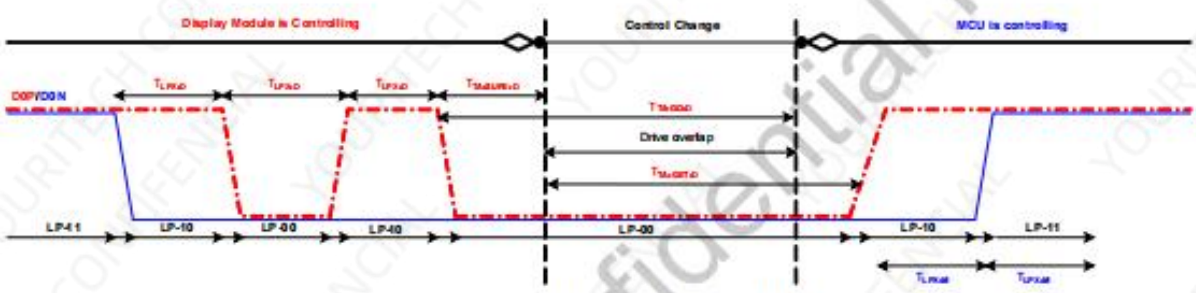


Figure: BTA from the Display Module to the MCU

DPHY Clock transmission & HSDT Bursts

Symbol	Description	Notes	Specification			Unit
			MIN	TYP	MAX	
T_{LPX}	Length of any LP state period	-	50	-	-	ns
$T_{CLK-TERM-EN}$	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	-	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	-	38	-	95	ns
$T_{CLK-PREPARE}+T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that HS-0 drive period before starting clock	-	300	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	-	8	-	-	UI
$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	-	60ns+52UI	-	-	ns
$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	-	60	-	-	ns
T_{EoT}	Time from start of $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	-	105ns +12UI	ns
$T_{D-TERM-EN}$	Time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	-	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	-	40ns + 4UI	-	85ns + 6UI	ns

$T_{HS-PREPARE}+T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence	-	145ns+10UI	-	-	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	-	max(8UI, 60ns+4UI)	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	-	40	-	55ns + 4UI	ns
T_{EoT}	Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state	-	-	-	105ns+12UI	ns
$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	-	100	-	-	ns

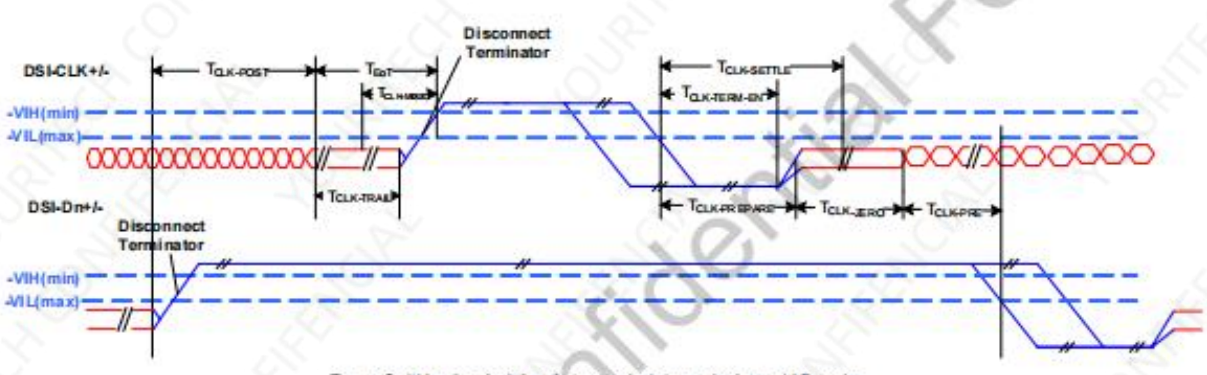


Figure: Swithing the clock lane between clock transmission and LP mode

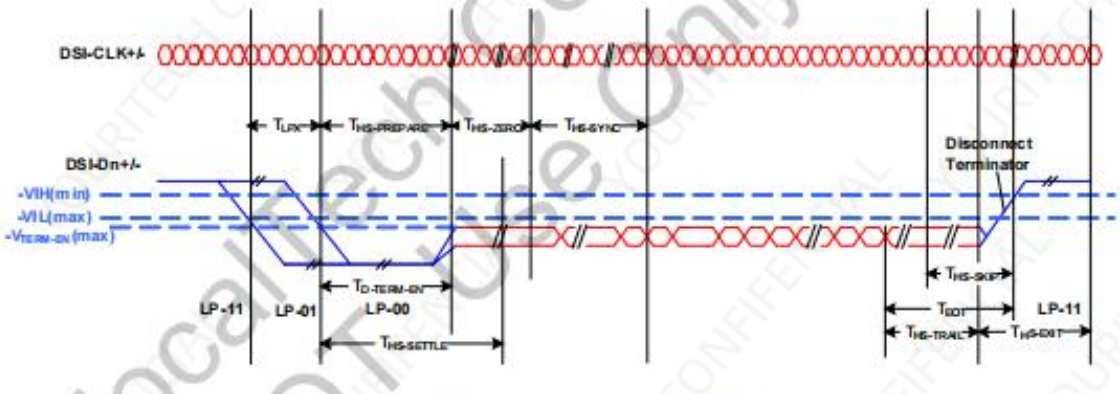


Figure: High Speed Data Transmission in Bursts

DPHY: LP-11 between High Speed and Low Power Modes

DSI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-11) when 4 different combinations, what are listed below, are possible:

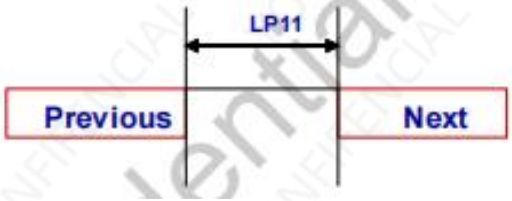
1. High Speed Mode => Stop State (SS, LP-11) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-11) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-11) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-11) => Low Power Mode

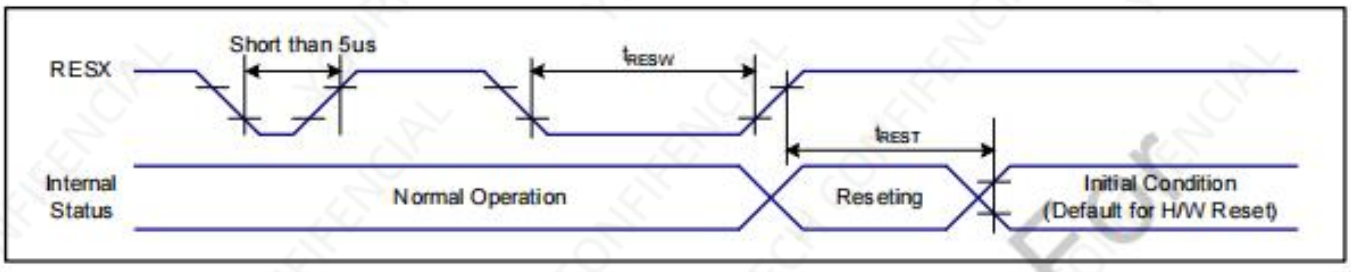
The Low Power Mode is also including 2 different functions:

1. Escape
2. Bus Turnaround (BTA)

Stop State (SS, LP-11) Timings from Previous mode to Next mode

Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100 ns	-	400ns+ 8UI	-	100 ns	-
HSDT	170ns+ 52UI	-	520ns+ 60UI	-	170ns+ 52UI	-
BTA	100 ns	-	400ns+ 8UI	-	100 ns	-





VSS=0V, VDDI=1.65V to 3.6V, Ta = -30°C to 70°C

Symbol	Parameter	Related Pin	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	Reset applied aduring Sleep-in mode	us
			70	-	-	Reset applied during Sleep-out mode	ms
t_{REST}	*2) Reset complete time	-	-	-	10	Reset applied during Sleep-in mode	ms
		-	-	-	120	Reset applied during Sleep-out mode	ms

Table: Reset input timing

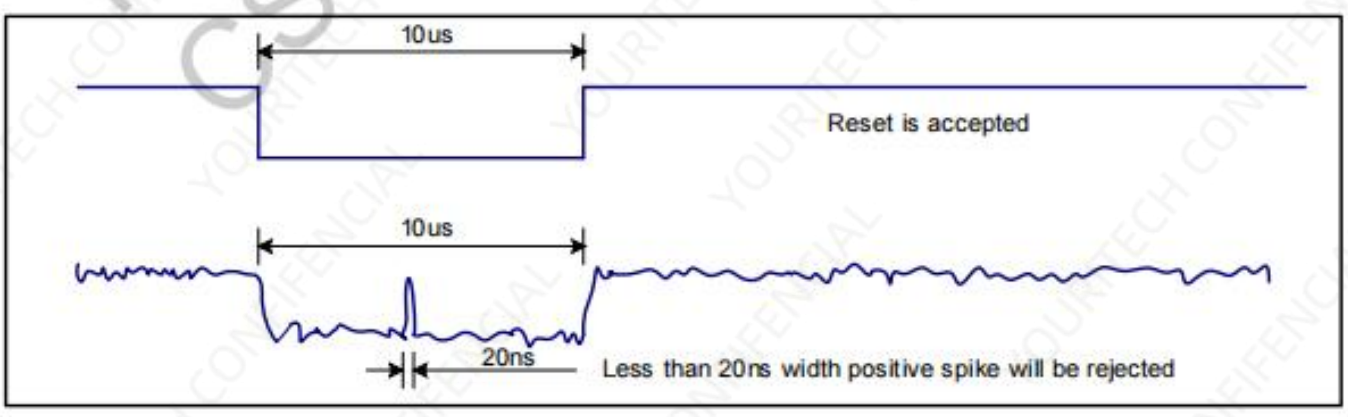
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset starts in Sleep-out mode. The display remains the blank state in Sleep-in mode) and then return to default condition for H/W reset.

Note 3. During Reset complete time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 10ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



7.Optical Characteristics

Optical Specification

Item	Symbol	Condition	Values			Unit	Notes
			Min.	Typ.	Max.		
Transmittance	TR%	/	5.30	6.23	/	%	基于 silicate BLU 实测 cellfactor 转换为 C-light 评估，WI APF+WO Haze
CR	/	/	1000	1500	/	/	Note 1
View angle	θL	Φ=180°	70	80	/	/	Note 1
(CR≥10)	θR	Φ=0°	70	80	/	/	
	θT	Φ=90°	70	80	/	/	
	θB	Φ=270°	70	80	/	/	
Response time	Tr+ Tf	/	/	24	28	ms	Note 2
Color filter Color Chromaticity (CIE1931)	Wx	/	-0.02	0.288	+0.02	/	@ CF C light Note 1 C Light
	Wy	/	0.305	0.310	0.345	/	
	Rx	/	0.652	0.670	0.692	/	
	Ry	/	0.297	0.317	0.337	/	
	Gx	/	0.283	0.233	0.323	/	
	Gy	/	0.545	0.627	0.585	/	
	Bx	/	0.121	0.138	0.161	/	
	By	/	0.046	0.079	0.086	/	
NTSC	/	/	77%	82%	/	/	
Cross Talk	/	/	/	/	2	%	
Gamma	/	/	1.9	2.2	2.5	/	

Test Conditions:

①Ambient temperature is 25℃.

②The test systems refer to Note 1

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room, the optical properties are measured at the center point of the LCD screen.

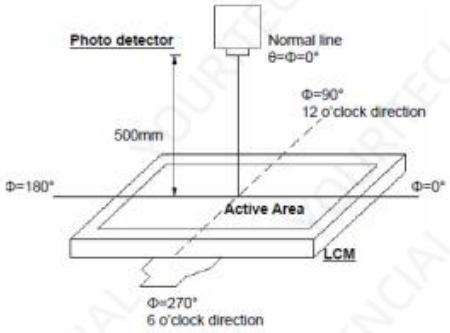
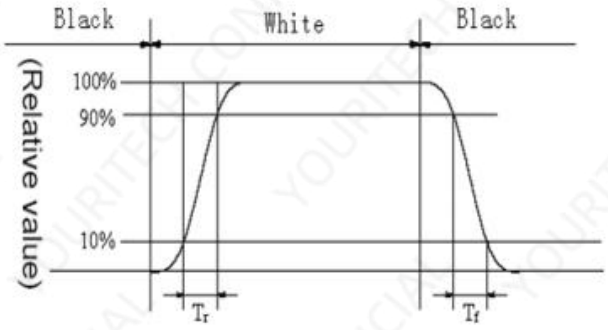


Fig. 4-2 Optical measurement system setup

Note 2: Definition of response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rising time (Tr) is the time between photo detector output intensity changed from 10% to 90%. And falling time (Tf) is the time between photo detector output intensity changed from 90% to 10%.



Note 3: Definition of color chromaticity

Color coordinates measured at center point of LCD.

8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+60°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH / 96H	
6	Thermal and cold shock	Static state，-20℃（30min）~60℃（30min），10 cycles	

9. Packing Method----TBD

- END -