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Optical Bonding

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Cover glass

System solutions

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Custom Display

Production Custom designs Installation

Mechanical design



MODEL NO : ET060HD02-T

MODEL VERSION: 01

SPEC VERSION : 1.0

ISSUED DATE: 2021-01-08

☐ Preliminary Specification

☒ Final Product Specification

Customer : _____

Approved by	Notes

Youri Confirmation

Prepared by	Reviewed by	Approved by
John	Johnny	Wang

1. Introduction

1.1 Scope of application

LCD specification: Dots 720xRGBx1280

As to basic specification of the driver IC, refer to the IC (**Raydium:RM68200**) specification and data book.

All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

TFT Structure: TFT PANNEL+IC +FPC+BL;

IPS Type LCD

720dot-segment and 1280 dot-common outputs;

16.7M Color can be selected by software;

White LED back light;

4lane MIPI interface

1.3 Applications:

2. LCM General specification

ITEM	Standard value	Unit
LCD Type	Normally black	--
Drive element	TFT active matrix	--
Number of pixels	720*3RGB(H)X1280(V)	Dots
Pixel arrangement	RGB stripe	--
Pixel Pitch (W*H)	0.10275(W) × 0.10275 (H)	mm
Active area	73.98(W) × 131.52(H)	mm
Viewing direction	ALL O'CLOCK	-
TFT Driver IC	RM68200	
TFT interface	4lane MIPI interface	-
Approx. Weight	TBD	g
LCM Size(W*H*T)	76.84(W) × 139.46(H) × 2.02T)	mm
Touch structure	--	
Touch Driver IC	--	-
Touch Interface	--	



3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T _{OPR}	-20	+60	°C
LCM Storage Temperature	T _{STG}	-30	+70	°C
Humidity	RH	-	90	%

4.Electrical Characteristics

4.1.1TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	1.65	1.8	3.3	V
Supply Voltage for(DC/DC)	VDD	2.5	3.3	3.6	V
Supply Voltage for(DC/DC)	AVDD				V
Supply Voltage for(DC/DC)	AVEE				V

4.2 Back-Light Unit Characeristics

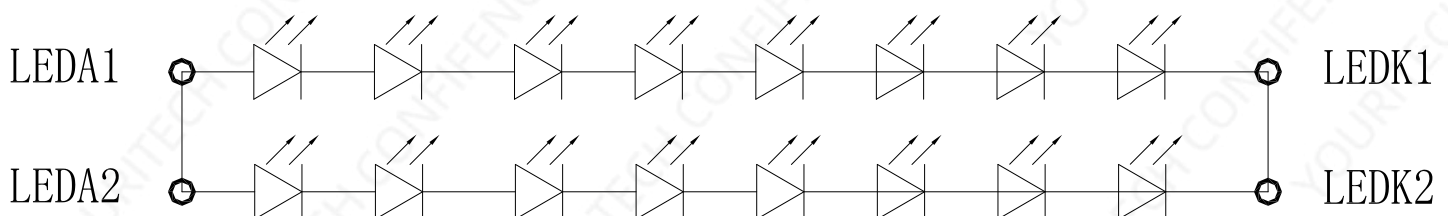
The back-light system is an edge-lighting type with 16 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V _F	22.4	--	25.6	V	-
Forward current	I _F	--	40	-	mA	-
Luminance(With LCD)	L _v		500	--	cd/m ²	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

- (1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



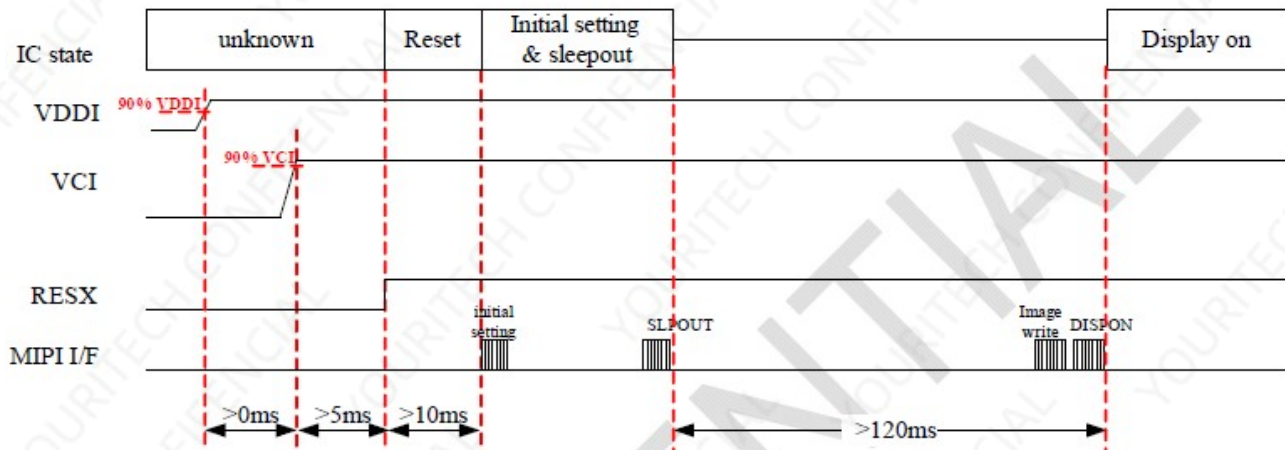
5. Module Function Description

Pin No.	Symbol	Functional	Notes
1	TD3N	MIPI DSI differential data pair	
2	TD3P		
3	GND	Power Ground	
4	TD2N	MIPI DSI differential data pair	
5	TD2P		
6	GND	Power Ground	
7	TCN	MIPI DSI differential clock pair	
8	TCP		
9	GND	Power Ground	
10	TD1N	MIPI DSI differential data pair	
11	TD1P		
12	GND	Power Ground	
13	T0N	MIPI DSI differential data pair	
14	TD0P		
15	GND	Power Ground	
16	RESET	Reset signal input terminal. Active at 'L'.	
17	VCC(3.3V)	MIPI Voltage (VDDAM to VSSAM): 2.5V ~ 3.6V	
18	IOVCC(1.8V)	I/O Voltage (VDDI to DGND): 1.65V ~ 3.3V	
19	GND	Power Ground	
20	NC	NC	
21	LEDK	Power supply for backlight cathode input terminal.	
22	LEDK	Power supply for backlight cathode input terminal.	
23	NC	NC	
24	LEDA	Power supply for backlight anode input terminal.	
25	LEDA	Power supply for backlight anode input terminal.	

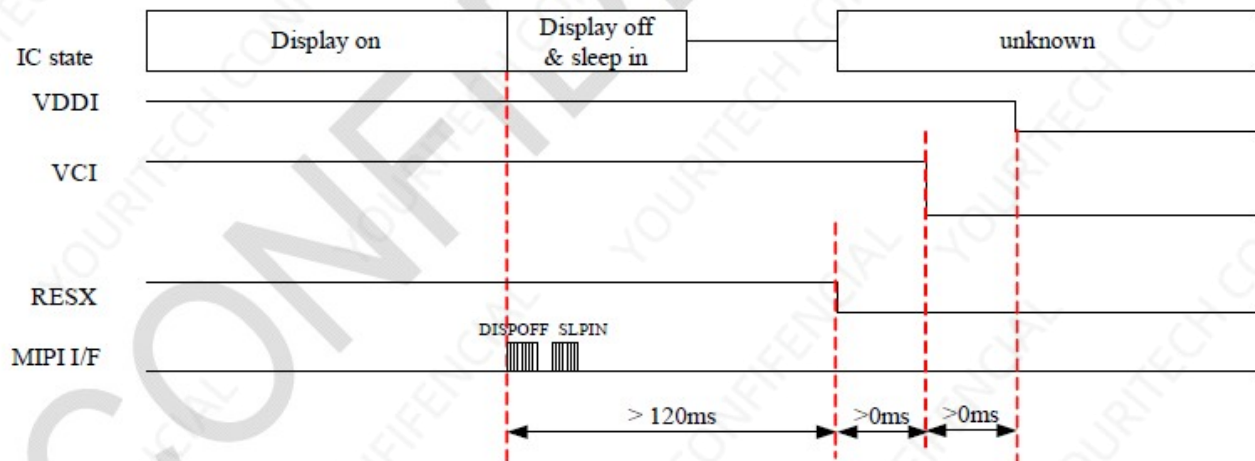
6. Timing Characteristics

Sequence I (Power IC & PFM mode: VCI / VDDI)

Power On sequence

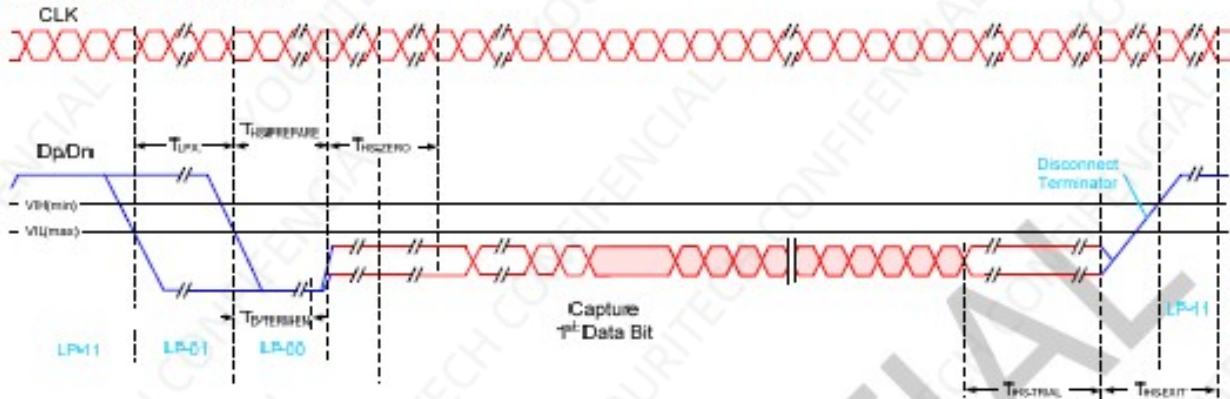


Power Off sequence

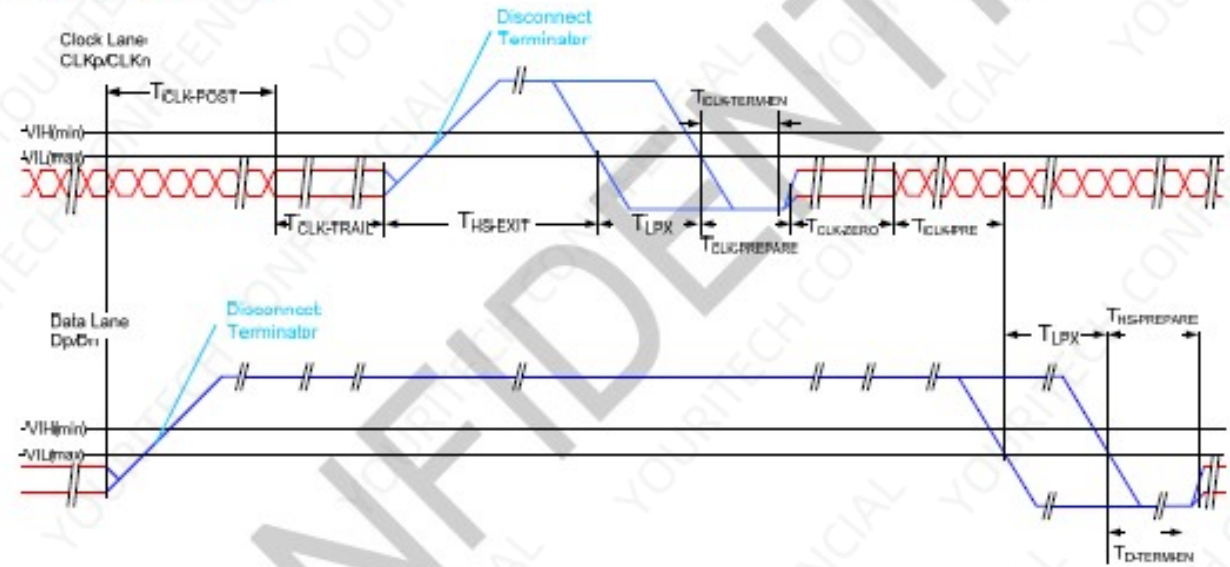


DSI Timing Characteristics HS

Data Transmission Burst



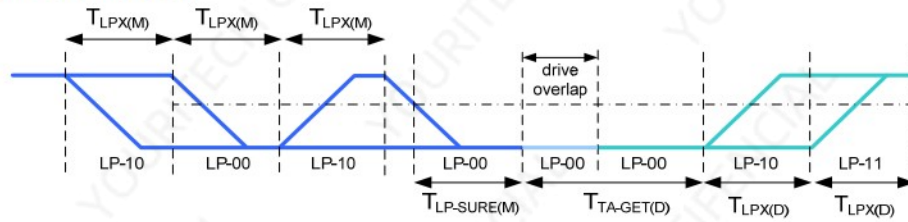
HS clock transmission



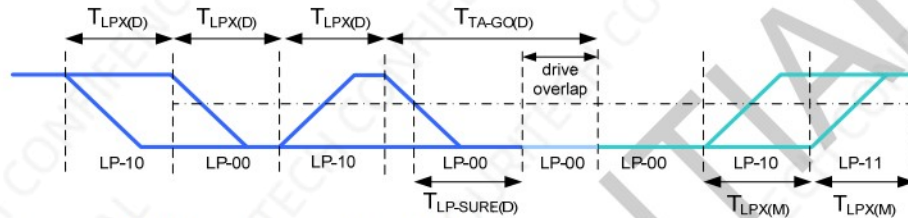
Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	$60ns + 52*UI$			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		$35 ns + 4*UI$	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	$40ns + 4*UI$		$85 ns + 6*UI$	ns
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	$145ns + 10*UI$			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	$60ns + 4*UI$			ns

Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

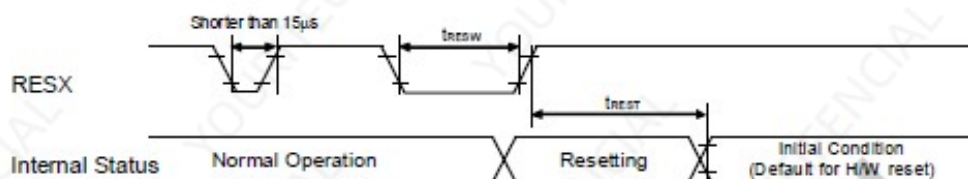
Low Power Mode:

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2 \cdot T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5 \cdot T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4 \cdot T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2 \cdot T_{LPX(D)}$	ns	2

NOTE:

1. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

Reset Timing Characteristics



Reset timing:

IOVCC=1.65V to 3.6V, AGND=DGND=0V, Ta=-40 to 85°C

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t _{RESW}	*1) Reset low pulse width	RESX	15	-	-		μs
t _{REST}	*2) Reset complete time	-	-	-	5	When reset applied during sleep-in mode	ms
		-	-	-	120	When reset applied during sleep-out mode	ms

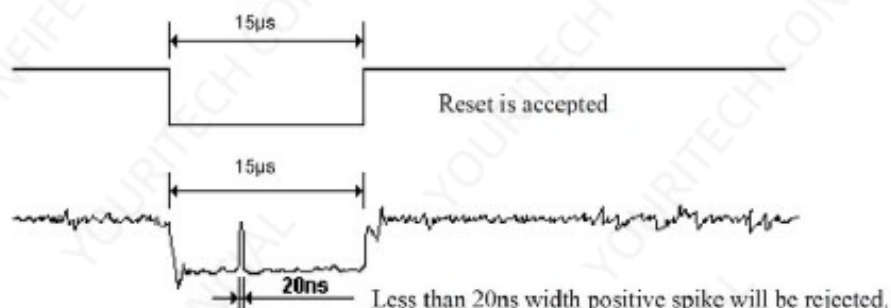
RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 15μs	IC Reset
Between 5μs and 15μs	Reset starts (It depends on voltage and temperature condition.)

Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in MTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Optical Specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T (%)	Θ=0 Normal viewing angle	—	3.64	—	%	Measuring with Normal Polarizer , For Reference Only
Transmittance (without Polarizer)		T (%)		—	9.85	—	%	
Contrast Ratio		CR		640	800	—		(1)(2) Measuring with Normal Polarizer , For Reference Only
Response Time	Rising	T _R		—	16	21	msec	(1)(3)
	Falling	T _F		—	19	24		
Color Gamut	(%)			—	70	—	%	C-light
Color Chromaticity (CIE1931)	White	W _x		0.284	0.304	0.324	—	(1)(4) CF glass
		W _y		0.304	0.324	0.344		
	Red	R _x		0.627	0.647	0.667	—	
		R _y		0.297	0.317	0.337		
	Green	G _x		0.238	0.258	0.278	—	
		G _y		0.546	0.566	0.586		
	Blue	B _x		0.120	0.140	0.160	—	
		B _y		0.068	0.088	0.108		
Viewing Angle	Hor.	Θ _L	CR>10	—	80	—	—	(1)(4) Measuring with Normal Polarizer , For Reference Only
		Θ _R		—	80	—		
	Ver.	Θ _U		—	80	—		
		Θ _D		—	80	—		
Optima View Direction		Free						(5)

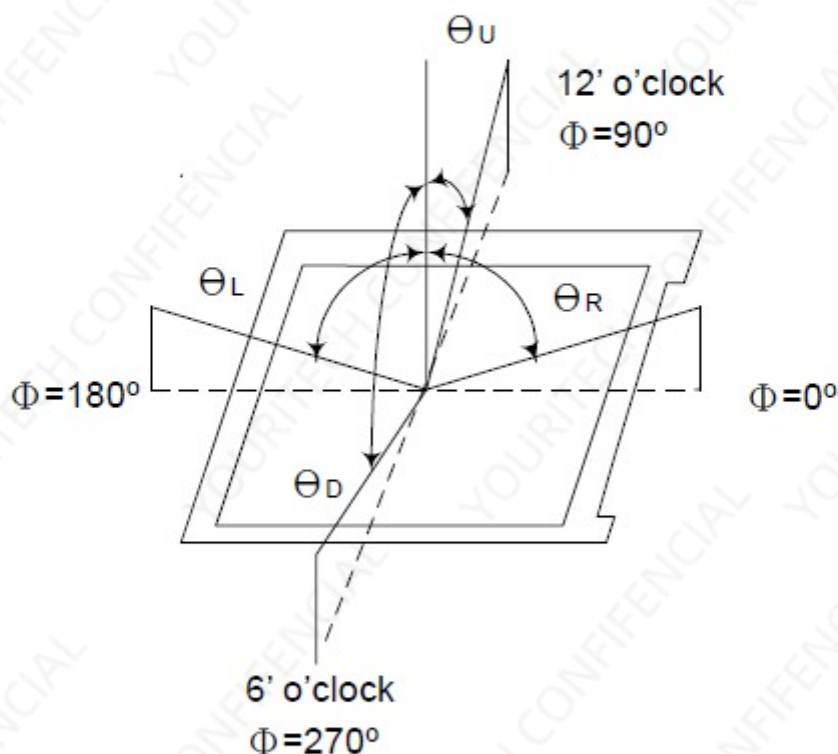
Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : $25 \pm 2^\circ\text{C}$
- 15min. warm-up time.

Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

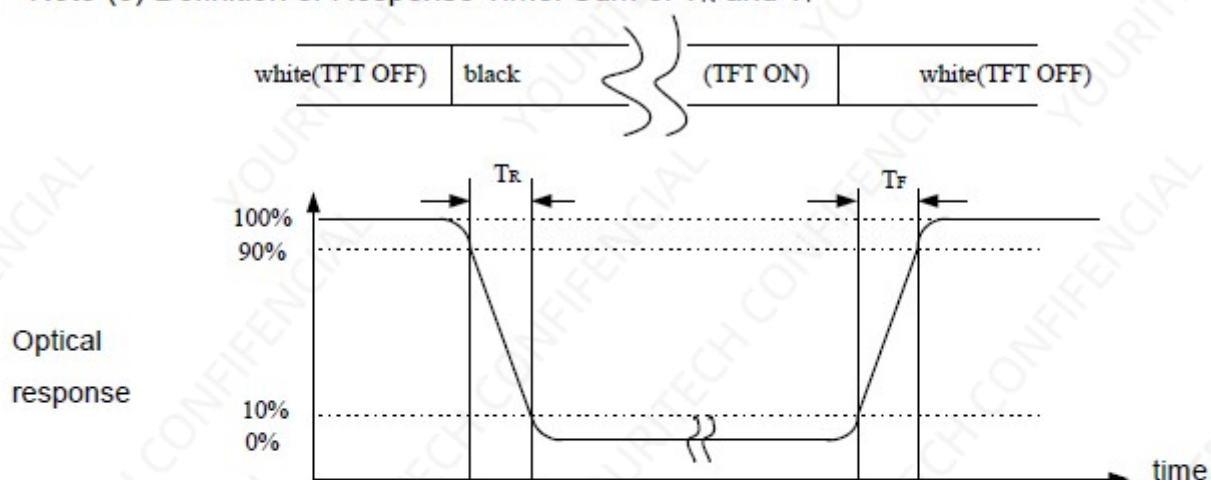
Note (1) Definition of Viewing Angle:



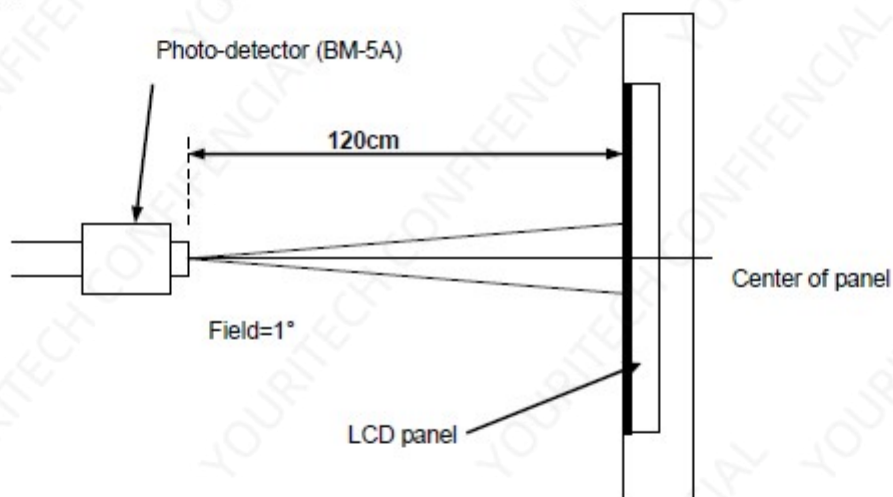
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$\text{CR} = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

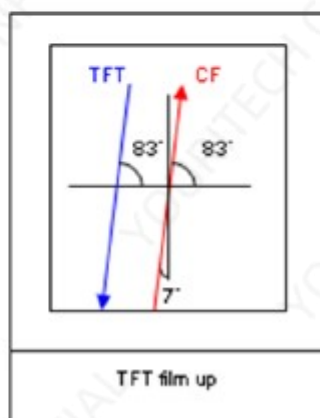
Note (3) Definition of Response Time: Sum of T_R and T_F



Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
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1	High Temp. Storage	+70°C / 96H	1. Functional test is OK. Missing Segment, short, unclear segment non-display, display abnormally and liquid crystal leakage un-allowed. 2. No low temperature bubbles, end seal loose and fall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Temp. Operating	+60°C / 96H	
4	Low Temp. Operating	-20°C / 96H	
5	High Temperature / Humidity storage	50°C x 90%RH / 96H	
6	Thermal and cold shock	Static state, -20°C (30min) ~60°C (30min), 50 cycles	

9. Packing Method----TBD

- END -