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PRODUCT SPECIFICATION

TFT-LCD MODULE

Model No：ET060WH02-O

For Customer's Acceptance	
Approved by	**Comment**

	Signature	Date
Prepared by		
Checked by		
Approved by		

Contents

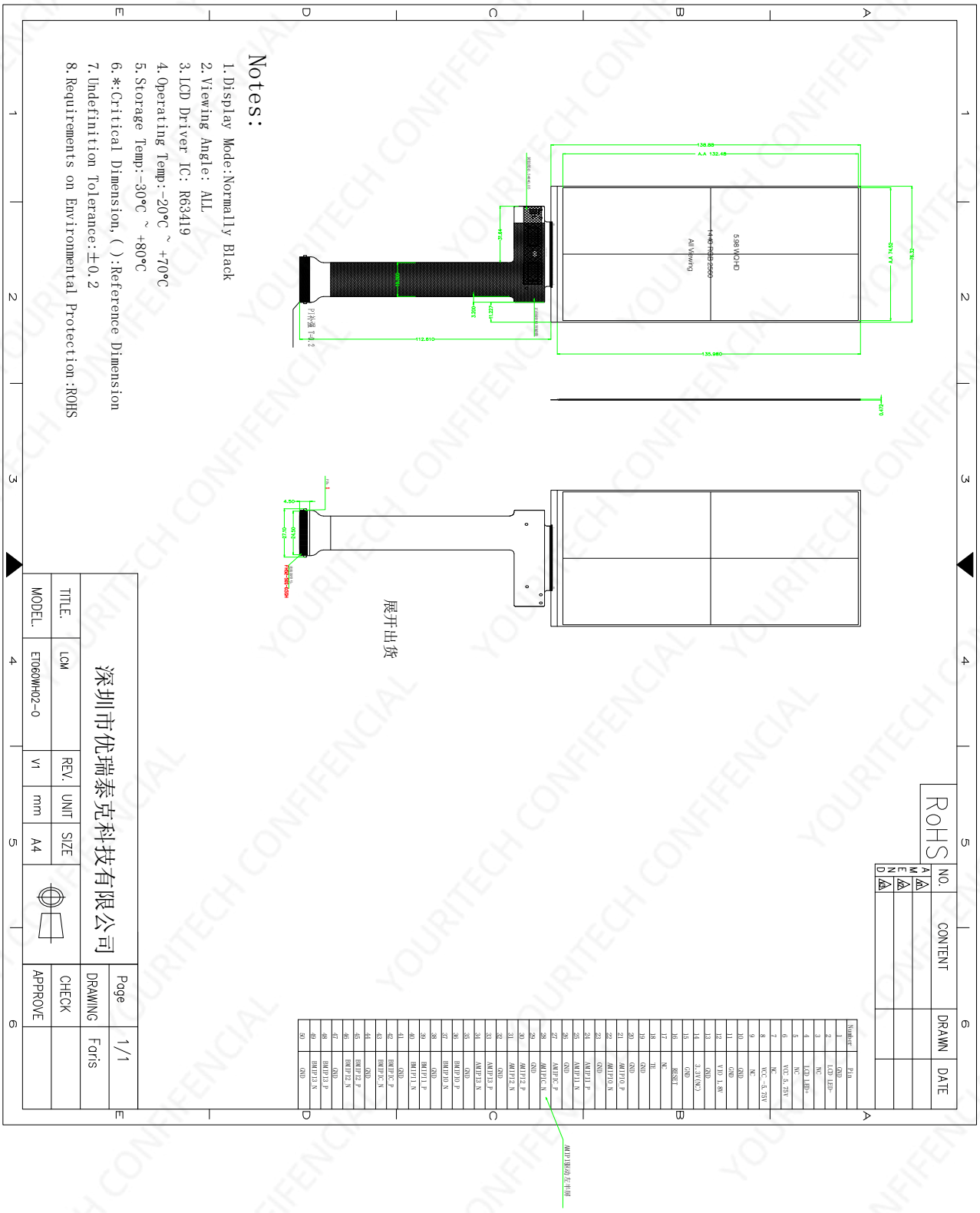
1. Document Revision History :

DOCUMENT REVISION	DATE	DESCRIPTION	PREPARED BY
A	2019-07-11	First Release.	

2. General Description

No	Item	Specification	Remark
1	Screen Size	6.0inch	
2	Display Mode	Normally Black	
3	Resolution	1440×RGB×2560	
4	Active Area	74.52*132.48	mm
5	Outline Dimension	76.32*138.88*0.472	mm
6	Viewing Direction	ALL	
7	Driver IC	R63419	
8	Interface	MIPI	
9	Back Light	-	
10	Touch Panel	-	

3. Outline Dimension



4. Interface Specification

Pin No	Symbol	Description	Note
1	GND	Ground	
2	LED-	Power Supply For LED Backlight Cathode Input.	
3	NC	No connection	
4	LED+	Power Supply For LED Backlight Anode Input.	
5	NC	No connection	
6	VCC_5.75	Power supply for Analog Circuit	
7	NC	No connection	
8	VCC_-5.75	Power supply for Analog Circuit	
9	NC	Dot clock signal for RGB interface operation.	
10	GND	Ground	
11	GND	Ground	
12	IOVCC	Power Supply For I/O.	
13	GND	Ground	
14	NC	No connection	
15	GND	Ground	
16	RESET	Reset Signal input pin.	
17	NC	No connection	
18	TE	Frame head pulse for tearing effect.	
19	GND	Ground	
20	GND	Ground	
21	A-D0P	Port A 1th line MIPI data positive signal	
22	A-D0N	Port A 1th line MIPI data negative signal	
23	GND	Ground	
24	A-D1P	Port A 2th line MIPI data positive signal	
25	A-D1N	Port A 2th line MIPI data negative signal	
26	GND	Ground	
27	A-CLKP	Port A MIPI Clock positive signal	
28	A-CLKN	Port A MIPI Clock negative signal	

29	GND	Ground	
30	A-D2P	Port A 3th line MIPI data positive signal	
31	A-D2N	Port A 3th line MIPI data negative signal	
32	GND	Ground	
33	A-D3P	Port A 4th line MIPI data positive signal	
34	A-D3N	Port A 4th line MIPI data negative signal	
35	GND	Ground	
36	B-D0P	Port B 1th line MIPI data positive signal	
37	B-D0N	Port B 1th line MIPI data negative signal	
38	GND	Ground	
39	B-D1P	Port B 2th line MIPI data positive signal	
40	B-D1N	Port B 2th line MIPI data negative signal	
41	GND	Ground	
42	B-CLKP	Port B MIPI Clock positive signal	
43	B-CLKN	Port B MIPI Clock negative signal	
44	GND	Ground	
45	B-D2P	Port B 3th line MIPI data positive signal	
46	B-D2N	Port B 3th line MIPI data negative signal	
47	GND	Ground	
48	B-D3P	Port B 4th line MIPI data positive signal	
49	B-D3N	Port B 4th line MIPI data negative signal	
50	GND	Ground	

5.Absolute Maximum Ratings

Electrical Maximum Ratings – for IC Only

Item	Symbol	Min.	Max.	Unit	Remark
Input power supply	IOV_{DD}	-0.3	+3.6	V	
Analog power supply	AV_{DD}	-0.3	+3.6	V	
Operating temperature (Ambient)	Topr	-20	+70	℃	
Storage temperature (Ambient)	Tstg	-30	+80	℃	

Note 1: If used beyond the absolute maximum ratings, the LSI may be destroyed. It is strongly recommended to use the LSI within the limits of its electrical characteristics during normal operation. The reliability of LSI is not guaranteed if used in the conditions beyond the limits and it may lead to malfunction.

6. Electrical Specifications

a. Typical Operation Condition (GND = 0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Digital Power Supply		IOVcc	1.7	1.8	1.9	V	
Analog Power Supply		VSP	4.8	5.2	5.4	V	
		VSN	-5.4	-5.2	-4.8	V	
Input Signal Voltage	H Level	V_{IH}	0.7 IOVcc	-	IOVcc	V	
	L Level	V_{IL}	GND	-	0.3 IOVcc	V	
Output Signal Voltage	H Level	V_{OH}	0.8 IOVcc	-	IOVcc	V	
	L Level	V_{OL}	GND	-	0.2 IOVcc	V	
LCD drive supply voltages		VGH	8.0	8.5	9.0	V	
		VGL	-9.0	-8.5	-8.0	V	
		VCOM	-	-0.15	-	V	Note.3

Note 1: The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

Note 2: MDDI interface electrical characteristics follow VESA V1.0

Note 3: Need OTP process for optimize VCOM

b. Current Consumption (GND=0V)

Mode	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Normal (Full)	P_N	VDDI = 1.8V	-	200	220	mW	Note 1
Sleep	P_S		-	2	5	mW	Note 2
Deep Standby	P_{DS}		-	0.5	1	mW	Note 3

Note 1: No backlight is driven , white pattern.

Note 2: Display off / sleep in

Note 3: Display off / sleep in / MIPI return to LP00

7. Timing Characteristics

a. MIPI DSI Characteristics

High Speed Mode

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
HS-RX	Differential input high threshold	VIDTH	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	-	70	
	Differential input low threshold	VIDTL	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-70	-	-	
	Single-ended input low voltage	VILHS	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	70	-	330	1
	Differential input impedance	ZID	Ω	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	100	-	2
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-50	-	550	
	Logic 1 input voltage	VIH	mV	IOVCC=1.65V~ 1.95V	880	-	1350	
	I/O leakage current	ILEAK	μA	Vin = -50mV ~ 1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-50	-	50	
	Thevenin output high level	VOH	V	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	IOVCC=DPHYVCC= 1.80V	110	-	-	2
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	450	-	-	

Notes: 1. VCMRX (DC) = (VP+VDN)/2

2. Excluding COG resistance (contact resistance and ITO wiring resistance).

MIPI DSI HS-RX Clock and Data-Clock Specifications

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
DSICLK Frequency	fDSICLK	MHz	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	100	-	500	4
DSICLK Cycle time	tCLKP	ns	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	1	-	10	
DSI Data Transfer Rate	tDSIR	Mbps	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	200	-	1000	4
Data to Clock Setup Time	tSETUP	UI	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	0.15	-	-	6
		ns	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	0.15	-	-	5,6
Clock to Data Hold Time	tHOLD	UI	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	0.15	-	-	6
		ns	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	0.15	-	-	5,6

Notes: 3. When fDSICLK<125MHz, change auto load NV setting so that it is compliant with THS-PREPARE+THS-ZERO spec.

4. Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.

5. tSETUP/tHOLD Time is measured without HS-TX Jitter.

MIPI DSI LP-RX/TX Clock and Data-Clock Specifications

Item	Symbol	Unit	Test condition	Min	Typ	Max	Notes
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	40 ns + 4*UI	-	85ns + 6*UI	
$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	$T_{HS-PREPARE}$ + $T_{HS-ZERO}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	145ns + 10*UI	-	-	
Time to drive flipped differential state after last payload data bit of a HS transmission burst	**$T_{HS-TRAIL}$**		IOVCC=DPHYVCC =1.65 ~ 1.95V	max (n*8*UI, 60 ns + n*4*UI)	-	-	1,2
Time to drive LP-11after HS burst	$T_{HS-EXIT}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	100	-	-	
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		IOVCC=DPHYVCC =1.65 ~ 1.95V	$4*T_{LPTX}$			
Time-out before new TX side starts driving	$T_{TA-SURE}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	$1*T_{LPTX}$	-	$2*T_{LPTX}$	
Time to drive LP-00 by new TX	T_{TA-GET}		IOVCC=DPHYVCC =1.65 ~ 1.95V	$5*T_{LPTX}$			
Length of any Low-Power state period	T_{LPX}	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	50	-	-	
Ratio of $T_{LPX(MASTER)}$/$T_{LPX(SLAVE)}$ between Master and Slave side	Ratio T_{LPX}		IOVCC=DPHYVCC =1.65 ~ 1.95V	2/3	-	3/2	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	**$T_{CLK-POST}$**		IOVCC=DPHYVCC =1.65 ~ 1.95V	60 ns + 52UI	-	-	3
$T_{CLK-PREPARE}$ +time for lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	300	-	-	
Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	UI	IOVCC=DPHYVCC =1.65 ~ 1.95V	8	-	-	
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	38	-	95	
Time to drive HS differential state after last payload clock bit of an HS transmission burst	$T_{CLK-TRAIL}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	60	-	-	
Time from start of THS-TRAIL period to start of LP-11 state	T_{EOT}		IOVCC=DPHYVCC =1.65 ~ 1.95V	-	-	105 ns + n*12*UI	2
Length of Low-Power TX period in case of using DSI clock	T_{LPTX1}	UI	IOVCC=DPHYVCC =1.65 ~ 1.95V	-	32	-	4
Length of Low-Power TX period in case of using internal OSC clock	T_{LPTX2}	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	-	1/(fosc/4)	-	

Notes: 1. *If a > b then max(a, b) = a, otherwise max(a, b) = b*

2. *Where n = 1 for Forward-direction HS mode.*
3. *The R63419 can work with this specification although the end part of internal process is remained when Clock Lane enter LP-11 and the R63419 can work without the remained process if tCLK-POST is more than 512 UI.*
4. *The R63419 uses DSI clock from the Host processor if Clock Lane is active, and internal oscillator clock if Clock Lane is disabled.*

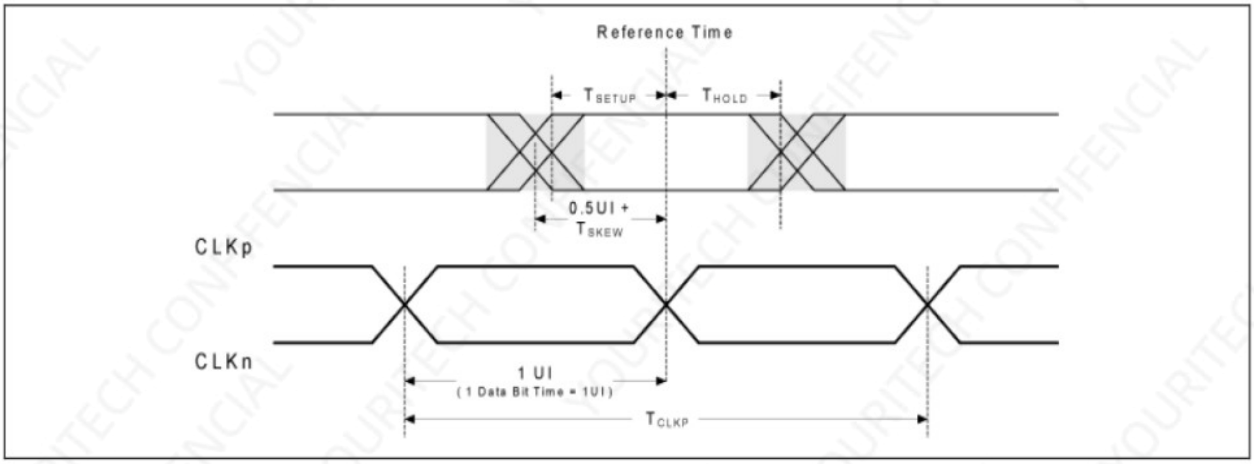


Fig. 2 Data to Clock Timing Definitions

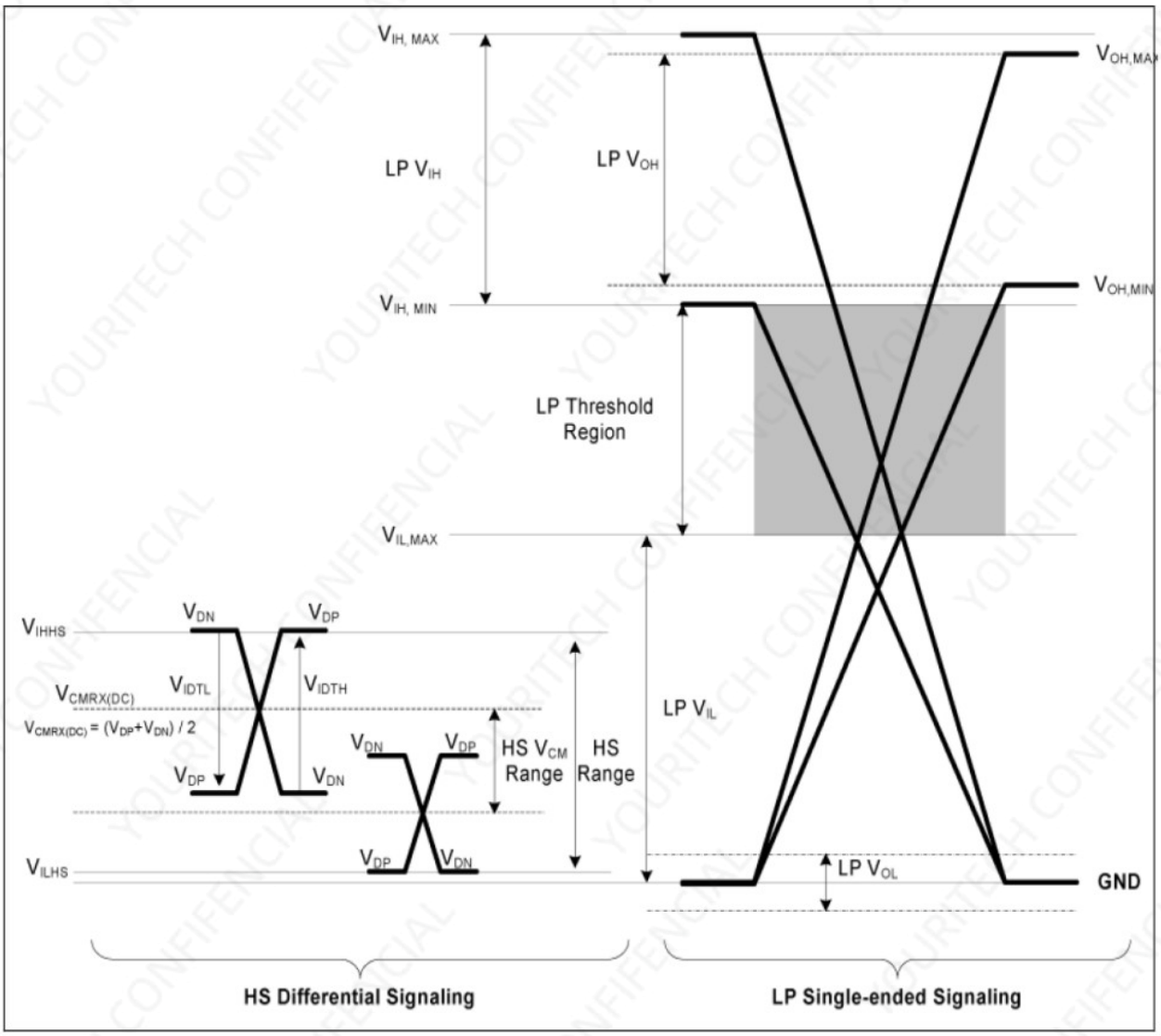


Fig. 3 DSI LP Mode

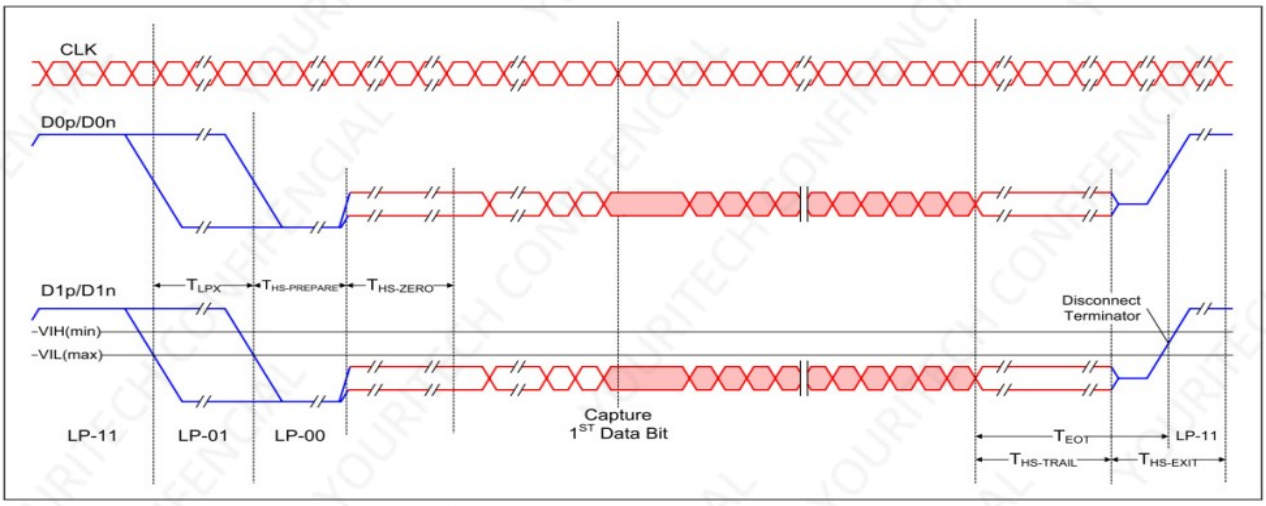


Fig. 4 HS Data Transmission in Bursts

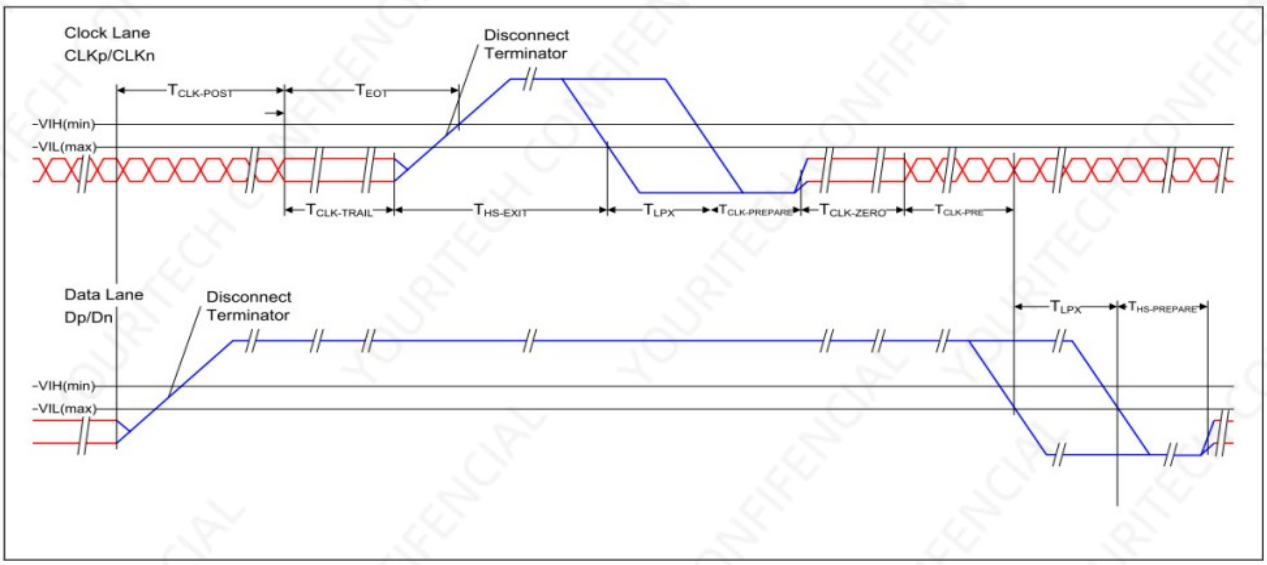


Fig. 5 Switching the Clock Lane between Clock Transmission and LP Mode

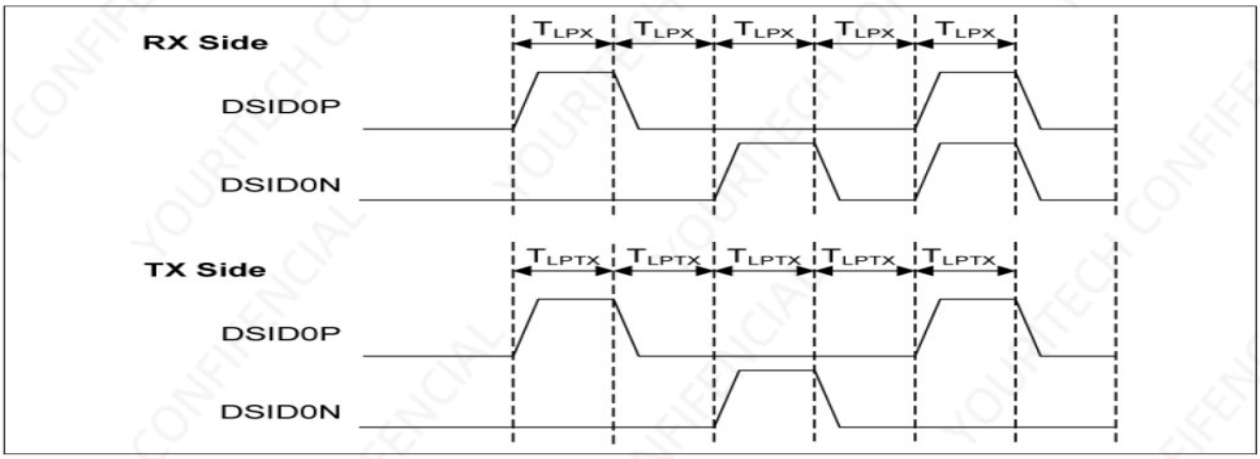


Fig. 6 DSI LP Mode

REST Timing Characteristics

Item	Symbol	Unit	Test condition	Min.	Max.
Reset low-level width1	tRW1	us	Power supply on	1000	–
Reset low-level width2	tRW2	us	Operation	1000	–
Reset time (Sleep IN)	tRT1	ms	–	–	3
Reset time (Sleep OUT)	tRT2	ms	–	–	3
Noise reject width	tRESNR	us	–	–	1

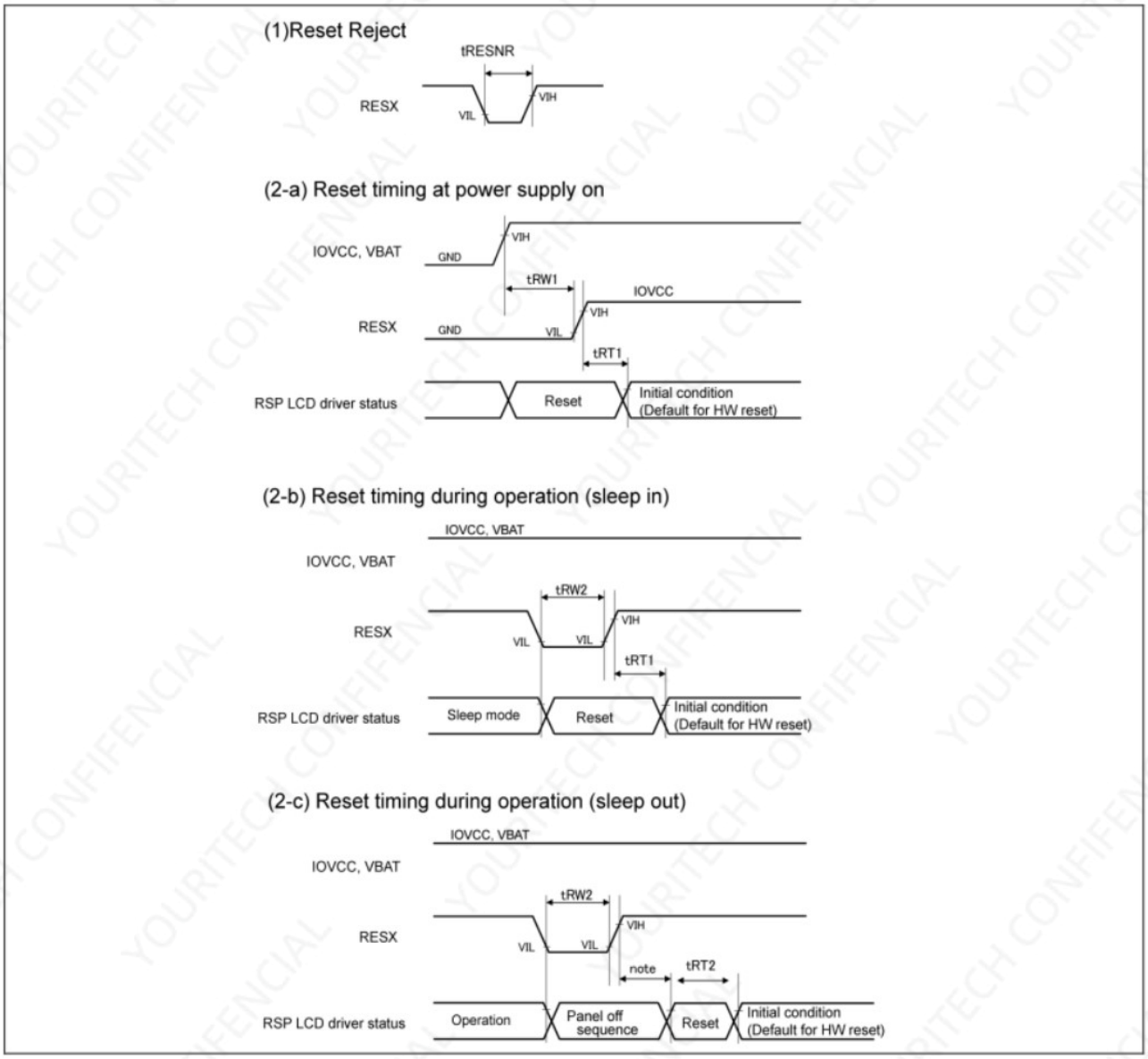
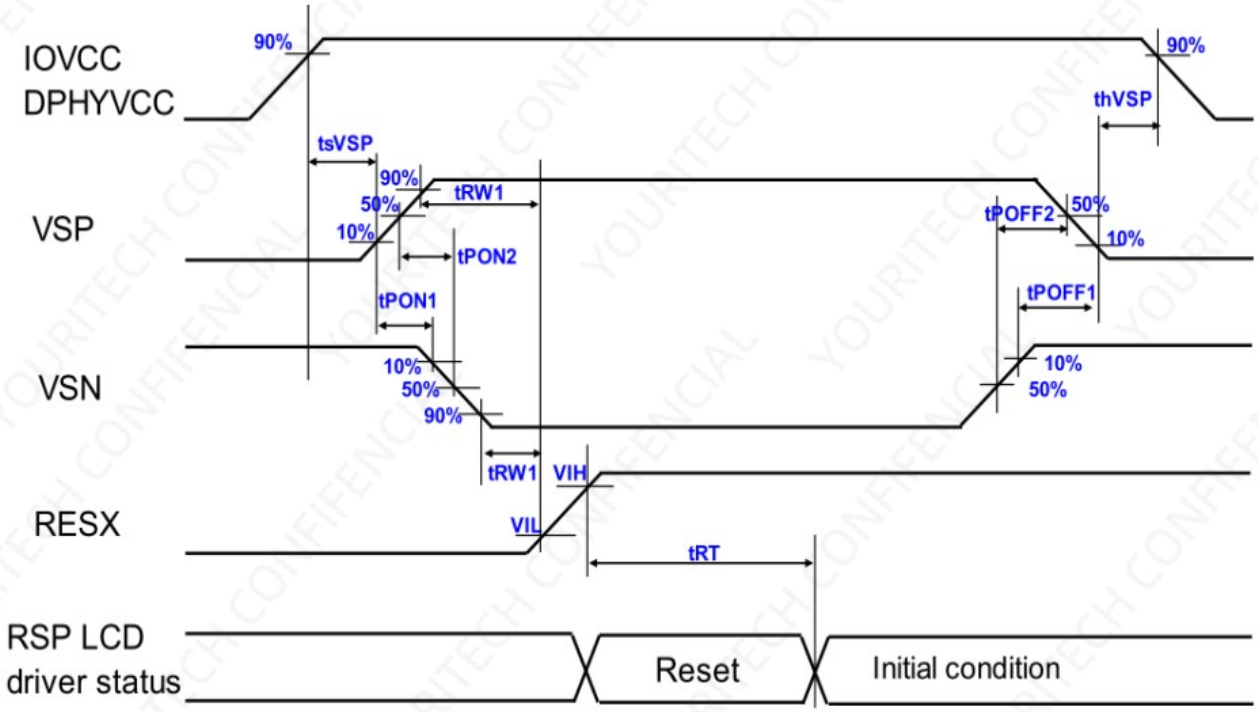


Fig. 7 Reset Timing Characteristics

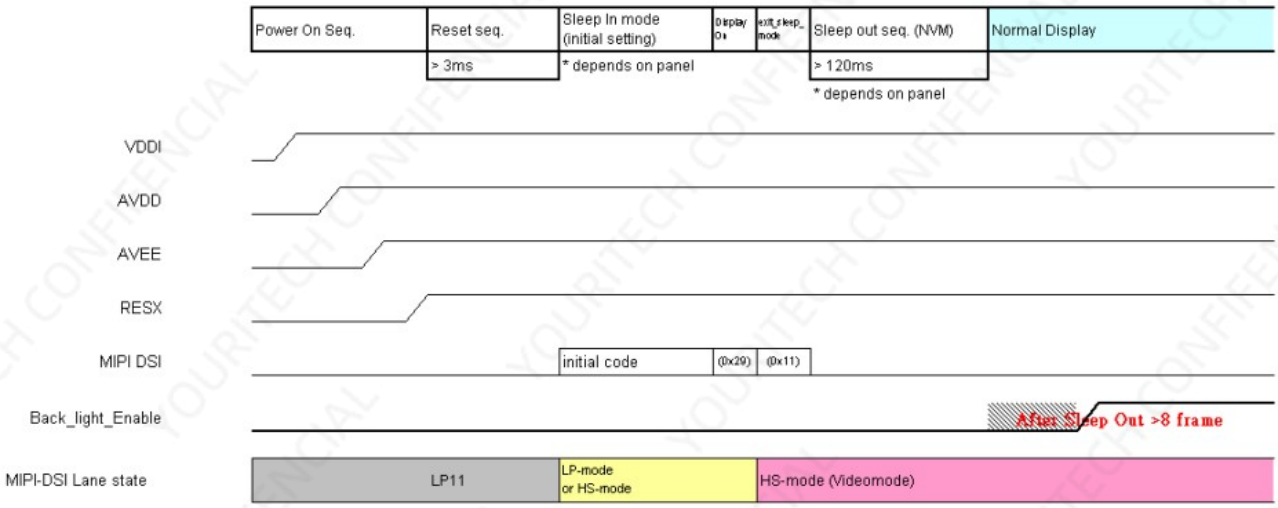
Note: 1. Refer to the appendix for details of "Panel off sequence".

8. Power Supply Configuration

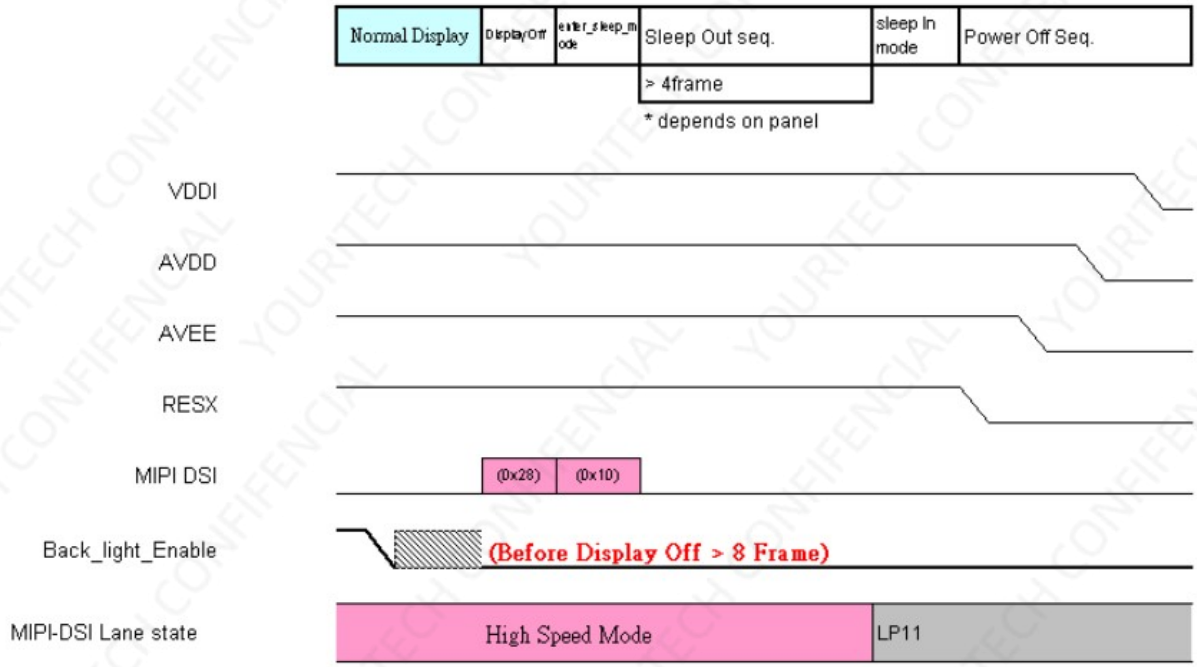
a. Power On Sequence



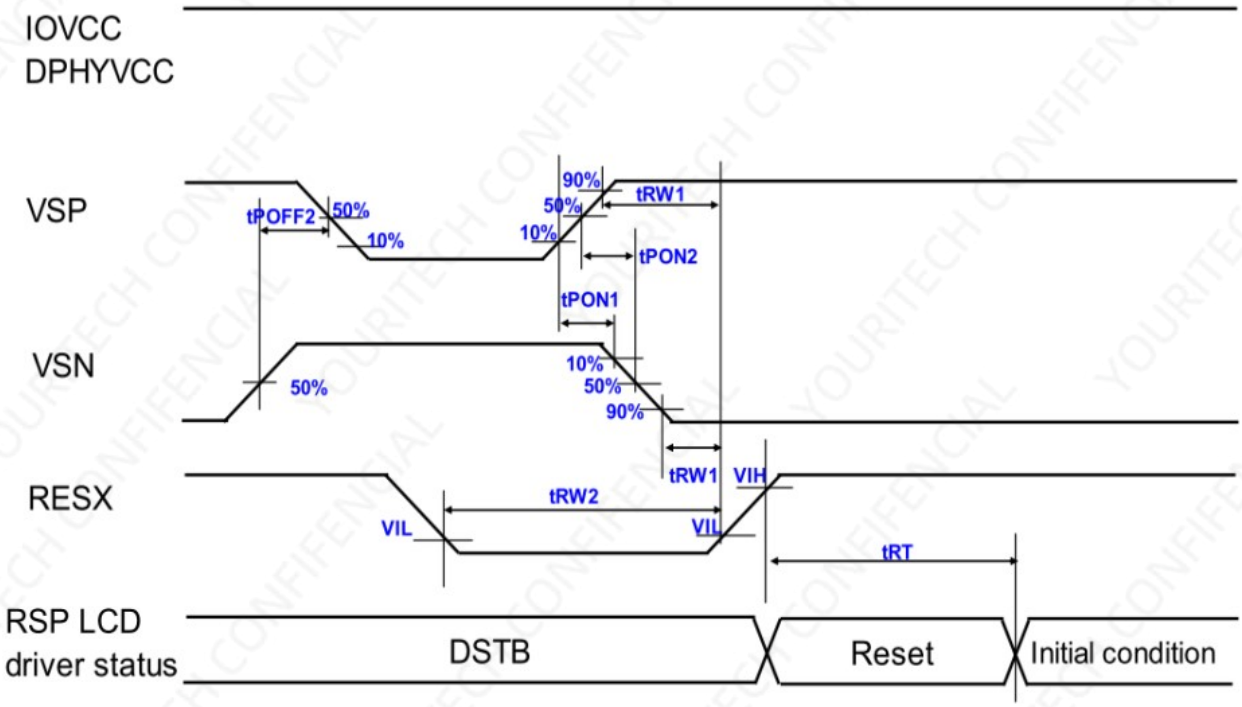
b. Display On Sequence



c. Display Off Sequence



d. Deep standby mode Sequence



Item	Symbol	Unit	Test Condition	Min	Max
VSP-VSN delay time (10% to 10%)	tPON1	us	Power On	0	–
VSP-VSN delay time (50% to 50%)	tPON2	us	Power On	0	–
System power on to VSP ON time	tsVSP	ms	Power On	1	–
Reset low-level width1	tRW1	ms	Power On	1	–
Reset low-level width2	tRW2	ms	Power Off	1	–
Reset time (Sleep IN)	tRT	ms	Power On	3	–
VSN-VSP delay time (10% to 10%)	tPOFF1	us	Power Off	0	–
VSN-VSP delay time (50% to 50%)	tPOFF2	us	Power Off	0	–
VSP OFF to system power off time	thVSP	us	Power Off	0	–

Fig. 8 Power supply on sequence

Notes: 1. Make sure that the following relationships are power supply sequence.

9.Optical Specification

Item 项目	Symbol 符号	Condition 条件	Min 最小值	Typ 典型值	Max 最大值	Unit 单位	Note 备注
Response time 响应时间	Tr&Tf	Θ=0° Ø=0° Ta=25°C	-	20	35	ms	1
Contrast ratio 对比度	Cr		-	1000	-	-	2
Color gamut 饱和度	S(%)		-	52	-	%	-
Luminance uniformity 均匀度	δWHITE		-	-	-	%	3
Viewing angle range 视角范围	Θx+	CR≧10 Ta=25°C	-	80	-	deg	4
	Θx-		-	80	-	deg	
	Θy+		-	80	-	deg	
	Θy-		-	80	-	deg	
LCM Luminance LCM 亮度	Lv	Θ=0° Ø=0° Ta=25°C	-	-	-	Cd/m2	5
CIE (X,Y) Chromaticity 色度坐标	White(X)		0.282	0.307	0.332	-	6
	White(Y)		0.298	0.323	0.348	-	

Note1.Response time is the time required for the display to transition from White to black(Rise Time,Tr)and from black to white(Decay Time,Tf).For additional information see FIG1...

Note2.contrast Ratio(CR) is defined mathematically by the following formula ,For more information see FIG2.

Contrast Ratio(CR)=Average Surface Luminance with all white pixels/ Average Surface Luminance with all black pixels

Note3.The uniformity in surface luminance(WHITE) is determined by measuring luminance at eath test position,and then dividing the maximum luminance of all white pixels by minimum luminance of all white pixels,For more information seeFIG2.

WHITE=Minimum Surface Luminance with all white pixels(P1,P2,.....)/Maximum Surface Luminance with all white pixels(P1,P2,.....)

Note4.Viewing angle is the angel at which contrast ratio is greater than a specific value.For TET

module,the specific value of contrast ratio is 10.For monochrome and color stn module,the specific value of contrast ratio is2.The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.For more information see FIG3

Note5. Surface luminance is the LCD surface luminance with all white pixels,For more information see FIG2.

LV=Average Surface Luminance with all white pixels(P1,P2,.....)

Note6.CIE(X,Y)chromaticity is the Center point value.For more information see FIG2.

Note7.For Viewing angle and response time testing,the testing date is base on Autronic-Melchers’s ConScope.Series instruments.For contrast ratio,Surface Luminance,Luminance uniformity and CIE,the testing date is base on CS-2000 photo detector.

Note8.For TN type TFT transmissive module,Gray scale reverse occurs in the direction of panel viewing angle

FIG1. The definition of Response time

响应时间定义

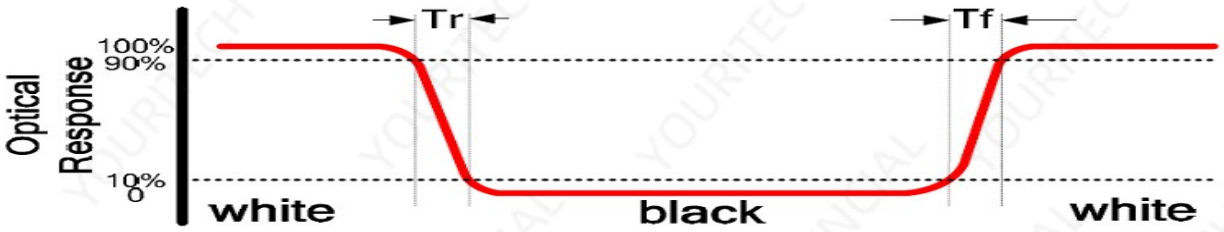
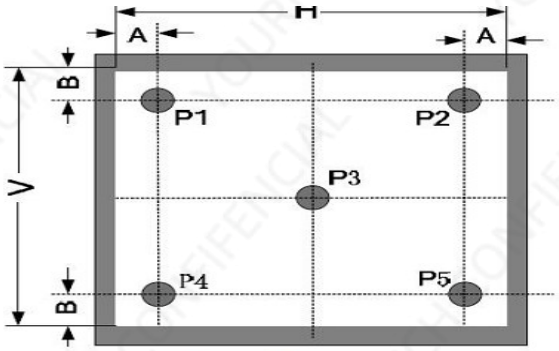
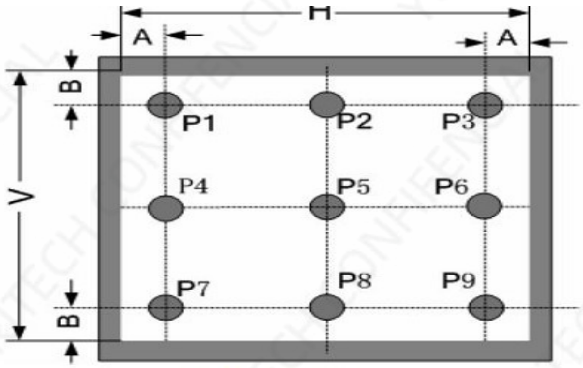


FIG2. Measuring method for Contrast ratio,surface luminance,Luminance uniformity,CIE(X,Y)chromaticity.



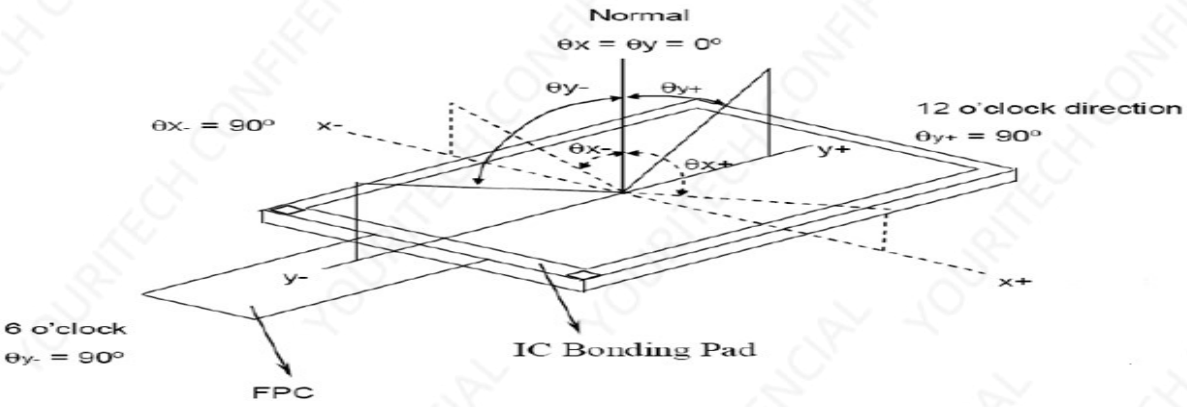
5 Points diagram



9 Points diagram

FI

G3 The definition of viewing angle 视角定义



10.Reliability Test Items

Item	Test Condition	Criterion
High Temperature Storage	70 ℃, 48 hrs	Note1,Note2
Low Temperature Storage	-20℃, 48hrs	
High Temp. & High Humidity Storage	40 ℃, 80％ RH, 48hrs	
Thermal Shock (Static)	-30℃, 30 min /80, 30 min, 20 cycles	
High Temperature Operation	60 ℃, 48 hrs	
Low temperature Operation	-10 ℃, 48 hrs	

Note1:Evaluation should be tested after storage at room temperature for two hours.
Note2:
Pass: Normal display image no line defect.
Fail: No display image, or line defects.
Partial transformation of the module parts should be ignored.

11.Precautions

Please pay attentions to the followings as using the LCD module.

Handling

(a) Do not apply strong mechanical stress like drop, shock or any force to LCD module. It may cause improper operation, even damage.

(b) Because the polarizer is very fragile and easy to be damaged, do not hit, press or rub the display surface with hard materials.

(c) Do not put heavy or hard material on the display surface, and do not stack LCD modules.

(d) If the display surface is dirty, please wipe the surface softly with cotton swab or clean cloth.

(e) Avoid using Ketone type materials (e.g. Acetone), Toluene, Ethyl acid or Methyl chloride to

clean the display surface. It might damage the touch panel surface permanently. The recommended solvents are water and Isopropyl alcohol.

(f) Wipe off water droplets or oil immediately.

(g) Protect the LCD module from ESD. It will damage the LSI and the electronic circuit.

(h) Do not touch the output pins directly with bare hands.

(i) Do not disassemble the LCD module.

(j) Do not lift the FPC of Touch Panel.

Storage

(a) Do not leave the LCD modules in high temperature, especially in high humidity for a long time.

(b) Do not expose the LCD modules to sunlight directly.

(c) The liquid crystal is deteriorated by ultraviolet. Do not leave it in strong ultraviolet ray for a long time.

(d) Avoid condensation of water. It may cause improper operation.

(e) Please stack only up to the number stated on carton box for storage and transportation. Excessive weight will cause deformation and damage of carton box.

Operation

(a) When mounting or dismounting the LCD modules, turn the power off.

(b) Protect the LCD modules from electric shock.

(c) The Driver IC control algorithms stated above should always obeyed to avoid damaging the LSI and electronic circuit.

(d) Be careful to avoid mixing up the polarity of power supply for backlight.

(e) Absolute maximum rating specified above has to be always kept in any case. Exceeding it may cause non-recoverable damage of electronic components or, nevertheless, burning.

(f) When a static image is displayed for a long time, remnant image is likely to occur.

(g) Be sure to avoid bending the FPC to an acute shape, it might break FPC.

(h) Most of the touch screens have air vent to equalize the inside air pressure to the outside one. The air vent must be open and liquid contact must be avoided as the liquid may be absorbed if the liquid is accumulated near the air vent.

(i) For the fragility of ITO film, it should avoid to use too tapering pen as the input material.

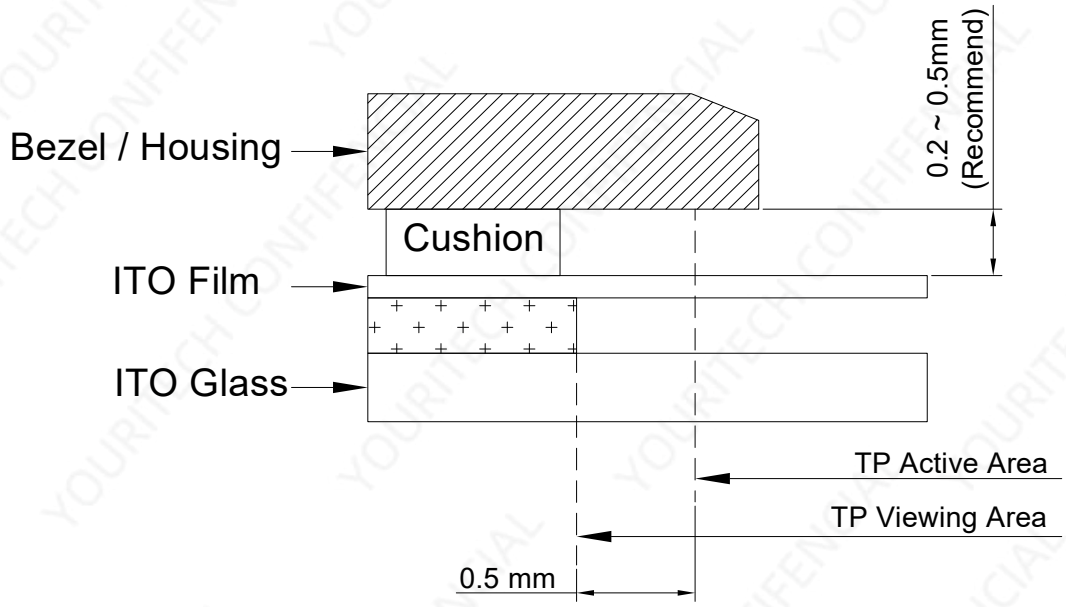
Touch Panel Mounting Notes

(a) If a cushion is used between bezel/housing and film must be choose as free as enough to absorb the expansion and contraction to avoid the distortion of film.

(b) The cushion must be placed out of the Viewing Area.

(c) Bezel/Housing edge must be posited between Key Area and Viewing Area. The edge enters the Key Area may cause unexpected input if the gap is too narrow or foreign particles like dusts exist between Bezel/Housing and ITO film.

(d) Mounting example:



The corner part has conductivity. Do not touch any metal part after mounting.

Others

a) If the liquid crystal leaks from the panel, it should be kept away from the eyes or mouth.

b) For the fragility of polarizer, it is recommended to attach a transparent protective plate over the display surface.

c) It is recommended to peel off the protection film on the polarizer slowly so that the electrostatic charge can be minimized.